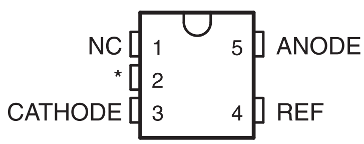
LOW-VOLTAGE ADJUSTABLE PRECISION SHUNT REGULATORS

Check for Samples: TLVH431A-Q1, TLVH431B-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Low-Voltage Operation: Down to 1.24 V**
- **Reference Voltage Tolerances at 25°C**
  - **0.5% for B Grade**
  - **1% for A Grade**
- **Adjustable Output Voltage, V_O = V_{REF} to 18 V**
- **Wide Operating Cathode Current Range: 100 μA to 70 mA**
- **0.25-Ω Typical Output Impedance**
- **–40°C to 125°C Specifications**

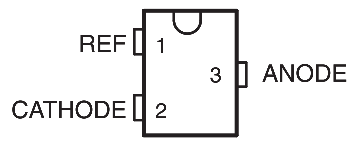
DBV (SOT-23-5) PACKAGE (TOP VIEW)



NC – No internal connection

* Pin 2 is attached to Substrate and must be connected to ANODE or left open.

DBZ (SOT-23-3) PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TLVH431 devices are low-voltage 3-terminal adjustable voltage references, with thermal stability specified over the automotive temperature range. Output voltage can be set to any value between V_{REF} (1.24 V) and 18 V with two external resistors (see Figure 2). These devices operate from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

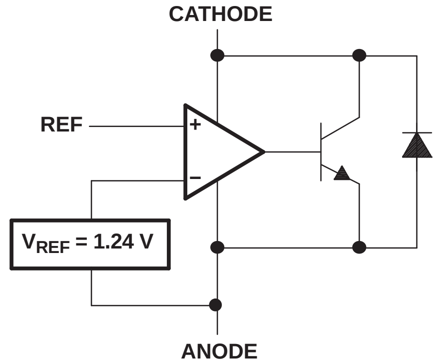
When used with an optocoupler, the TLVH431 devices are ideal voltage reference in isolated feedback circuits for 3-V to 3.3-V switching-mode power supplies. They have a typical output impedance of 0.25 Ω. Active output circuitry provides a very sharp turn-on characteristic, making the TLVH431 an excellent replacement for low-voltage Zener diodes in many applications, including on-board regulation and adjustable power supplies.

ORDERING INFORMATION(1)

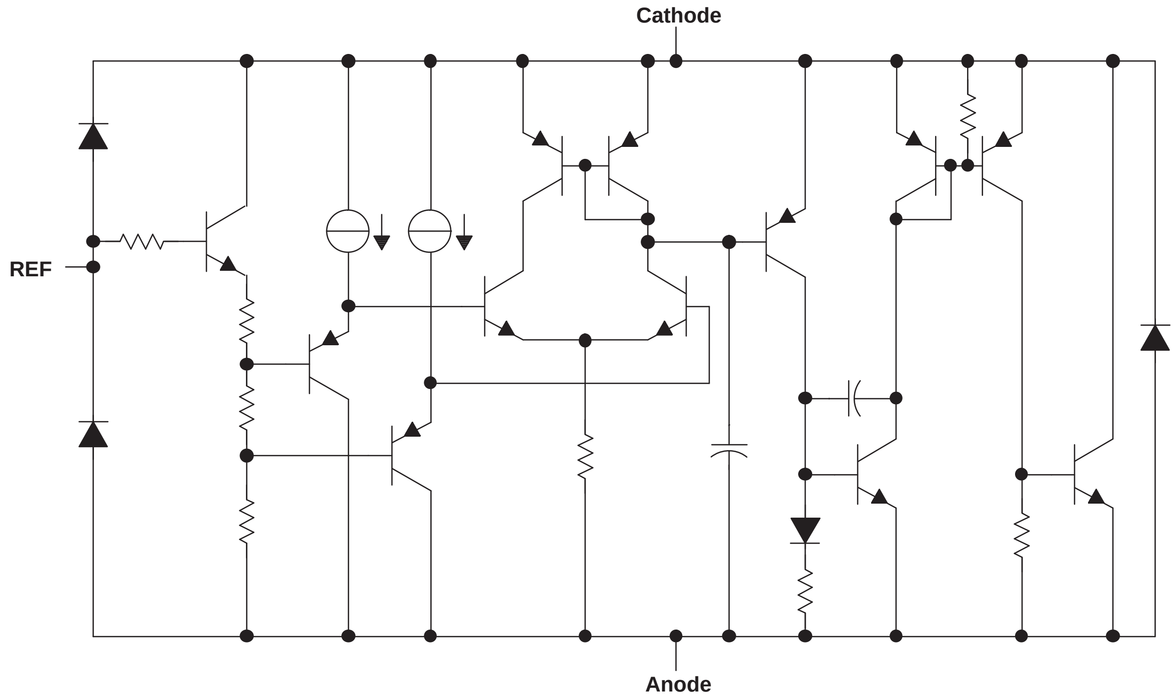
T_A	V_{REF} TOLERANCE	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	0.5%	SOT-23-5 – DBV	Reel of 3000	TLVH431BQDBVRQ1	VOPQ
	0.5%	SOT-23-3 - DBZ	Reel of 3000	TLVH431BQDBZRQ1	VPIQ
	1%	SOT-23-5 – DBV	Reel of 3000	TLVH431AQDBVRQ1	VOOQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

LOGIC BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{KA}	Cathode voltage(2)	20 V
I_K	Cathode current range	–25 mA to 80 mA
I_{ref}	Reference current range	–0.05 mA to 3 mA
θ_{JA}	Package thermal impedance(3) (4)	206°C/W
T_J	Operating virtual junction temperature	150°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the anode terminal, unless otherwise noted.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{KA}	Cathode voltage	V_{REF}	18	V
I_K	Cathode current (continuous)	0.1	70	mA
T_A	Operating free-air temperature	–40	125	°C

TLVH431A ELECTRICAL CHARACTERISTICS

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10 mA	T_A = 25°C	1.228	1.24	1.252	V
			T_A = full range(1) (see Figure 1)	1.209		1.271	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range(1) (2)	$V_{KA} = V_{REF}$, I_K = 10 mA (see Figure 1)			11	31	mV
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change to cathode voltage change	$V_K = V_{REF}$ to 18 V, I_K = 10 mA (see Figure 2)			–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 2)			0.1	0.5	μA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range(1) (2)	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 2)			0.15	0.5	μA
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 1)			60	100	μA
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 18 V (see Figure 3)			0.02	0.1	μA
$\lvert z_{KA} \rvert$	Dynamic impedance(3)	$V_{KA} = V_{REF}$, f ≤ 1 kHz, I_K = 0.1 mA to 70 mA (see Figure 1)			0.25	0.4	Ω

(1) Full temperature range is –40°C to 125°C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{^oC}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\,(T_A = 25^oC)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.
αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as:

$$\left|z_{KA}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is defined as:

$$\left|z_{KA}\right| = \frac{\Delta V}{\Delta I} \approx \left|z_{KA}\right| \times \left(1 + \frac{R1}{R2}\right)$$

TLVH431B ELECTRICAL CHARACTERISTICS

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10 mA	T_A = 25°C	1.234	1.24	1.246	V
			T_A = full range(1) (see Figure 1)	1.221		1.265	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range(1) (2)	$V_{KA} = V_{REF}$, I_K = 10 mA (see Figure 1)			11	31	mV
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change to cathode voltage change	I_K = 10 mA, $V_K = V_{REF}$ to 18 V (see Figure 2)			–1.5	–2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 2)			0.1	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range(1) (2)	I_K = 10 mA, R1 = 10 kΩ, R2 = open (see Figure 2)			0.15	0.5	µA
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 1)			60	100	µA
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 18 V (see Figure 3)			0.02	0.1	µA
$\|z_{KA}\|$	Dynamic impedance(3)	$V_{KA} = V_{REF}$, f ≤ 1 kHz, I_K = 0.1 mA to 70 mA (see Figure 1)			0.25	0.4	Ω

(1) Full temperature range is –40°C to 125°C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{^oC}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\,(T_A = 25^oC)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device.

αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as:

$$\left|z_{KA}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors (see Figure 2), the total dynamic impedance of the circuit is defined as:

$$\left|z_{KA}'\right| = \frac{\Delta V}{\Delta I} \approx \left|z_{KA}\right| \times \left(1 + \frac{R1}{R2}\right)$$

PARAMETER MEASUREMENT INFORMATION

Operation of the device at any conditions beyond those indicated under *recommended operating conditions* is not implied.

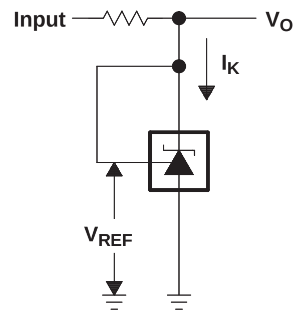


Figure 1. Test Circuit for $V_{KA} = V_{REF}$, $V_O = V_{KA} = V_{REF}$

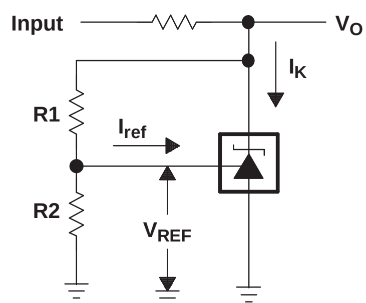


Figure 2. Test Circuit for $V_{KA} > V_{REF}$, $V_O = V_{KA} = V_{REF} \times (1 + R1/R2) + I_{ref} \times R1$

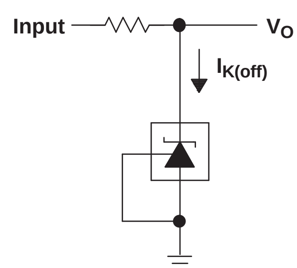


Figure 3. Test Circuit for $I_{K(off)}$

PARAMETER MEASUREMENT INFORMATION (continued)

REFERENCE VOLTAGE
vs
JUNCTION TEMPERATURE

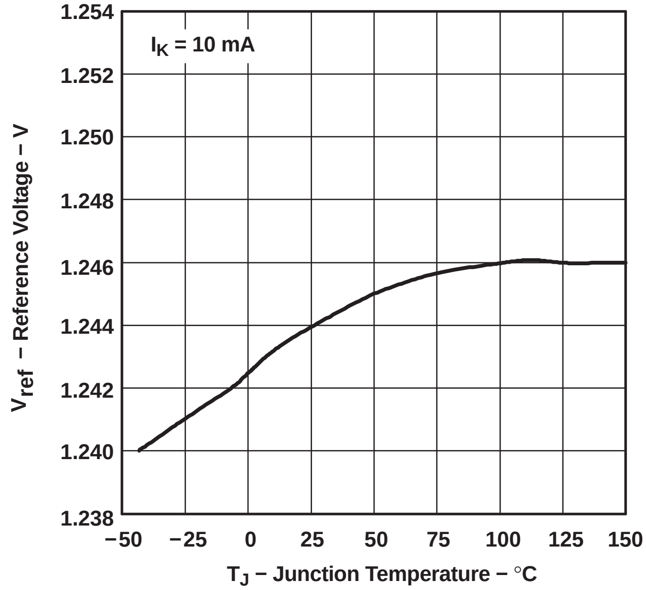


Figure 4.

REFERENCE INPUT CURRENT
vs
JUNCTION TEMPERATURE

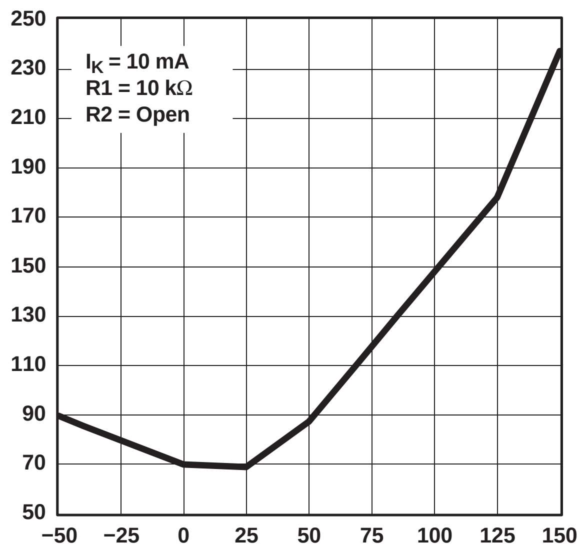


Figure 5.

PARAMETER MEASUREMENT INFORMATION (continued)

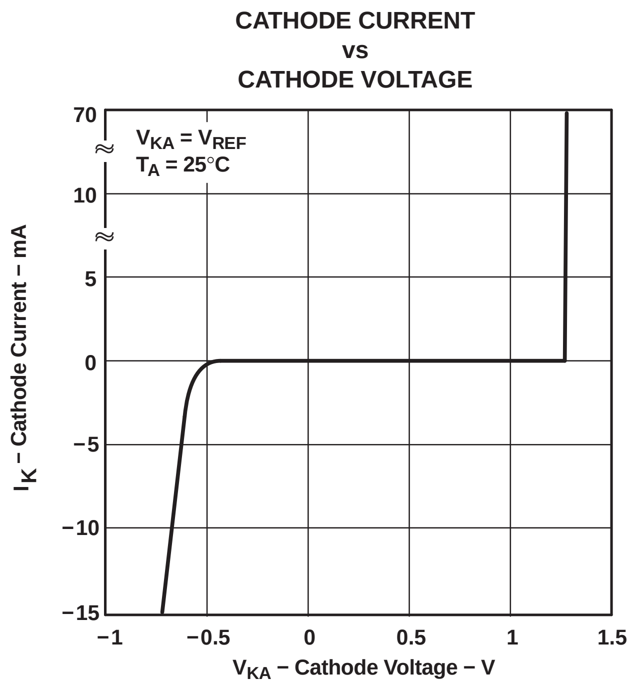


Figure 6.

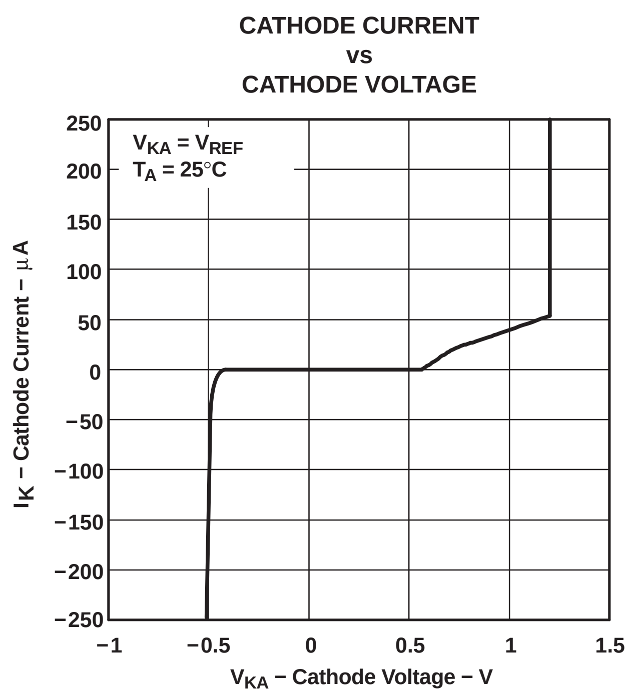


Figure 7.

PARAMETER MEASUREMENT INFORMATION (continued)

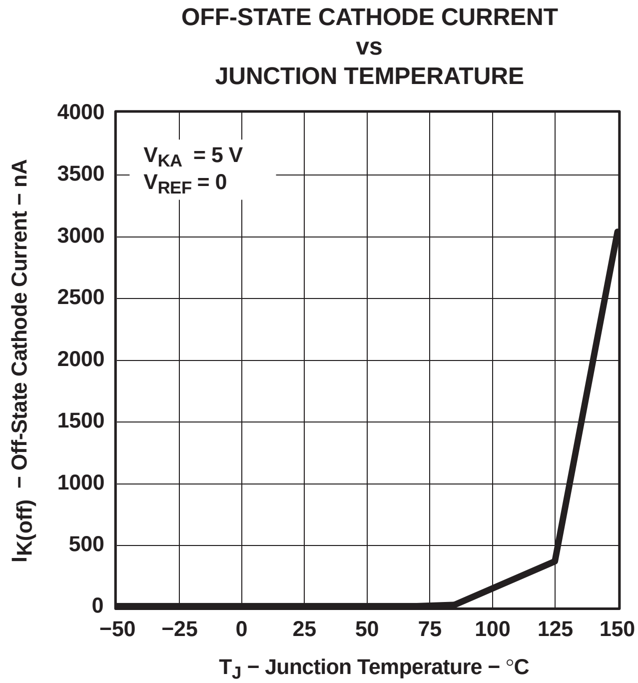


Figure 8.

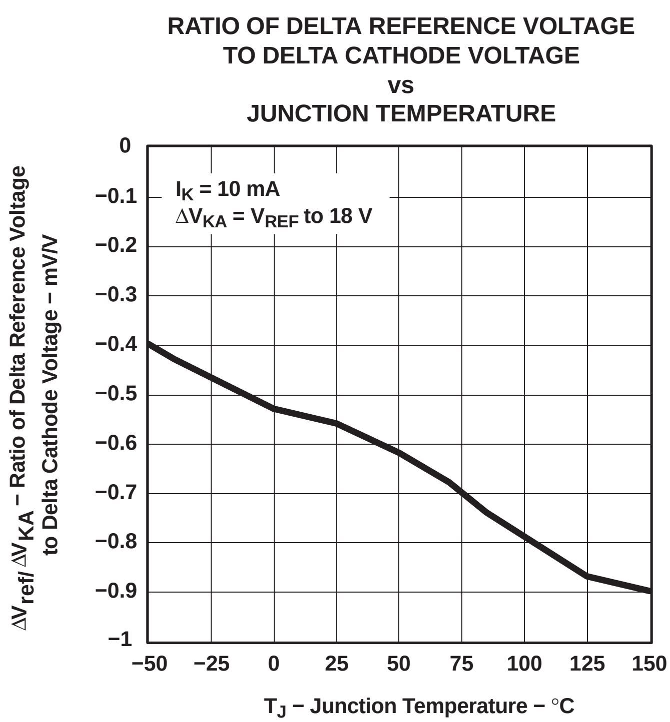
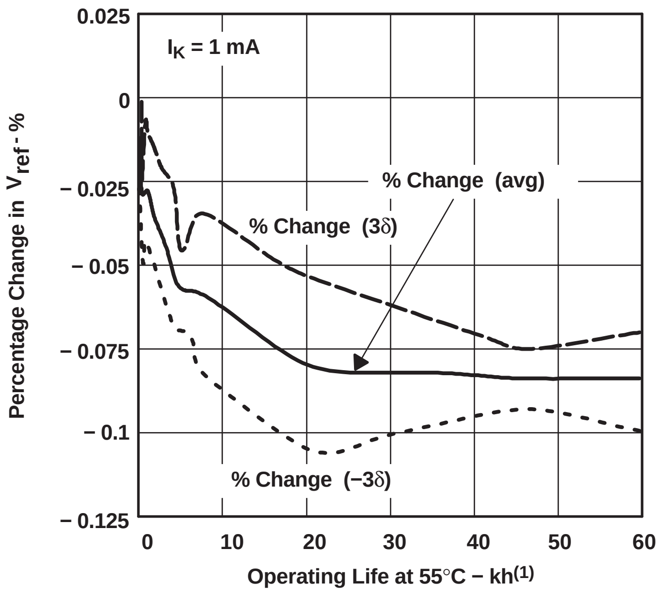


Figure 9.

PARAMETER MEASUREMENT INFORMATION (continued)

PERCENTAGE CHANGE IN V_{REF}
vs
OPERATING LIFE AT 55°C



(1) Extrapolated from life-test data taken at 125°C; the activation energy assumed is 0.7 eV.

Figure 10.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

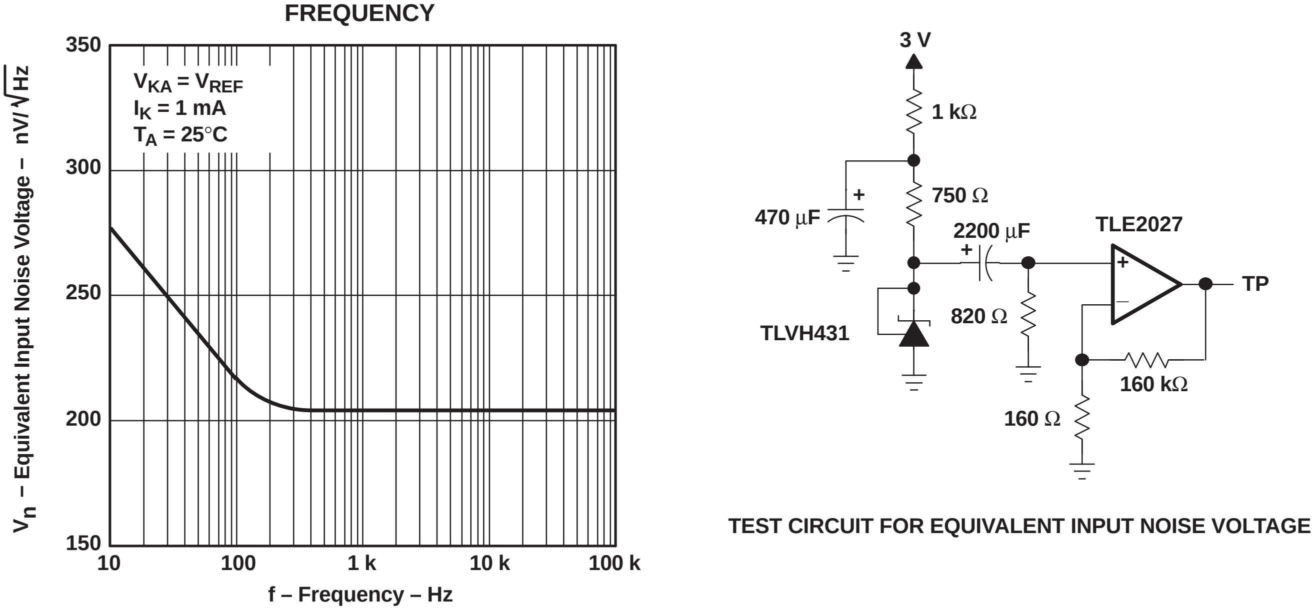
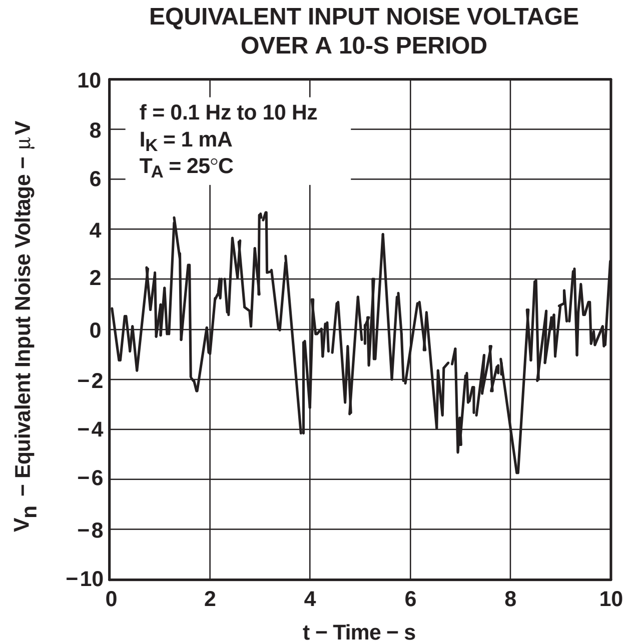
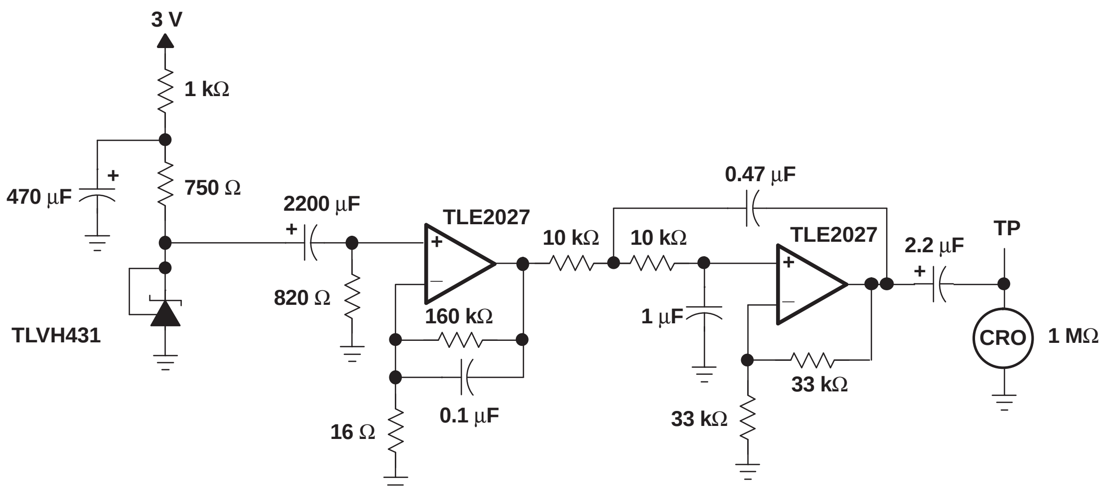


Figure 11.

PARAMETER MEASUREMENT INFORMATION (continued)

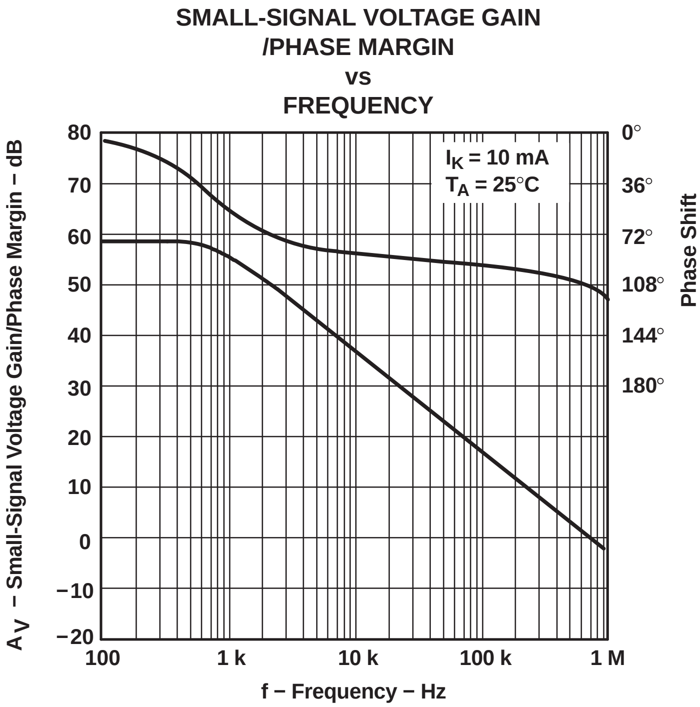




TEST CIRCUIT FOR 0.1-Hz TO 10-Hz EQUIVALENT NOISE VOLTAGE

Figure 12.

PARAMETER MEASUREMENT INFORMATION (continued)



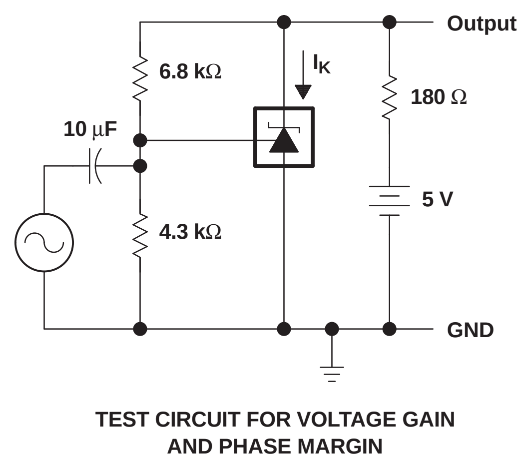
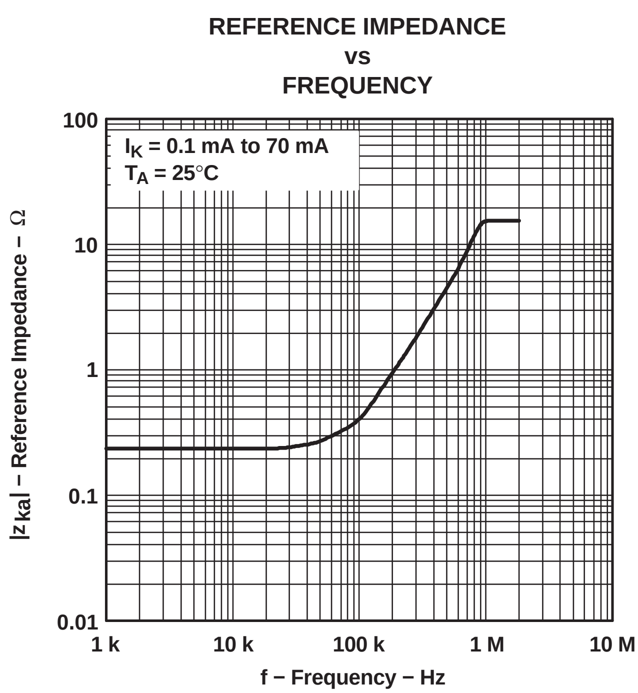


Figure 13.



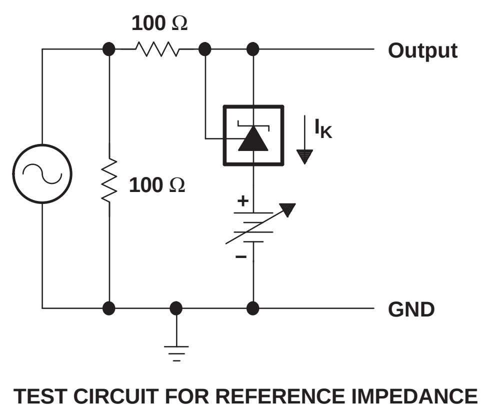
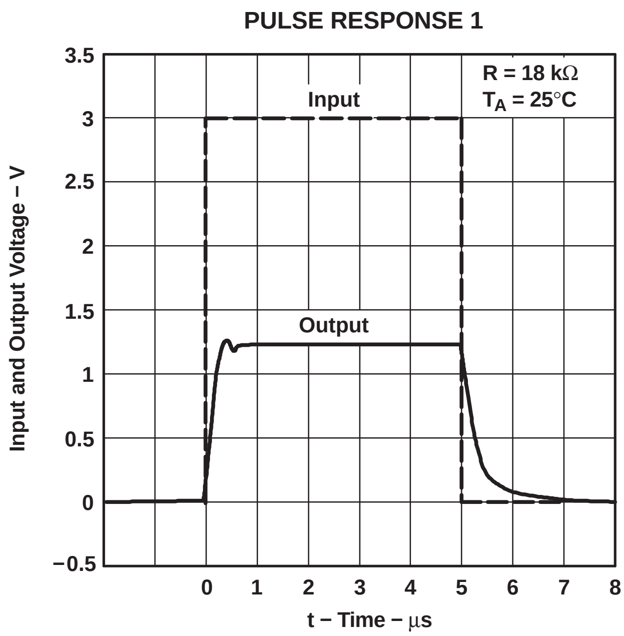
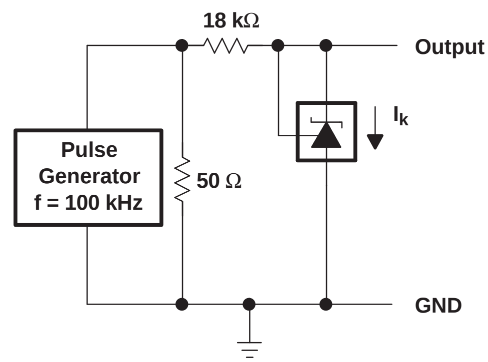


Figure 14.

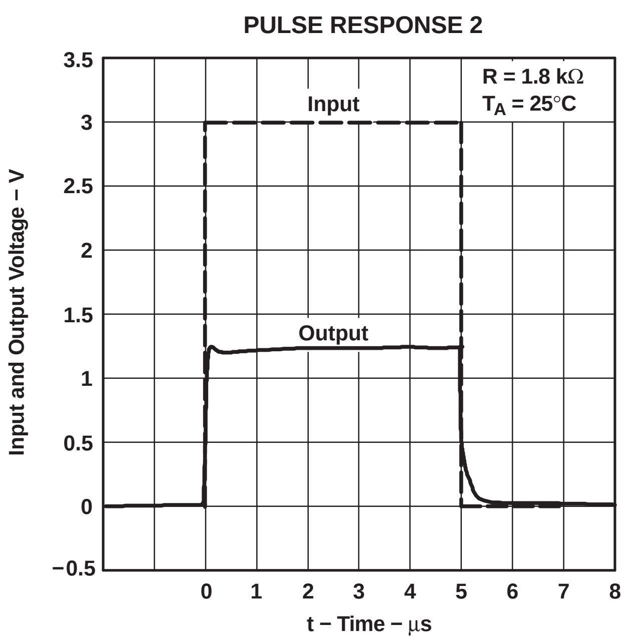
PARAMETER MEASUREMENT INFORMATION (continued)

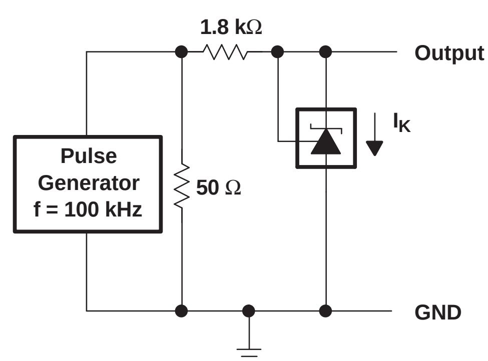




TEST CIRCUIT FOR PULSE RESPONSE 1

Figure 15.





TEST CIRCUIT FOR PULSE RESPONSE 2

Figure 16.

PARAMETER MEASUREMENT INFORMATION (continued)

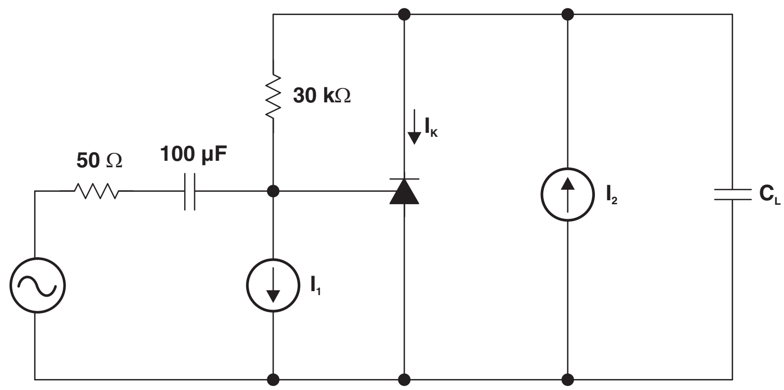


Figure 17. Phase Margin Test Circuit

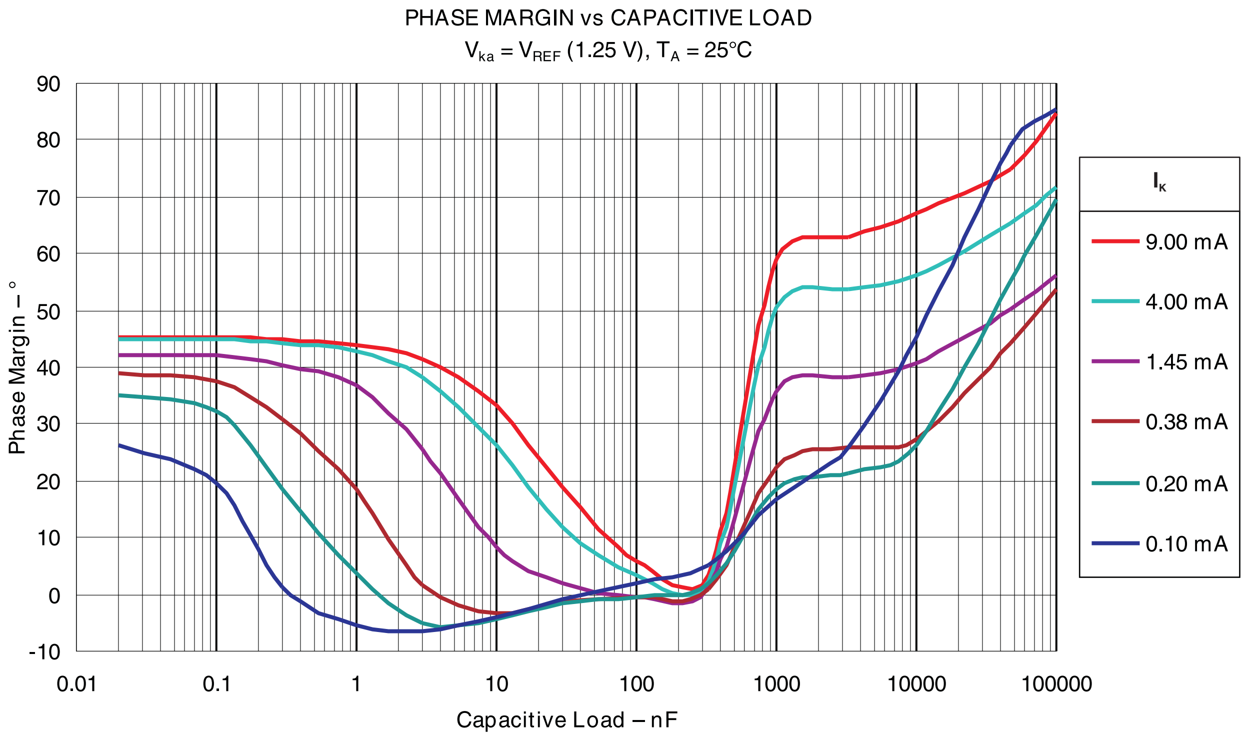


Figure 18.

PARAMETER MEASUREMENT INFORMATION (continued)

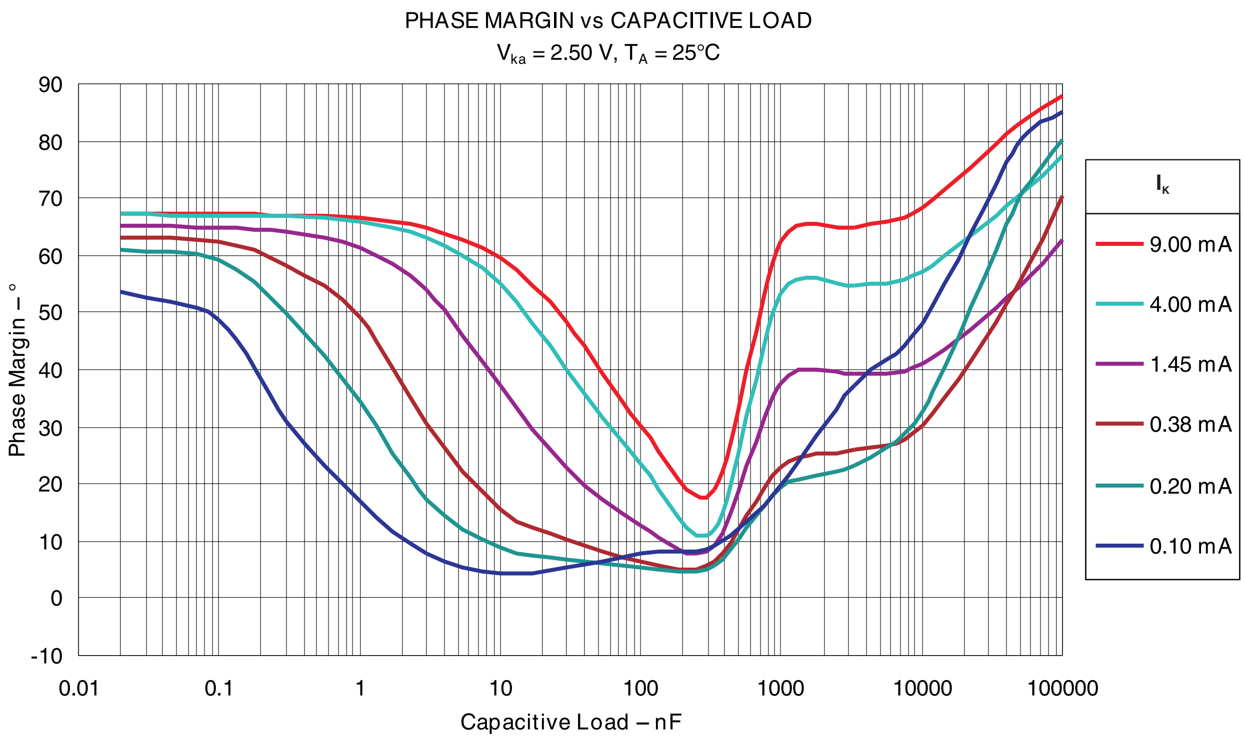


Figure 19.

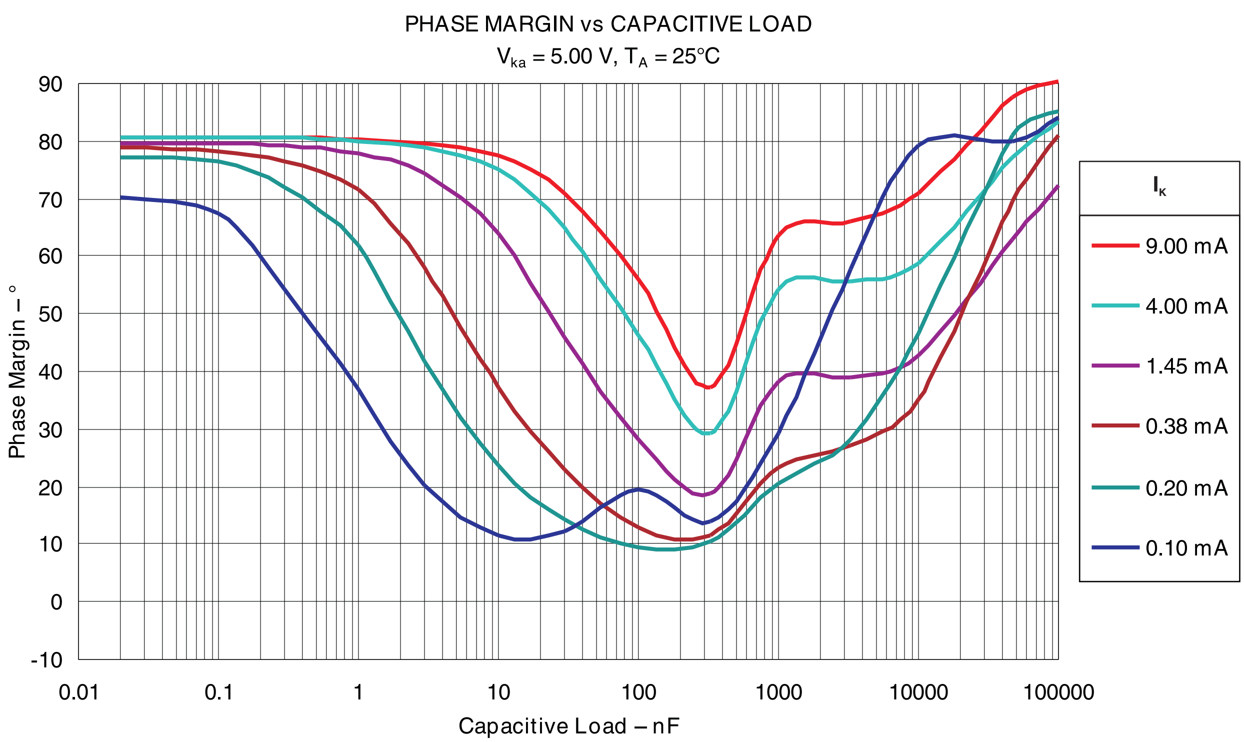


Figure 20.

APPLICATION INFORMATION

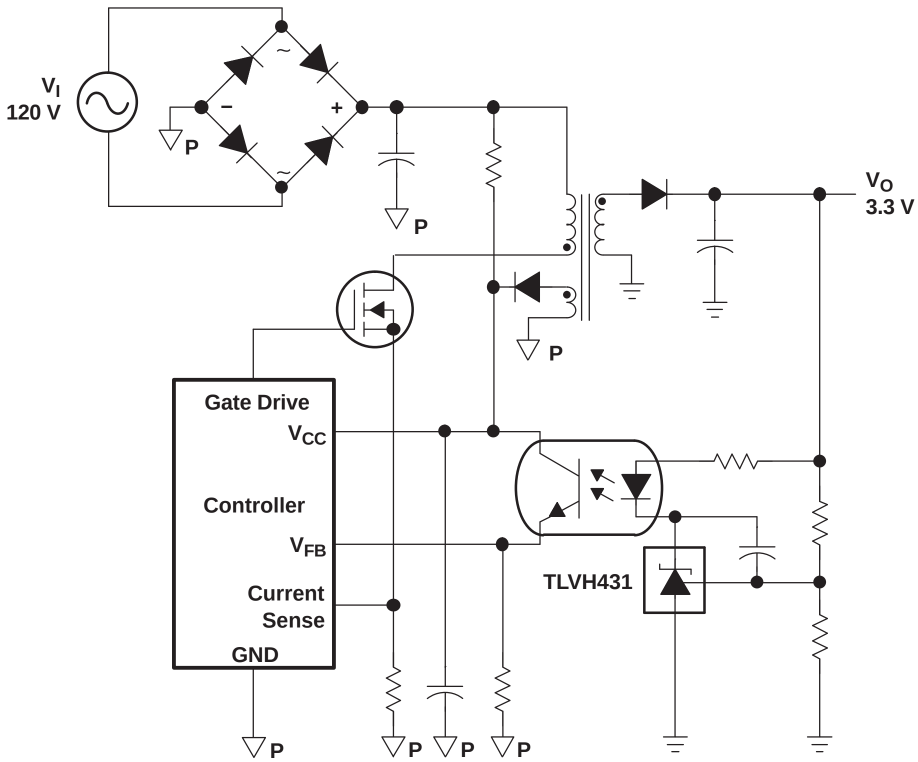


Figure 21. Flyback With Isolation Using TLVH431 as Voltage Reference and Error Amplifier

Figure 21 shows the TLVH431 used in a 3.3-V isolated flyback supply. Output voltage V_O can be as low as reference voltage V_{REF} (1.24 V). The output of the regulator plus the forward voltage drop of the optocoupler LED (1.24 + 1.4 = 2.64 V) determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7 Vdc is possible in the topology shown in Figure 21.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLVH431AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOOQ	Samples
TLVH431BQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOPQ	Samples
TLVH431BQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VPIQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLVH431A-Q1, TLVH431B-Q1 :

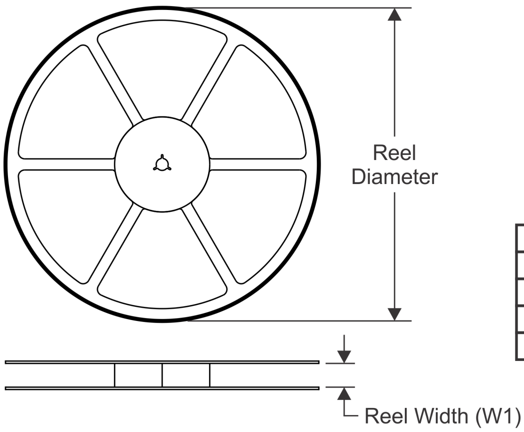
- Catalog: TLVH431A, TLVH431B

NOTE: Qualified Version Definitions:

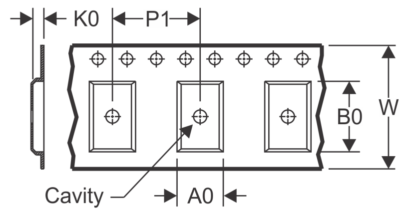
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

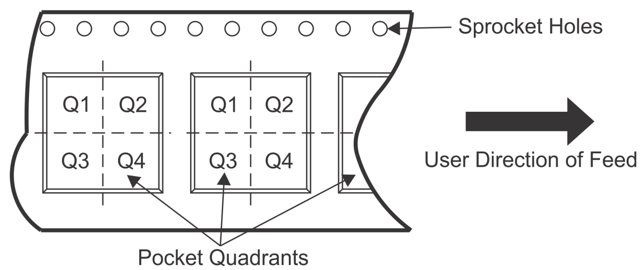


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

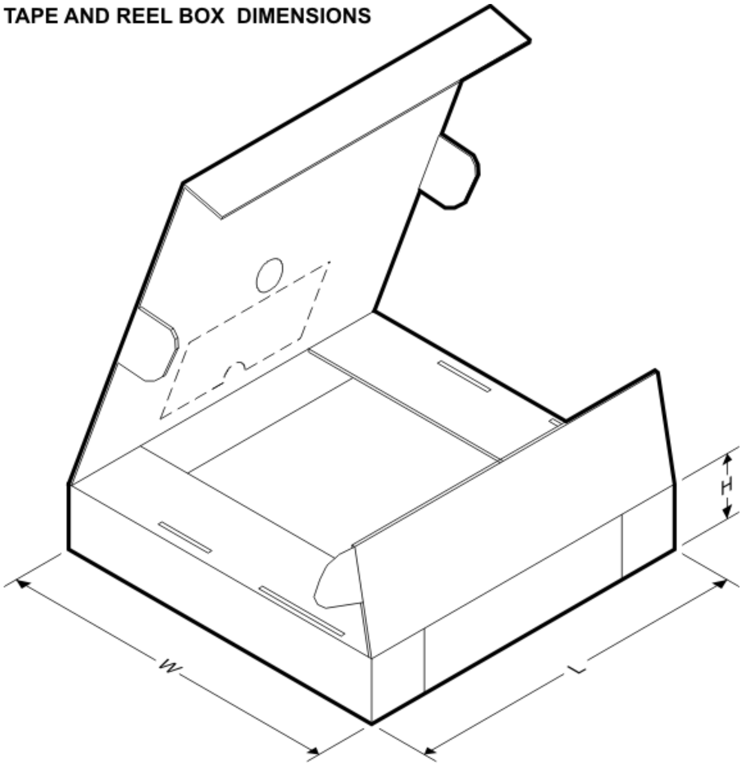
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLVH431AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLVH431BQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLVH431BQDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

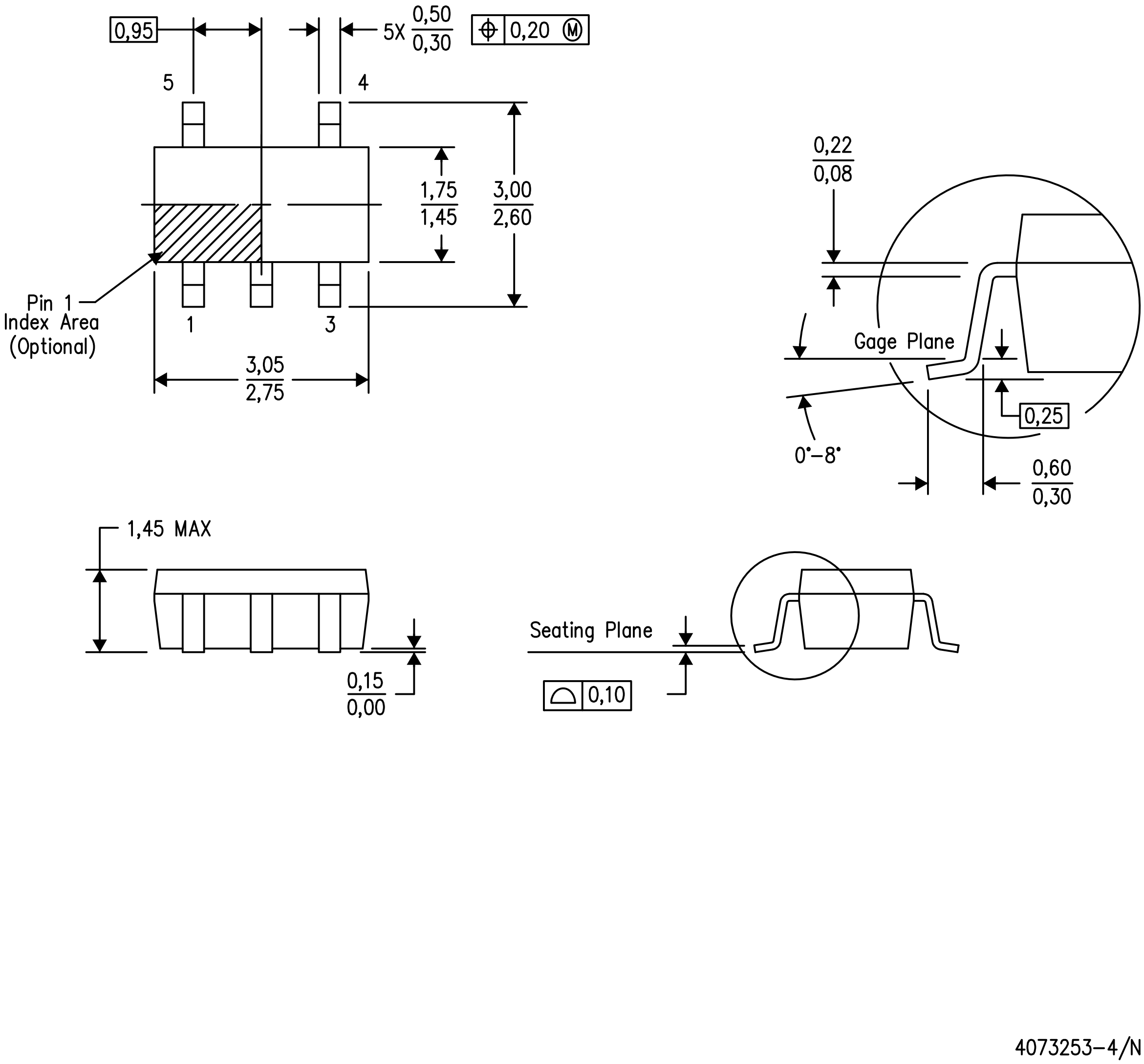
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

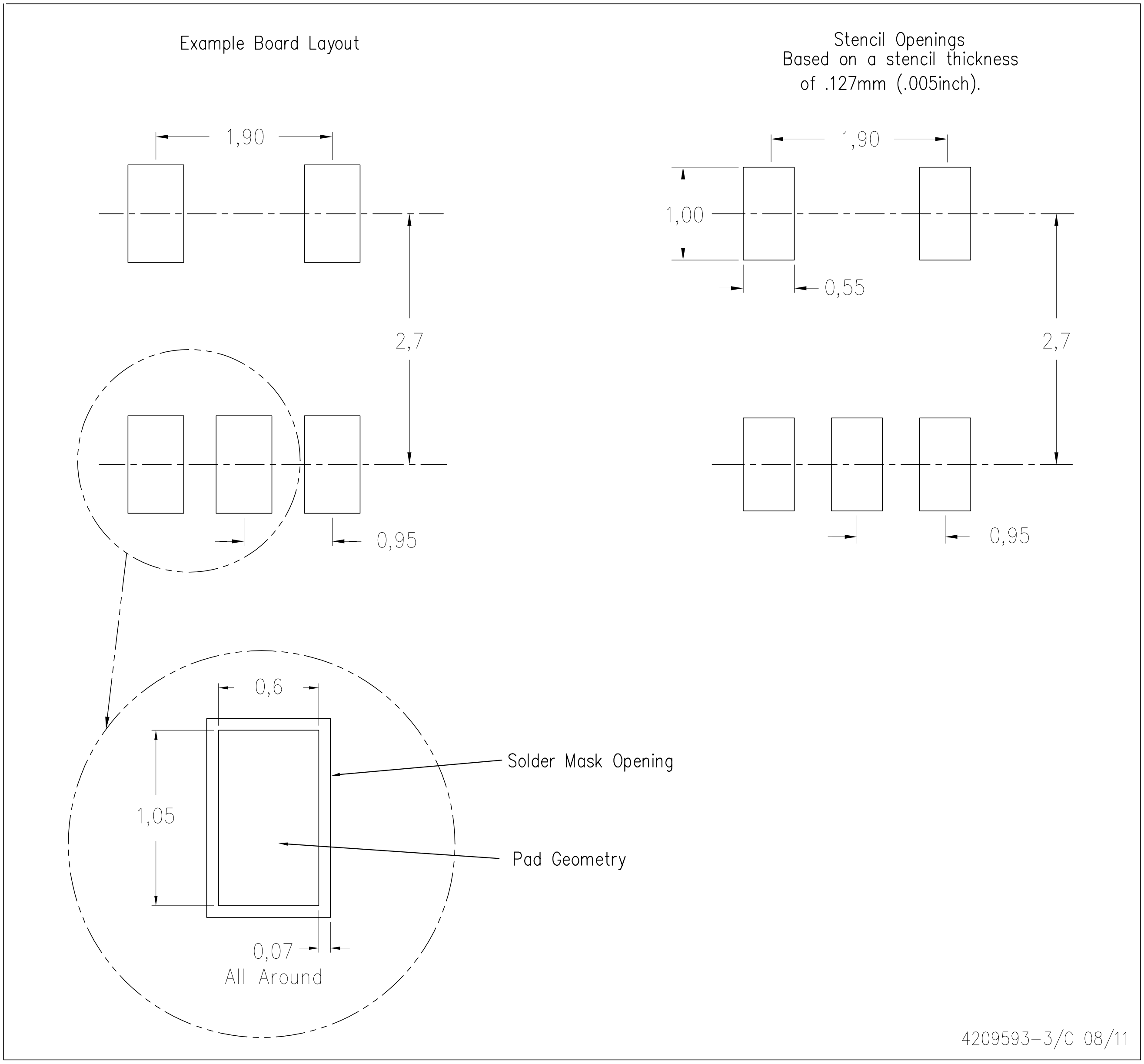
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLVH431AQDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
TLVH431BQDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
TLVH431BQDBZRQ1	SOT-23	DBZ	3	3000	203.0	203.0	35.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



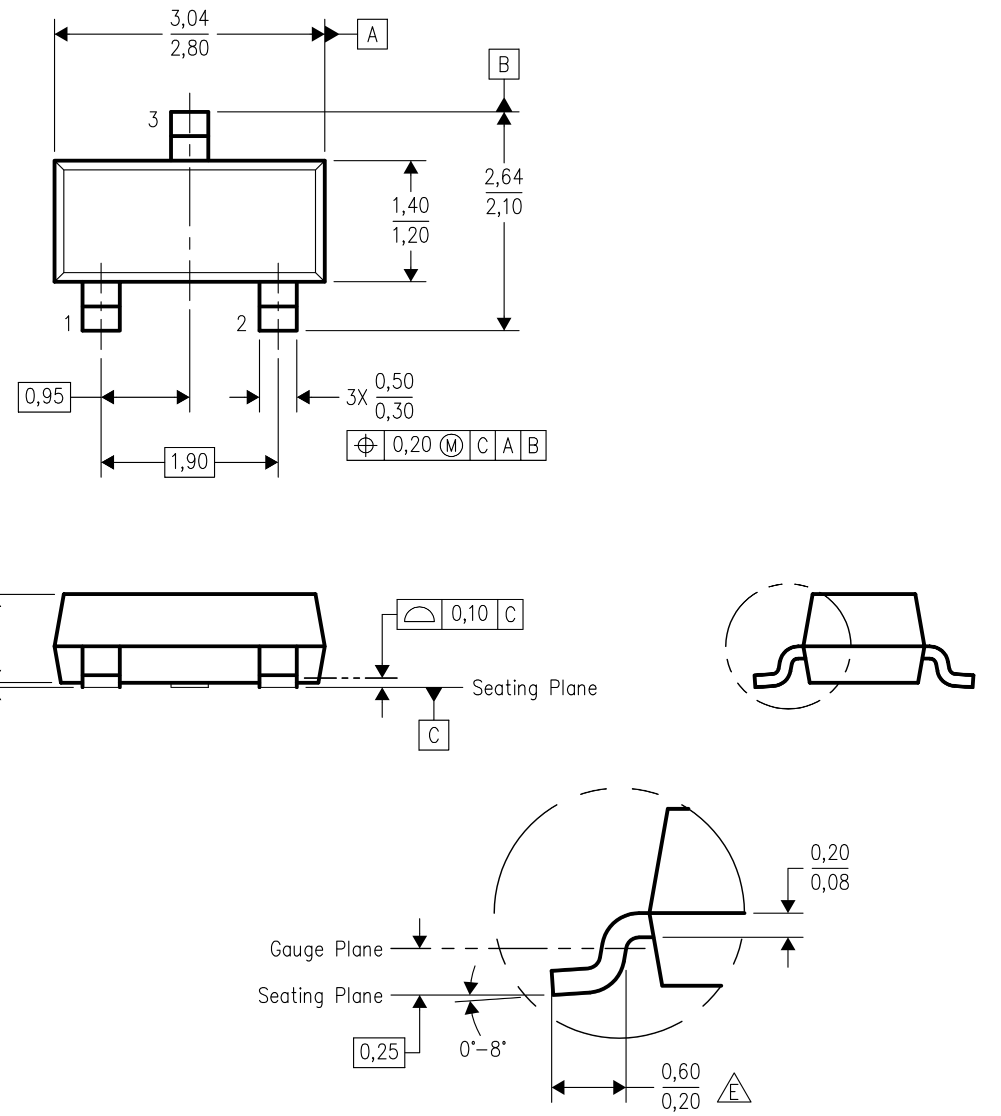
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DBZ (R-PDSO-G3) PLASTIC SMALL-OUTLINE



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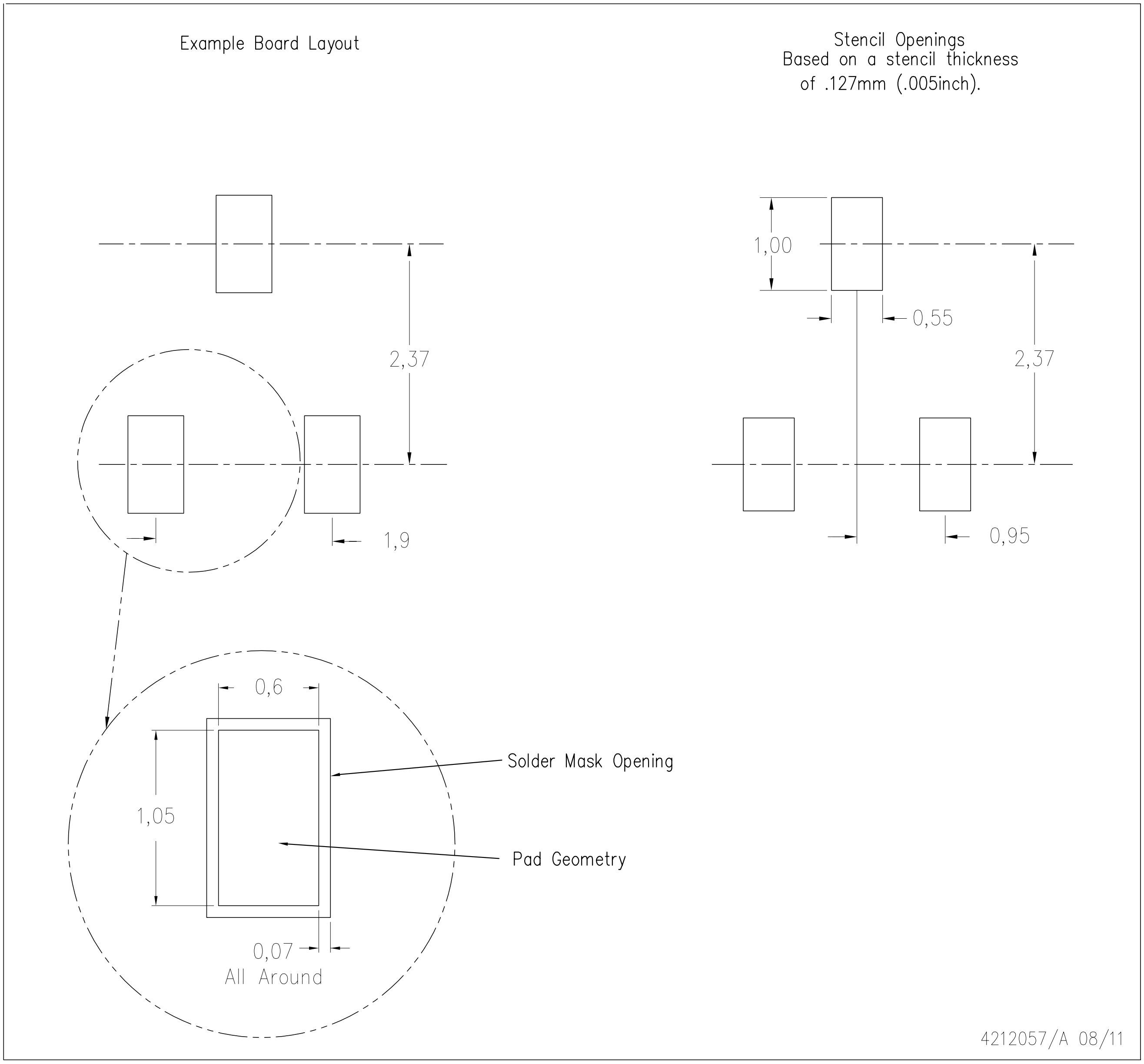
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Lead dimensions are inclusive of plating.
- D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
- E. Falls within JEDEC TO–236 variation AB, except minimum foot length.

DBZ (R–PDSO–G3) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.