MULTI-ISSUE 64-BIT MICROPROCESSOR

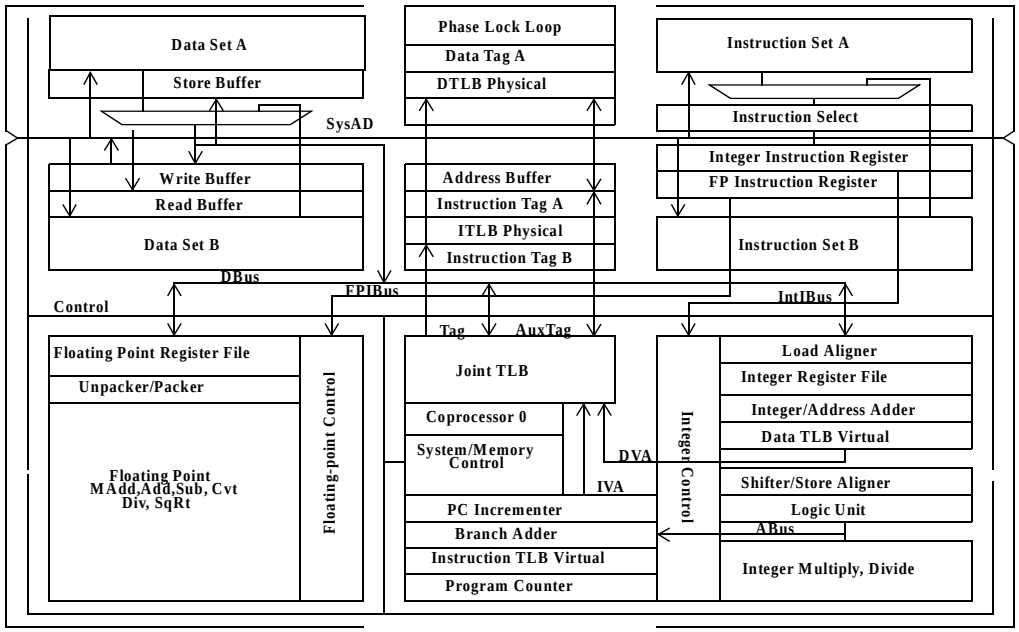
79RC5000

RISController

Features

- **Dual issue super-scalar execution core**
  - *250 MHz frequency*
  - *Dual issue floating-point ALU operations with other instruction classes*
  - *Traditional 5-stage pipeline, minimizes load and branch latencies*
- **Single-cycle repeat rate for most floating point ALU operations**
- **High level of performance for a variety of applications**
  - *High-performance 64-bit integer unit achieves 330 dhrystone MIPS (dhrystone 2.1)*
  - *Ultra high-performance floating-point accelerator, directly implementing single- and double-precision operations achieves 500mflops*
  - *Extremely large on-chip primary cache*
  - *On-chip secondary cache controller*
- **MIPS-IV 64-bit ISA for improved computation**
  - *Compound floating-point operations for 3D graphics and floating-point DSP*
  - *Conditional move operations*
- **Large on-chip TLB**
- **Active power management, including use of WAIT operation**
- **Large, efficient on-chip caches**
  - *32KB Instruction Cache, 32KB Data Cache*
  - *2-set associative in each cach*
  - *Virtually indexed and physically tagged to minimize cache flushes*
  - *Write-back and write-through selectable on a per page basis*
  - *Critical word first cache miss processing*
  - *Supports back-to-back loads and stores in any combination at full pipeline rate*
- **High-performance memory system**
  - *Large primary caches integrated on-chip*
  - *Secondary cache control interface on-chip*
  - *High-frequency 64-bit bus interface runs up to 125MHz*
  - *Aggregate bandwidth of on-chip caches, system interface of 5.6GB/s*
  - *High-performance write protocols for graphics and data communications*
- **Compatible with a variety of operating systems**
  - *Windows™ CE*
  - *Numerous MIPS-compatible real-time operating systems*
- **Uses input system clock, with processor pipeline clock multiplied by a factor of 2-8**
- **Industrial and commercial temperature range**

Block Diagram



The IDT logo is a registered trademark and RC32134, RC32364, RC64145, RC64474, RC64475, RC4650, RC4640, RC4600,RC4700 RC3081, RC3052, RC3051, RC3041, RISController, and RISCore are trademarks of Integrated Device Technology, Inc.

© 2001 Integrated Device Technology, Inc.

DESCRIPTION

The RC5000 serves many performance critical embedded applications, such as high-end internetworking systems, color printers, and graphics terminals.

The RC5000 is optimized for high-performance applications, with special emphasis on system bandwidth and floating point operations, through integration of high-performance computational units and a high-performance memory hierarchy. For this class of application, the result is a relatively low-cost CPU capable of approximately 330 Dhrystone MIPS.

IDT's objectives in offering the RC5000 include:

- Offering a high performance upgrade path to existing embedded customers in the internetworking, office automation and visualization markets.
- Providing a significant improvement in the floating- point performance currently available in a moderately priced MIPS CPU.
- Providing improvements in the memory hierarchy of desktop systems by using large primary caches and integrating a secondary cache controller.
- Enabling improvements in performance through the use of the MIPS-IV ISA.

Instruction Issue Mechanism

The RC5000 recognizes two general classes of instructions for multi-issue:

- Floating-point ALU
- All others

These instruction classes are pre-decoded by the RC5000, as they are brought on-chip. The pre-decoded information is stored in the instruction cache.

Assuming that there are no pending resource conflicts, the RC5000 can issue one instruction per class per pipeline clock cycle. Note that this broad separation of classes insures that there are no data dependencies to restrict multi-issue.

However, long-latency resources in either the floating-point ALU (e.g. DIV or SQRT instructions) or instructions in the integer unit (such as multiply) can restrict the issue of instructions. Note that the R5000 does not perform out-of-order or speculative execution; instead, the pipeline slips until the required resource becomes available.

There are no alignment restrictions on dual-issue instruction pairs. The RC5000 fetches two instructions from the cache per cycle. Thus, for optimal performance, compilers should attempt to align branch targets to allow dual-issue on the first target cycle, since the instruction cache only performs aligned fetches.

Instruction Set Architecture

The RC5000 implements the MIPS-IV 64-bit ISA, including CP1 and CP1X functional units (and their instruction set).

Integer Pipeline

The RC5000 is a limited dual-issue machine that utilizes a traditional 5-stage integer pipeline. This basic integer pipeline of the RC5000 is illustrated in Figure 1. The integer instruction execution speed is tabulated (in number of pipeline clocks) as follows:

Operation	Latency	Repeat
Load	2	1
Store	2	1
MULT/MULTU	8	8
DMULT/DMULTU	12	12
DIV/DIVU	36	36
DDIV/DDIVU	68	68
Other Integer ALU	1	1
Branch	2	2
Jump	2	2

Table 1 Integer Instruction Execution Speed

The RC5000's short pipeline keeps the load and branch latencies very low. The caches contain special logic that allows any combination of loads and stores to execute in back-to-back cycles without requiring pipeline slips or stalls. (This assumes that the operation does not miss in the cache.)

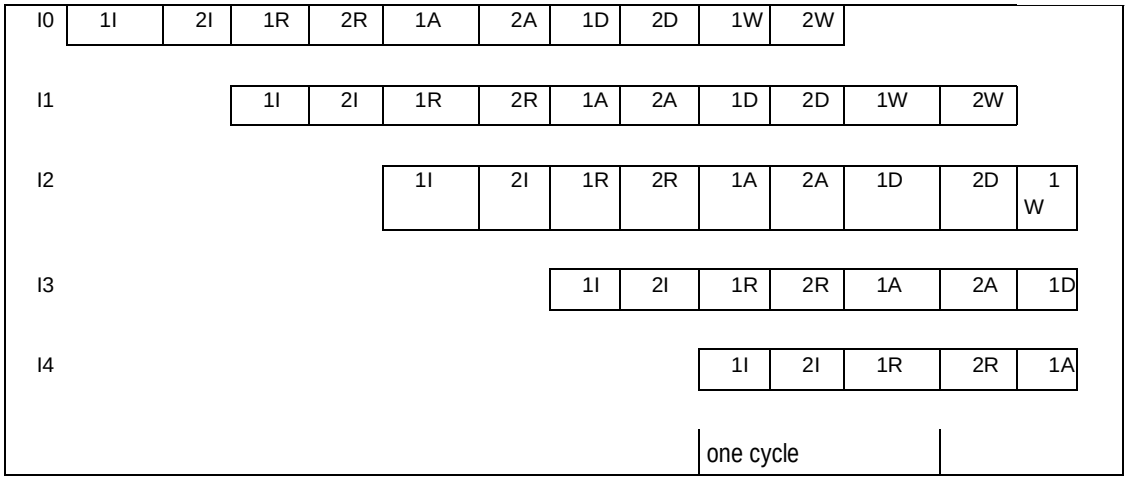


Figure 1 R5000 Integer Pipeline Stages

Key to Figure

1I-1R	Instruction cache access
2I	Instruction virtual to physical address translation
2A-2D	Data cache access and load align
1D	Data virtual to physical address translation
1D-2D	Virtual to physical address translation
2R	Register file read
2R	Bypass calculation
2R	Instruction decode
2R	Branch address calculation
1A	Issue or slip decision
1A-2A	Integer add, logical, shift
1A	Data virtual address calculation
2A	Store align
1A	Branch decision
2W	Register file write

RC5000 Computational Units

The RC5000 contains the following computational units:

Integer ALU. The RC5000 implements a full, single-cycle 64-bit ALU for all integer ALU functions other than multiply and divide. Bypassing is used to support back-to-back ALU operations at the full pipeline rate, without requiring stalls for data dependencies.

Integer Multiply/Divide Unit. This unit is separated from the primary ALU, to allow these longer latency operations to run in parallel with other operations. The pipeline stalls only if an attempt to access the HI or LO registers is made before the operation completes.

Floating-point ALU. This unit is responsible for all CP1/CP1X ALU operations other than DIV/SQRT. The unit is pipelined to allow a single-cycle repeat rate for single-precision operations

Floating-point DIV/SQRT unit. This unit is separated from the other floating-point ALU, so that these long latency operations do not prevent the issue of other floating point operations.

In addition, the RC5000 implements separate logical units to implement loads, stores, and branches.

Operating Frequency

The input clock operates in a frequency range of 33MHz to 100MHz. The pipeline frequency for the RC5000 is 2 to 8 times the input clock (up to the maximum for the speed grade of CPU).

Thermal Considerations

The RC5000 utilizes special packaging techniques, to improve the thermal properties of high-speed processors. The RC5000 is packaged using cavity down packaging in a 223-pin PGA package with integral thermal slug, and a 272-pin BGA package. These packages effectively dissipate the power of the CPU, increasing device reliability.

The RC5000 utilizes an all-aluminum package with the die attached to a normal copper lead frame mounted to the aluminum casing. Due to the heat-spreading effect of the aluminum, the package allows for an efficient thermal transfer between the die and the case. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation.

The RC5000 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package.

The following equation relates ambient and case temperatures:

$T_A = T_C - P * \varnothing_{CA}$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device. Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 1.

	$\varnothing_{CA}$					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
PGA	16	7	5	3	2.5	2
BGA	14	6	4	3	2.5	2

Table 2 Thermal Resistance (ýCA) at Various Airflows

Note: The RC5000 implements advanced power management to substantially reduce the average power dissipation of the device. This operation is described in the *IDT79RV5000 RISC Microprocessor Reference Manual.*

Note:

Per the RC5000 Documentation errata, Revision 1.0, dated February 1999 and per the RC5000 Device errata, dated February 1999, mode bits 20, 33 and 37 must be set to 1.

Revision History

January 1996: Corrected pin list for Clock/Control, Initialization, and Secondary Cache interfaces in Pin Description section. Changed pins AA19 and AA21 from Vcc to Vss in Advance Pin-Out section.

March 1997: Upgraded data sheet status from "Preliminary" to Final. Added section on thermal considerations. Added section on absolute maximum ratings.

June 1997: Revised Power Consumption and System Interface Parameters.

September 1997: Added user notation on Boot Mode Bits 20 and 33 for 200 MHz frequency.

June 1998: Added 250 MHz. Changed naming conventions.

June 1999: Added 267 MHz and 300 MHz.

October 28, 1999: Added industrial temperature data and revised package designation code in the Ordering Information section.

March 23, 2000: Expanded the data presentation in the System Interface Parameters table and revised the values in this table.

April 10, 2001: In the Data Output and Data Output Hold categories of the System Interface Parameters table, changed values in the Min column for all speeds from 1.5 and 1.0 to 0.

Logic Diagram

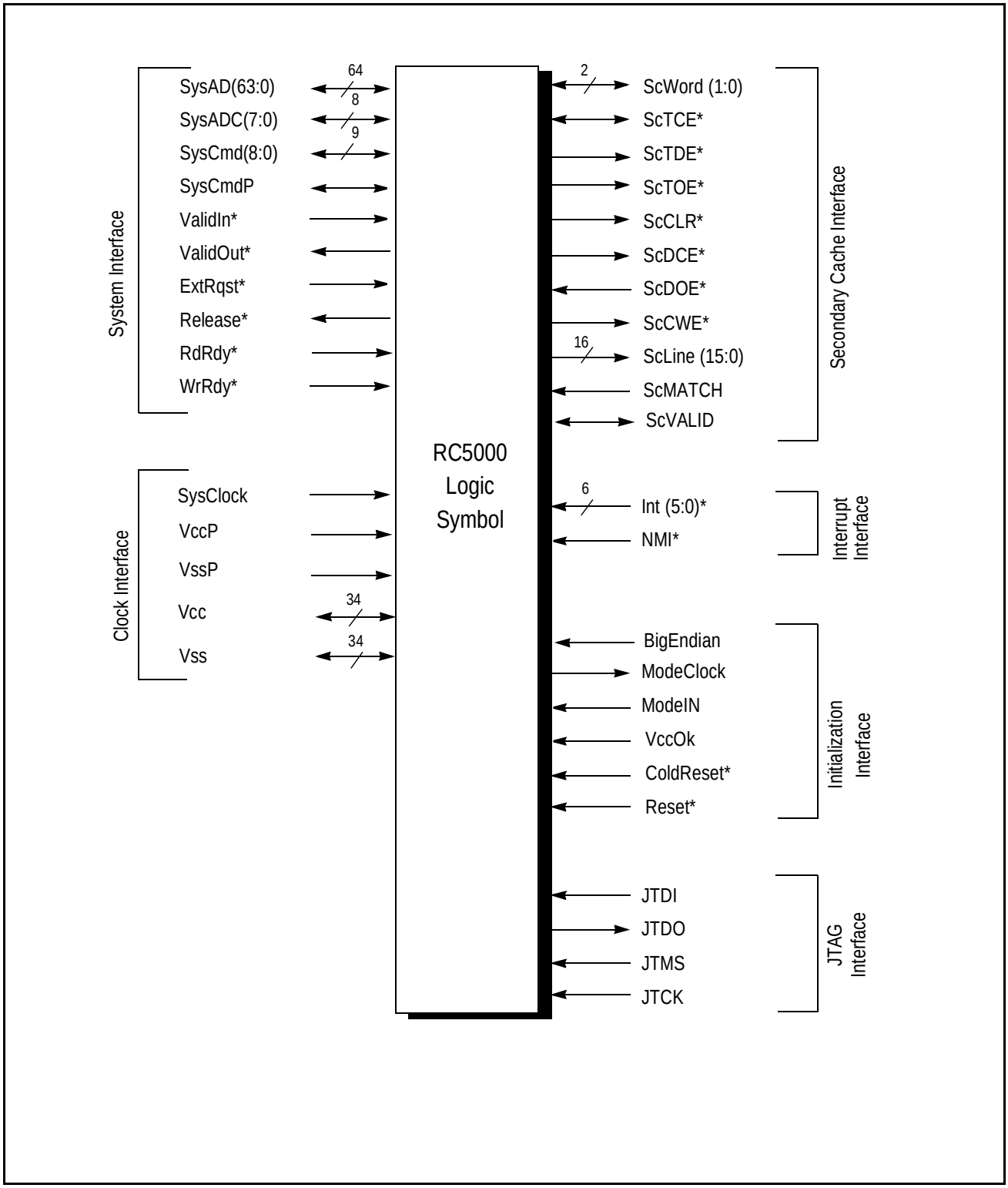


Figure 2 RC5000 Logic Symbol Diagram

Pin Description

The RC5000 implements a bus similar to that of the RC4700. Table 2 lists and describes the RC5000 signals.

Pin Name	Type	Description
System interface		
ExtRqst*	Input	**External Request.** Signals that the system interface needs to submit an external request.
Release*	Output	**Release Interface.** Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	**Read Ready.** Signals that an external agent can now accept a processor read.
WrRdy*	Input	**Write Ready.** Signals that an external agent can now accept a processor write request.
ValidIn*	Input	**Valid Input.** Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	**Valid Output.** Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	Input/ Output	**System Address/Data bus.** A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/ Output	**System Address/Data check bus.** An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	Input/ Output	**System Command/data identifier bus.** A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/ Output	**Reserved System Command/data identifier bus parity.** For the RC5000, unused on input and zero on output.
Clock/control interface		
SysClock	Input	**Master Clock.** Master clock input at the bus frequency. The pipeline clock is derived by multiplying this clock up.
VCCP	Input	**Quiet VCC for PLL.** Quiet VCC for the internal phase locked loop.
VSSP	Input	**Quiet VSS for PLL.** Quiet VSS for the internal phase locked loop.
Interrupt interface		
Int(5:0)*	Input	**Interrupt.** Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt. Non-maskable interrupt, ORed with bit 6 of the interrupt register.
JTAG interface:		
JTDI	Input	**JTAG Data In.** Connected directly to JTDO. No JTAG implemented; should be pulled High.
JTCK	Input	**JTAG Clock Input.** Unused input; should be pulled High.

Table 3: RC5000 Signal Names and Descriptions (Page 1 of 2)

Pin Name	Type	Description
JTDO	Output	**JTAG Data Out.** Connected directly to JTDI. If no external scan used, this is a no connect.
JTMS	Input	**JTAG Command.** Unused input. Should be pulled High.

Initialization interface:

VCCOk	Input	**VCC is OK.** When asserted, this signal indicates to the RC5000 that the power supply has been above Vcc minimum for more than 100 milliseconds and will remain stable. The assertion of VCCOk initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	**Cold Reset.** This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with SysClock.
Reset*	Input	**Reset.** This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or syn chronously to initiate a warm reset. Reset must be synchronously de-asserted with SysClock.
ModeClock	Output	**Boot Mode Clock.** Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	**Boot Mode Data In.** Serial boot-mode data input.
BigEndian	Input	**Endian mode select.** Allows the system to change the processor addressing mode without rewriting the mode ROM. If endianness is to be specified by using the BigEndian pin, program mode ROM bit 8 to 0; if endianness is to be specified by the mode ROM, ground the BigEndian pin.

Secondary cache interface:

ScCLR*	Output	**Secondary Cache Block Clear.** Clears all valid bits in those Tag RAM's which support this function.
ScCWE*(1:0)	Output	**Secondary Cache Write Enable.** Asserted during writes to the secondary cache
ScDCE*(1:0)	Output	**Data RAM Chip Enable.** Chip Enable for Secondary Cache Data RAM
ScDOE*	Input	**Data RAM Output Enable.** Asserted by the external agent to enable data onto the SysAD bus
ScLine (15:0)	Output	**Data RAM Output Enable.** Cache line index for secondary cache
ScMATCH	Input	**Secondary cache Tag Match.** Asserted by Tag RAM on Secondary cache tag match
ScTCE*	Output	**Secondary cache Tag RAM Chip Enable.** Chip enable for secondary cache tag RAM.
ScTDE*	Output	**Secondary cache Tag RAM Data Enable.** Data Enable for Secondary Cache Tag RAM.
ScTOE*	Output	**Secondary cache Tag RAM Output Enable.** Tag RAM Output enable for Secondary Cache Tag RAM's
ScWord (1:0)	Input/ Output	**Secondary cache Word Index.** Determines correct double-word of Secondary cache Index
ScValid	Input/ Output	**Secondary cache Valid.** Always driven by the CPU except during a cache probe operation, when it is driven by the tag RAM.

Table 3: RC5000 Signal Names and Descriptions (Page 2 of 2)

Absolute Maximum Ratings

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Symbol	Rating	Commercial (3.3V±5%)	Industrial (3.3V±5%)	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5[1] to +4.6	–0.5[1] to +4.6	V
T_C	Operating Temperature (case)	0 to +85	-40 to +85	°C
T_{BIAS}	Case Temperature Under Bias	–55 to +125	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	–55 to +125	°C
I_{IN}	DC Input Current	20[2]	20[3]	mA
I_{OUT}	DC Output Current	50[4]	50[5]	mA

1. IN minimum = –2.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
2. .When VIN < 0V or VIN > VCC.
3. .When VIN < 0V or VIN > VCC.
4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.
5. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

Recommended Operation Temperature and Supply Voltage

Grade	Temperature	GND	RV5000 V_{cc}
Commercial	0°C to +85°C (Case)	0V	3.3V±5%
Industrial	-40°C to +85°C (Case)	0V	3.3V±5%

AC Electrical Characteristics

(V_{CC}= 3.3V± 5%; T_{case} = 0°C to +85°C for commercial or T_{case} = -40°C to +85°C for industrial)

Clock Parameters—RC5000

Note: Boot Mode Bits 20, 33 and 37 must be set to "1" for all frequencies

Parameter	Symbol	180MHz		200MHz		250MHz		Units
		Min	Max	Min	Max	Min	Max	
Pipeline Clock Frequency	PCLk	100	180	100	200	100	250	
SysClock HIGH	t_{SCHIGH}	3	—	3	—	3	—	ns
SysClock LOW	t_{SCLOW}	3	—	3	—	3	—	ns
SysClock Frequency	_	33	90	33	100	33	125	MHz
SysClock Period	t_{SCP}	11.1	30	10	30	8	30	ns
SysClock Rise Time[1]	t_{SCRise}	—	2.5	—	2	—	2	ns
SysClock Fall Time[1]	t_{SCFall}	—	2.5	—	2	—	2	ns
ModeClock Period	$t_{ModeCKP}$	—	256 t_{SCP}	—	256 t_{SCP}	—	256 t_{SCP}	ns

1. Rise and Fall times are measured between 10% and 90%

Capacitive Load Deration—RC5000

Parameter	Symbol	Test Conditions	180MHz		200MHz		250MHz		Units
			Min	Max	Min	Max	Min	Max	
Load Derate	C_{LD}	—	—	2	—	2	—	2	ns/25pF

System Interface Parameters—RC5000

Note: 50 pf loading on external output signals

Parameter	Symbol	Test Conditions	180 MHz pipeline / 90 MHz Bus Frequency		200 MHz pipeline / 100MHz Bus Frequency		250MHz pipeline / 125 MHz Bus Frequency		Units
			Min	Max	Min	Max	Min	Max	
Data Output	t_{DO} = Max t_{DM} = Min	$mode_{14..13}$ = 10 (fastest, 100%)	0[1]	7	0[1]	5	0[1]	4.7	ns
		$mode_{14..13}$ = 11 (83%)	0[1]	8	0[1]	7	0[1]	5	ns
		$mode_{14..13}$ = 00 (67%)	0[1]	9	0[1]	9	0[1]	6	ns
		$mode_{14..13}$ = 01 (slowest, 50%)	0[1]	11	0[1]	11	0[1]	7	ns
Data Output Hold	t_{DOH}[1]	$mode_{14..13}$ = 10 (fastest)	0	—	0	—	0	—	ns
		$mode_{14..13}$ = 11 (83%)	0	—	0	—	0	—	ns
		$mode_{14..13}$ = 00 (67%)	0	—	0	—	0	—	ns
		$mode_{14..13}$ = 01 (slowest)	0	—	0	—	0	—	ns
Data Input	t_{DS}	t_{rise} = 3ns t_{fall} = 3ns	1.5	—	1.5	—	1.5	—	ns
	t_{DH}		0.5	—	0.5	—	0.5	—	ns

1. Guaranteed by design.

Boot Time Interface Parameters—RC5000

Parameter	Symbol	Test Conditions	180MHz / 90 MHz		200MHz / 100 MHz		250MHz / 125 MHz		Units	Conditions
			Min	Max	Min	Max	Min	Max		
Mode Data Setup	t_{DS}	—	4	—	4	—	4	—	ns	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	ns	Master Clock Cycle

DC Electrical Characteristics

(V_{cc} = 3.3V± 5%; T_{case} = 0°C to +85°C for commercial or T_{case} = -40°C to +85°C for industrial)

Parameter	180MHz		200MHz		250MHZ		Conditions
	Min	Max	Min	Max	Min	Max	
VOL	—	0.1V	—	0.1V	—	0.1V	|IOUT|= 20uA
VOH	VCC - 0.1V	—	VCC - 0.1V	—	VCC - 0.1V	—	
VOL	—	0.4V	—	0.4V	—	0.4V	|IOUT|= 4mA
VOH	2.4V	—	2.4V	—	2.4V	—	
VIL	–0.5V	0.2VCC	–0.5V	0.2VCC	–0.5V	0.2VCC	—
VIH	0.7VCC	VCC + 0.5V	0.7VCC	VCC + 0.5V	0.7VCC	VCC + 0.5V	—
IIN	—	±10uA	—	±10uA	—	±10uA	0 ≤ VIN ≤ VCC
CIN	—	10pF	—	10pF	—	10pF	—
CIO	—	10pF	—	10pF	—	10pF	—
Cclk	—	10pF	—	10pF	—	10pF	
I/OLEAK	—	20uA	—	20uA	—	20uA	Input/Output Leakage

Power Consumption—RC5000

Parameter		180MHz Max	200MHz Max	250MHz Max	Conditions
System Condition		180/45MHz	200/50MHz	250/62.5MHz	—
I_{cc}	Standby	120mA	120mA	120mA	C_L = 50 pF
	Active	1100mA	1300mA	1800mA	C_L = 50pF Pipelined writes or write re-issue T_c = 25°C

Physical Specifications

The RC5000 is available in two packages, the 223-pin CPGA and the 272-ball SBGA. The 223-pin CPGA package is shown in Figure 2 and Table 3; information on the SBGA package is shown in Figure 3 and Table 4.

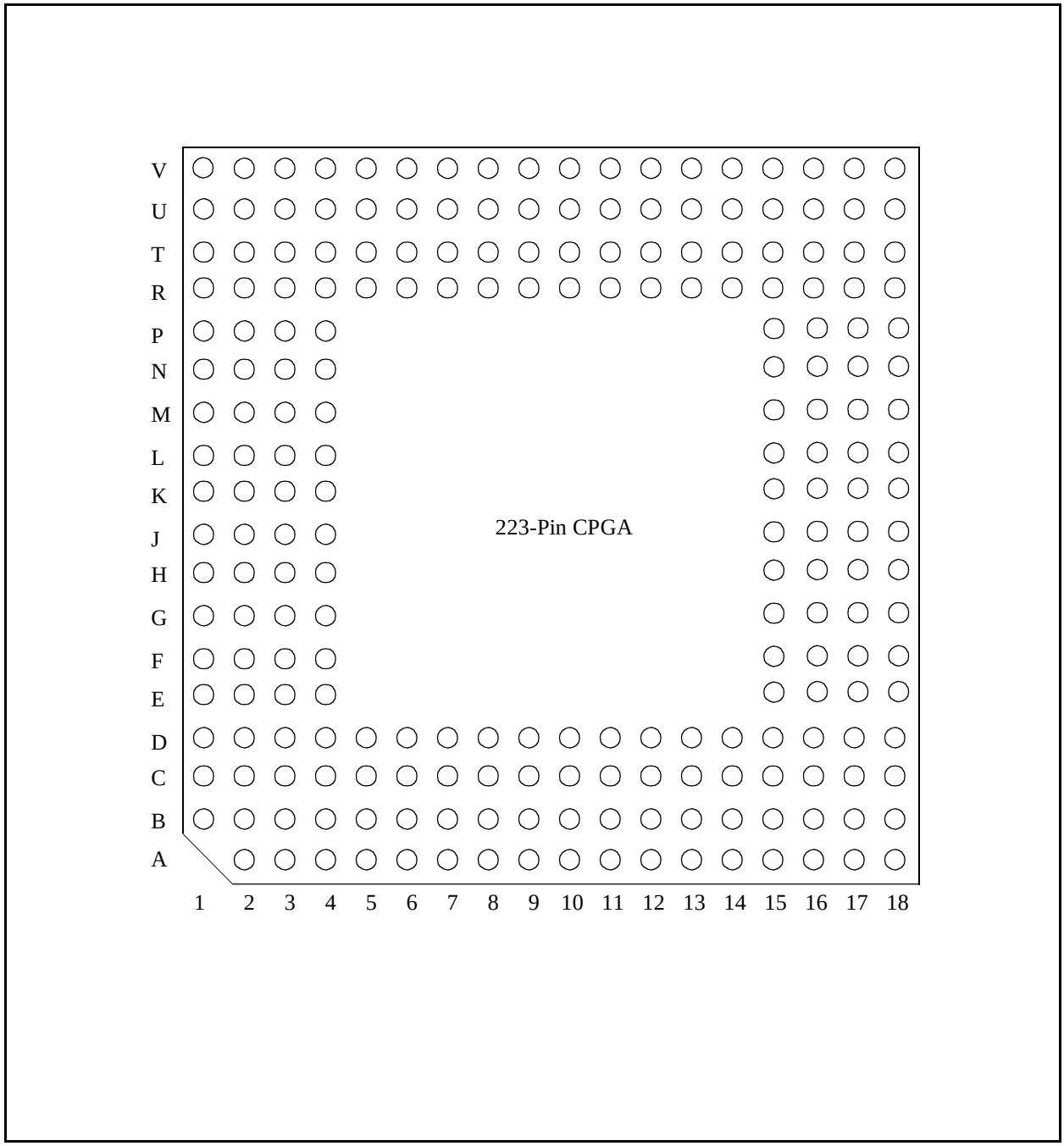


Figure 3 RC5000 223-pin CPGA Pin Orientation (Bottom View)

223-Pin CPGA Pinout

Pin #	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	Vcc	C5	SysADC[6]	E18	Vcc	K17	VssP	R6	SysAD[51]	U9	SysAD[63]
A3	Vss	C6	SysAD[16]	F1	Vcc	K18	Vss	R7	SysAD[55]	U10	SysAD[13]
A4	Vcc	C7	SysAD[50]	F2	Reserved	L1	Vss	R8	SysAD[27]	U11	SysAD[11]
A5	Vss	C8	SysAD[22]	F3	ScValid	L2	SysCmd[8]	R9	SysAD[31]	U12	SysAD[9]
A6	Vss	C9	SysAD[24]	F4	INT[1]*	L3	SysCmd[7]	R10	SysAD[43]	U13	SysAD[37]
A7	Vcc	C10	SysAD[28]	F15	ScDCE[0]*	L4	SysCmd[5]	R11	SysAD[39]	U14	SysAD[3]
A8	Vss	C11	SysAD[62]	F16	ScCWE[0]*	L15	ScLine[12]	R12	SysAD[35]	U15	ScWord[0]
A9	Vcc	C12	SysAD[44]	F17	ScTDE*	L16	ScLine[14]	R13	SysAD[1]	U16	Vcc
A10	Vss	C13	SysAD[10]	F18	Vss	L17	ScLine[15]	R14	ScWord[1]	U17	Vss
A11	Vcc	C14	SysAD[38]	G1	Vss	L18	Vcc	R15	ScLine[0]	U18	Vss
A12	Vss	C15	SysAD[4]	G2	Reserved	M1	Vcc	R16	ScLine[3]	V1	Vss
A13	Vcc	C16	SysAD[34]	G3	Reserved	M2	SysCmd[6]	R17	ScLine[6]	V2	Vss
A14	Vss	C17	SysAD[2]	G4	Reserved	M3	SysCmd[4]	R18	Vss	V3	Vcc
A15	Vss	C18	Vss	G15	ScCLR*	M4	SysCmd[1]	T1	Vss	V4	Vss
A16	Vcc	D1	Vss	G16	ScTCE*	M15	ScLine[8]	T2	SysAD[15]	V5	Vss
A17	Vss	D2I	INT3*	G17	ModeIn	M16	ScLine[10]	T3	SysAD[47]	V6	Vcc
A18	Vss	D3	INT5*	G18	Vcc	M17	ScLine[13]	T4	SysAD[17]	V7	Vss
B1	Vss	D4	Release*	H1	Vcc	M18	Vss	T5	SysAD[19]	V8	Vcc
B2	Vss	D5	Vcc	H2	Reserved	N1	Vss	T6	SysAD[23]	V9	Vss
B3	Vcc	D6	SysADC[2]	H3	Reserved	N2	SysCmd[3]	T7	SysAD[57]	V10	Vcc
B4	SysADC[4]	D7	SysAD[48]	H4	Reserved	N3	SysCmd[2]	T8	SysAD[29]	V11	Vss
B5	SysADC[0]	D8	SysAD[52]	H15	VccOK	N4	SysADC[7]	T9	Vcc	V12	Vcc
B6]	SysAD[18	D9	SysAD[56]	H16	ModeClock	N15	ScLine[5]	T10	SysAD[45]	V13	Vss
B7]	SysAD[20]	D10	SysAD[60]	H17	SysClock	N16	ScLine[7]	T11	SysAD[41]	V14	Vcc
B8	SysAD[54]	D11	SysAD[14]	H18	Vss	N17	ScLine[11]	T12	SysAD[7]	V15	Vss
B9	SysAD[26]	D12S	SysAD[42]	J1	Vss	N18	Vcc	T13	SysAD[5]	V16	Vss
B10	0SysAD[58]	D13	SysAD[8]	J2	WrRdy*	P1	Vcc	T14	SysAD[33]	V17	Vcc
B11	SysAD[30]	D14	SysAD[36]	J3	ValidIn*	P2	SysCmd[0]	T15	Reset*	V18	Vss
B12	SysAD[46]	D15	ColdReset*	J4	ExtReq*	P3	SysCmdP	T16	ScLine[1]		
B13	SysAD[12]	D16	SysAD[0]	J15	JTDO	P4	SysADC[1]	T17	Vcc		
B14	SysAD[40]	D17	ScTOE*	J16	JTDI	P15	ScLine[2]	T18	Vcc		
B15	SysAD[6]	D18	Vcc	J17	JTCK	P16	ScLine[4]	U1	Vcc		
B16	Vss	E1	Vss	J18	Vcc	P17	ScLine[9]	U2	Vcc		
B17	Vcc	E2	INT[0]*	K1	Vcc	P18	Vss	U3	Vss		
B18	Vcc	E3	INT[2]*	K2	ScMatch	R1	Vcc	U4	SysAD[21]		
C1	Vcc	E4	NT[4]*	K3	RdRdy*	R2	SysADC[5]	U5	SysAD[53]		
C2	Vcc	E15	SysAD[32]	K4S	cDOE*	R3	SysADC[3]	U6	SysAD[25]		
C3	ValidOut*	E16	ScDCE[1]*	K15	JTMS	R4	BigEndian	U7	SysAD[59]		
C4	NMI*	E17	ScCWE[1]*	K16	VccP	R5	SysAD[49]	U8	SysAD[61]		

272-Ball SBGA Package

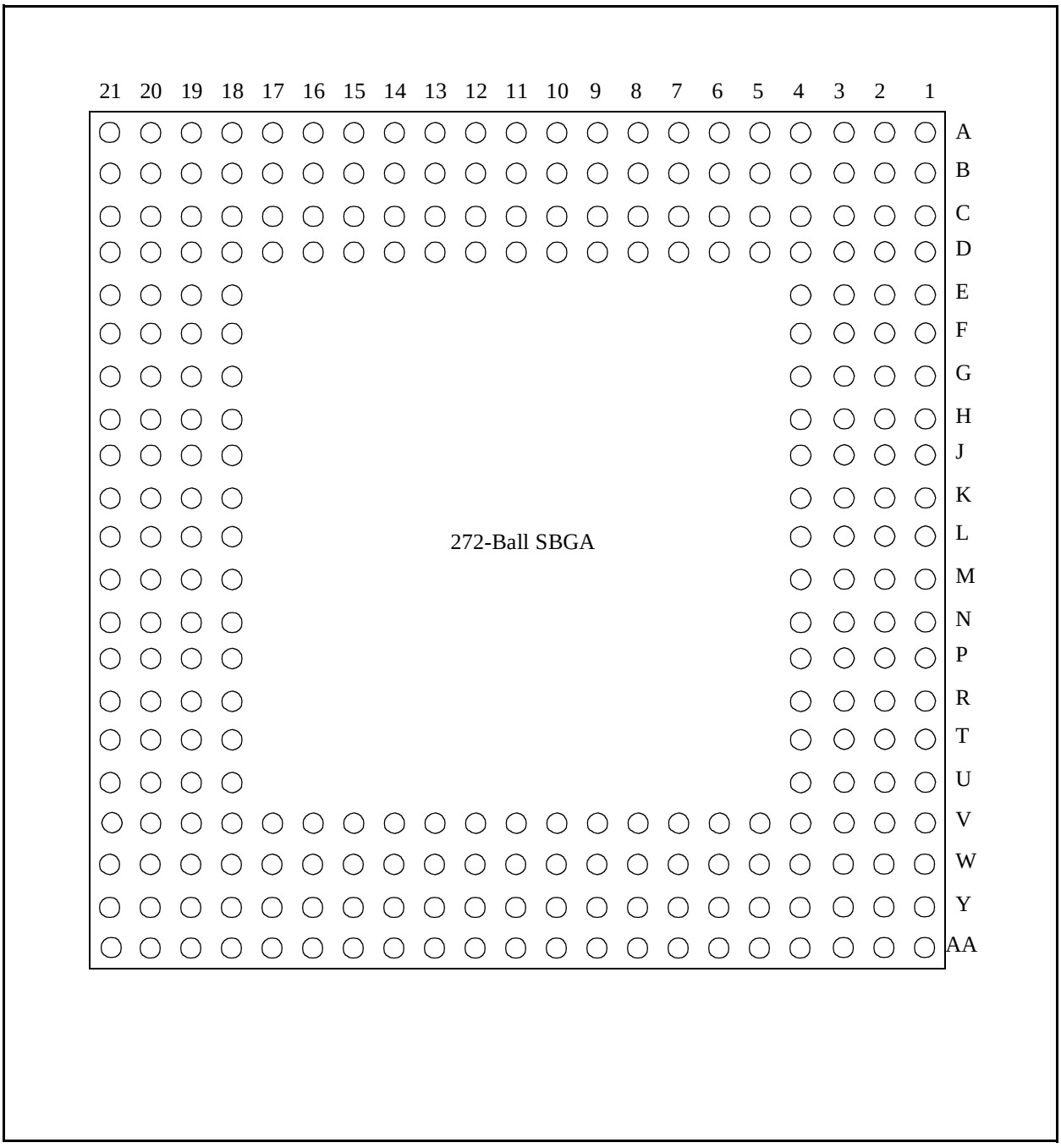
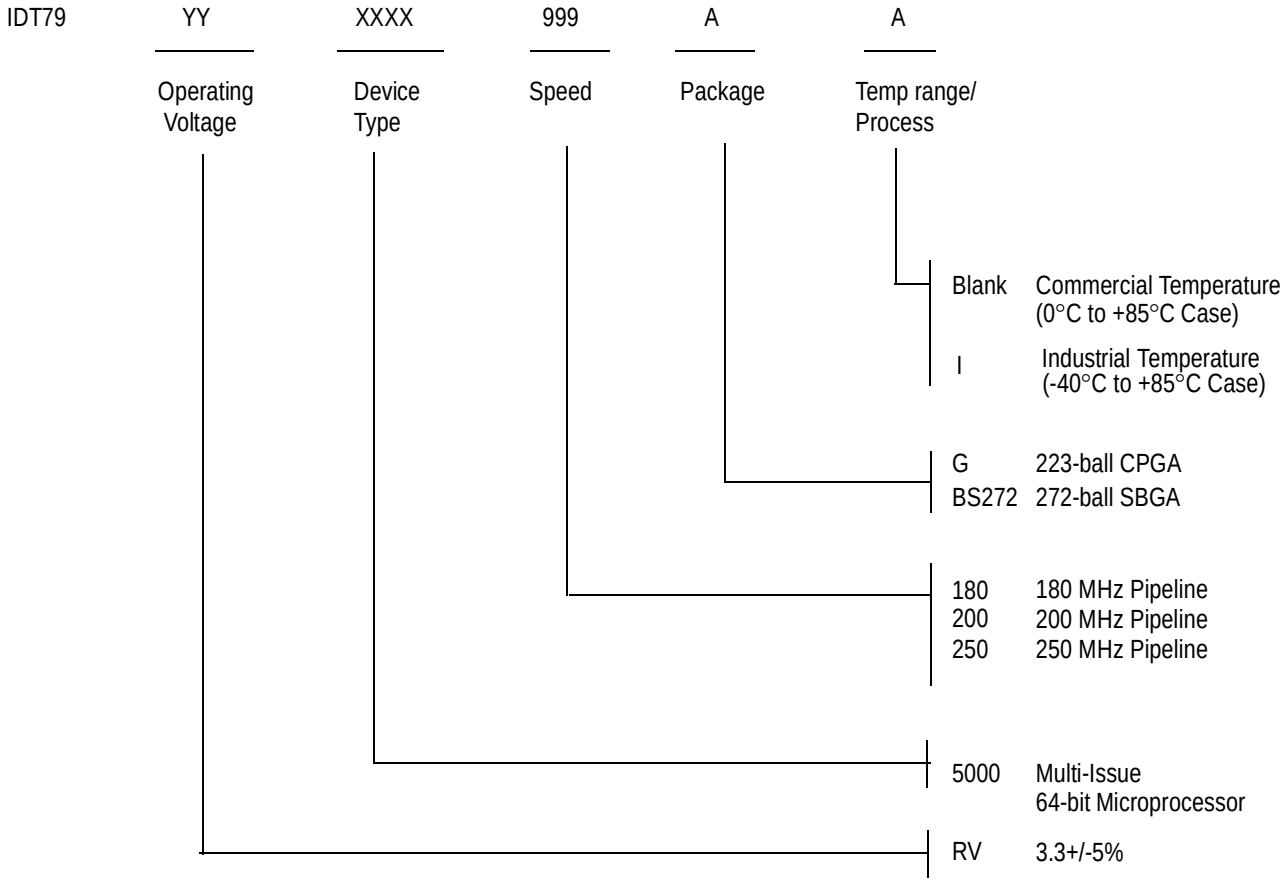


Figure 4 Ball Grid Array Package (Bottom View)

272-Ball SBGA Pinout

Pkg Pin	Function	Pkg Pin	Function	Pkg Pin	Function	Pkg Pin	Function	Pkg Pin	Function	Pkg Pin	Function
AA1	Vss	B5	SysAD0	D9	Vss	J2	SysAD46	P21	SysAD55	W1	Vss
AA2	Vcc	B6	ScTOE*	D10	Vcc	J3	SysAD14	R1	Vss	W2	Vcc
AA3	Vss	B7	ScCLR*	D11	Vccp	J4	Vss	R2	SysAD18	W3	Vcc
AA4	ValidOut*	B8	ScTDE*	D12	Vcc	J18	Vss	R3	SysAD48	W4	Vcc
AA5	Vss	B9	ModeClock	D13	Vss	J19	SysAD9	R4	Vcc	W5	Int*5
AA6	Int*0	B10	JTDI	D14	Vcc	J20	SysAD41	R18	Vcc	W6	Int*4
AA7	Vss	B11	JTCK	D15	Vcc	J21	Vss	R19	SysAD53	W7	Int*1
AA8	Reserved	B12	N/C	D16	Vss	K1	SysAD60	R20	SysAD23	W8	Reserved
AA9	Vss	B13	ScLine14	D17	Vcc	K2	SysAD30	R21	Vss	W9	Reserved
AA10	WrRdy*	B14	ScLine10	D18	Vss	K3	SysAD62	T1	SysAD16	W10	Reserved
AA11	Vss	B15	ScLine9	D19	Vcc	K4	Vcc	T2	SysADC0	W11	ValidIn*
AA12	ScMatch	B16	ScLine6	D20	Vcc	K18	Vcc	T3	SysADC2	W12	ScDOE*
AA13	Vss	B17	ScLine3	D21	Vcc	K19	SysAD11	T4	Vss	W13	SysCmd7
AA14	SysCmd6	B18	ScLine1	E1	Vss	K20	SysAD43	T18	Vss	W14	SysCmd4
AA15	Vss	B19	Vcc	E2	SysAD36	K21	SysAD13	T19	SysAD19	W15	SysCmd1
AA16	SysCmd2	B20	Vcc	E3	SysAD4	L1	Vss	T20	SysAD51	W16	SysADC7
AA17	Vss	B21	Vcc	E4	Vcc	L2	SysAD58	T21	SysAD21	W17	SysADC5
AA18	SysADC3	C1	Vss	E18	Vcc	L3	SysAD28	U1	Vss	W18	SysAD47
AA19	Vss	C2	Vcc	E19	ScWord1	L4	Vcc	U2	SysADC4	W19	BigEndian
AA20	Vcc	C3	ColdReset*	E20	ScWord0	L18	Vcc	U3	SysADC6	W20	Vcc
AA21	Vss	C4	SysAD34	E21	Vss	L19	SysAD45	U4	Vcc	W21	Vss
A1	Vss	C5	ScDCE*1	F1	SysAD8	L20	SysAD63	U18	Vcc	Y1	Vcc
A2	Vcc	C6	ScDCE*0	F2	SysAD38	L21	Vss	U19	SysAD17	Y2	Vcc
A3	Vss	C7	ScCWE*0	F3	SysAD6	M1	SysAD26	U20	SysAD49	Y3	Vcc
A4	SysAD32	C8	ScTCE*	F4	Vss	M2	SysAD56	U21	Vss	Y4	Release*
A5	Vss	C9	ModeIn	F18	Vss	M3	SysAD24	V1	Vcc	Y5	Int*3
A6	ScCWE*1	C10	JTDO	F19	SysAD1	M4	Vcc	V2	Vcc	Y6	Int*2
A7	Vss	C11	Vssp	F20	SysAD33	M18	Vcc	V3	Vcc	Y7	ScValid
A8	VCCOK	C12	JTMS	F21	SysAD3	M19	SysAD29	V4	Vss	Y8	Reserved
A9	Vss	C13	ScLine13	G1	Vss	M20	SysAd61	V5	NMI*	Y9	Reserved
A10	MasterClk	C14	ScLine11	G2	SysAD10	M21	SysAD31	V6	Vss	Y10	Reserved
A11	Vss	C15	ScLine8	G3	SysAD40	N1	Vss	V7	Vcc	Y11	ExtRqst*
A12	ScLine15	C16	ScLine5	G4	Vcc	N2	SysAD54	V8	Vcc	Y12	RdRdy*
A13	Vss	C17	ScLine4	G18	Vcc	N3	SysAD22	V9	Vss	Y13	SysCmd8
A14	ScLine12	C18	ScLine0	G19	SysAD35	N4	Vss	V10	Vcc	Y14	SysCmd5
A15	Vss	C19	Reset*	G20	SysAD5	N18	Vss	V11	Vcc	Y15	SysCmd3
A16	ScLine7	C20	Vcc	G21	Vss	N19	SysAD27	V12	Vcc	Y16	SysCmd0
A17	Vss	C21	Vss	H1	SysAD42	N20	SysAD59	V13	Vss	Y17	SysCmdP
A18	ScLine2	D1	Vcc	H2	SysAD44	N21	Vss	V14	Vcc	Y18	SysADC1
A19	Vss	D2	Vcc	H3	SysAD12	P1	SysAD50	V15	Vcc	Y19	SysAD15
A20	Vcc	D3	Vcc	H4	Vcc	P2	SysAD52	V16	Vss	Y20	Vcc
A21	Vss	D4	Vss	H18	Vcc	P3	SysAD20	V17	Vcc	Y21	Vcc
B1	Vcc	D5	Vcc	H19	SysAD7	P4	Vcc	V18	Vss		
B2	Vcc	D6	Vss	H20	SysAD39	P18	Vcc	V19	Vcc		
B3	Vcc	D7	Vcc	H21	SysAD37	P19	SysAD25	V20	Vcc		
B4	SysAD2	D8	Vcc	J1	Vss	P20	SysAD57	V21	Vcc		

Ordering Information



Valid Combinations

IDT79RV5000 - 180, 200MHz	G	CPGA package
IDT79RV5000 - 180, 200, 250MHz	BS272	SBGA package
IDT79RV5000 - 180, 200MHz	BS272 I	SBGA package

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-330-1748
www.idt.com

for Tech Support:
email: rischelp@idt.com
phone: 408-492-8208

The IDT logo is a registered trademark of Integrated Device Technology, Inc.