Si47xx Antenna, Schematic, Layout, and Design Guidelines

1. Introduction

This document provides general Si47xx design guidelines and AM/FM/SW/LW/WB antenna selections which includes schematic, BOM, layout and design checklist.

All users should follow the Si47xx design guidelines presented in Section 2 and then users can proceed to the appropriate antenna selections according to the application and device used presented in Sections 3 through 10.

To get an in-depth knowledge about each individual antenna, the antenna theory and interface model is presented in the Appendices.

Table 1. Supported Devices and Antennas

Part Number	General Description	Function					FM Antenna			WB Antenna	AM/LW Antenna		SW Antenna
		FM Transmitter	FM Receiver	AM Receiver	SW/LW Receiver	WB Receiver	Headphone	Embedded	Cable	Whip	Ferrite Loop	Air Loop	Whip
Si4700	FM Receiver		✓				✓						
Si4701	FM Receiver with RDS		✓				✓						
Si4702	FM Receiver		✓				✓						
Si4703	FM Receiver with RDS		✓				✓						
Si4704	FM Receiver		✓				✓	✓	✓				
Si4705	FM Receiver with RDS		✓				✓	✓	✓				
Si4706	High Performance RDS Receiver		✓				✓	✓	✓				
Si4707	WB Receiver with SAME					✓				✓			
Si4710	FM Transmitter	✓						✓	✓				
Si4711	FM Transmitter with RDS	✓						✓	✓				
Si4712	FM Transmitter with RPS	✓						✓	✓				
Si4713	FM Transmitter with RDS & RPS	✓						✓	✓				
Si4720	FM Transceiver	✓	✓				✓	✓	✓				
Si4721	FM Transceiver with RDS	✓	✓				✓	✓	✓				
Si4730	AM/FM Receiver		✓	✓			✓				✓	✓	
Si4731	AM/FM Receiver with RDS		✓	✓			✓				✓	✓	
Si4734	AM/SW/LW/FM Receiver		✓	✓	✓		✓				✓	✓	✓
Si4735	AM/SW/LW/FM Receiver with RDS		✓	✓	✓		✓				✓	✓	✓
Si4736	AM/FM/WB Receiver		✓	✓		✓	✓			✓	✓	✓	
Si4737	AM/FM/WB Receiver with RDS		✓	✓		✓	✓			✓	✓	✓	
Si4738	FM/WB Receiver		✓			✓	✓			✓			
Si4739	FM/WB Receiver with RDS		✓			✓	✓			✓			
Si4784	FM Receiver		✓				✓		✓				
Si4785	FM Receiver with RDS		✓				✓		✓				

Copyright © 2014 by Silicon Laboratories

TABLE OF CONTENTS

Section **Page**

1. Introduction 1
2. Si47xx 3x3 mm QFN Schematic and Layout 5
2.1. Si47xx 3x3 mm Design 5
2.2. Emissions Mitigation Components 7
2.3. Si47xx 3x3 mm Schematic 9
2.4. Si47xx 3x3 mm Bill of Materials 10
2.5. Si47xx 3x3 mm Layout 12
2.6. Si47xx 3x3 mm Design Checklist 16
3. Headphone Antenna for FM Receiver on FMI (Si470x/2x/3x/8x Only) 18
3.1. Headphone Antenna Design 18
3.2. Headphone Antenna Schematic 19
3.3. Headphone Antenna Bill of Materials 20
3.4. Headphone Antenna Layout 21
3.5. Headphone Antenna Design Checklist 21
4. Cable Antenna for FM Receive on FMI (Si470x/2x/3x/8x Only) 22
4.1. Cable Antenna Design 22
4.2. Cable Antenna Schematic 22
4.3. Cable Antenna Bill of Materials 23
4.4. Cable Antenna Layout 24
4.5. Cable Antenna Design Checklist 24
5. Embedded Antenna for FM Transmit on TXO and Receive on LPI (Si4704/05/06/1x/2x Only) 25
5.1. Embedded Antenna Design 25
5.2. Embedded Antenna Schematic 31
5.3. Embedded Antenna Bill of Materials 32
5.4. Embedded Antenna Layout 33
5.5. Embedded Antenna Design Checklist 33
6. Cable Antenna for FM Transmit on TXO and Receive on LPI (Si4704/05/06/1x/2x Only) 34
6.1. Cable Antenna Design 34
6.2. Cable Antenna Schematic 34
6.3. Cable Antenna Bill of Materials 35
6.4. Cable Antenna Layout 36
6.5. Cable Antenna Design Checklist 36
7. Whip Antenna for FM/WB Receiver on FMI (Si4707/3x Only) 37
7.1. FM/WB Whip Antenna Design 37
7.2. FM/WB Whip Antenna Schematic 37
7.3. FM/WB Whip Antenna Bill of Materials 38
7.4. FM/WB Whip Antenna Layout 38
7.5. FM/WB Whip Antenna Design Checklist 38
8. Ferrite Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only) 39

8.1. Ferrite Loop Antenna Design 39
8.2. Ferrite Loop Antenna Schematic 40
8.3. Ferrite Loop Antenna Bill of Materials 40
8.4. Ferrite Loop Antenna Layout 41
8.5. Ferrite Loop Antenna Design Checklist 41
9. Air Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only) 42
9.1. Air Loop Antenna Design 42
9.2. Air Loop Antenna Schematic 43
9.3. Air Loop Antenna Bill of Materials 44
9.4. Air Loop Antenna Layout 44
9.5. Air Loop Antenna Design Checklist 44
10. Whip Antenna for SW Receive on AMI (Si4734/35 Only) 45
10.1. SW Whip Antenna Design 45
10.2. SW Whip Antenna Schematic 46
10.3. SW Whip Antenna Bill of Materials 48
10.4. SW Whip Antenna Layout 49
10.5. SW Whip Antenna Design Checklist 49
Appendix A—FM Receive Headphone Antenna Interface Model 50
Appendix B—FM Transmit Embedded Antenna Interface Model 55
Appendix C—AM Ferrite Loop Stick Antenna Interface Model 63
Document Change List 67
Contact Information 69

2. Si47xx 3x3 mm QFN Schematic and Layout

This section shows the minimal schematic and layout options required for optimal Si47xx performance. Population options are provided to support a single layout for all 3 x 3 mm QFN devices, mitigate system noise, operate the internal oscillator with an external crystal, and filter VCO energy.

2.1. Si47xx 3x3 mm Design

C1 (22 nF) is a required bypass capacitor for VD/VDD supply pin 11. Place C1 as close as possible to the VD/VDD pin 11 and GND pin 12. Place a via connecting C1 VD/VDD supply to the power rail such that the cap is closer to the Si47xx than the via. Route C1 GND directly and only to GND pin 12 with a wide, low inductance trace. C1 GND should not be routed to GND via. These recommendations are made to reduce the size of the current loop created by the bypass cap and routing, minimize bypass cap impedance and return all currents to the GND pad.

Note: For Si47xx rev D parts, C1 is required on pin 11 (VA). The C1 design guidelines described above should be followed. For an illustration of these guidelines, refer to Figure 3.

C2 (22 nF) is an optional bypass capacitor for VA/LIN/DFS supply pin 16 (Si4702/03 only) and may be placed to mitigate supply noise. Place C2 as close as possible to the VA/LIN/DFS pin 16 and GND pin 15. Place a via connecting C2 VA supply to the power rail such that the cap is closer to the Si47xx than the via. Route C2 GND directly and only to GND pin 15 with a wide, low inductance trace. Route GND/RIN/DOUT pin 15 to the GND pad if designing only for the Si4702/03. If designing for all Si47xx devices, do not route GND/RIN/DOUT pin 15 to the GND pad. In this case the on-chip connection between pin 15 and the GND pad will provide a ground connection. These recommendations are made to reduce the size of the current loop created by the bypass cap and routing, minimize bypass cap impedance and return all currents to the GND pad.

C3 (100 nF) is an optional bypass capacitor for the VIO supply pin 10 and may be placed to mitigate supply noise. Place C3 as close as possible to the VIO pin 10 and the GND pin 12. Place a via connecting C3 VIO supply to the power rail such that the cap is closer to the Si47xx than the via. Route C3 GND directly and only to GND pin 12 with a wide, low inductance trace. C3 GND should not be routed to GND via. These recommendations are made to reduce the size of the current loop created by the bypass cap and routing, minimize bypass cap impedance and return all currents to the GND pad.

Note: For Si47xx rev D parts, C3 is required on pin 10 (VD). The C3 design guidelines described above should be followed.

C6 and C7 (0.39µF) are ac coupling caps for transmitter audio input to VA/LIN/DFS pin 16 and GND/RIN/DOUT pin 15 (Si471x/2x analog audio input mode only). The input resistance of the transmitter audio input and the cap will set the high pass pole given by Equation 1. The input resistance of the audio input is programmatically selectable as 396 kΩ, 100 kΩ, 74 kΩ, or 60 kΩ (default). Placement location is not critical.

$$f_c = \frac{1}{2\pi RC}$$

Equation 1. High-Pass Pole Calculation

C8 and C9 (0.39 µF.) are ac coupling caps for receiver analog audio output from ROUT/DIN pin 13 and LOUT/DFS pin 14 (Si470x/2x/3x/8x audio output mode only). The input resistance of the amplifier, such as a headphone amplifier, and the capacitor will determine the high pass pole given by Equation 1. Placement location is not critical.

C10 and C11 (7–22 pF) are optional crystal loading caps required only when using the internal oscillator feature. Refer to the crystal data sheet for the proper load capacitance and be certain to account for parasitic capacitance. Place caps C10 and C11 such that they share a common GND connection and the current loop area of the crystal and loading caps is minimized.

C12 and C13 (2.2 pF) are noise mitigation caps if digital audio option is in use. The caps need to be placed close to the Si47xx chip.

X1 (32.768 kHz) is an optional crystal required only when using the internal oscillator feature. Place the crystal X1 as close to GPO3/DCLK pin 17 and RCLK pin 9 as possible to minimize current loops. Route the RCLK trace as far from SDIO pin 8 and SDIO trace as possible to minimize capacitive coupling.

R1 (0 Ω) is an optional jumper used to route the digital audio clock to GPO3/DCLK pin 17. R1 is only required for a universal design which accommodates BOM population options selecting between crystal and digital audio (Si4705/06/1x/2x/31/35/37/39/8x only).

Note: Crystal and digital audio mode cannot be used at the same time. Populate R1 and remove C10, C11, and X1 when using digital audio.

Populate C10, C11, and X1 and remove R1 when using the internal oscillator. Place resistor R1 as close to DCLK/GPO3 pin 17 as possible as shown in Layout Example 4 to minimize trace length from pin 17 to the crystal and load cap.

R2-R6 (25 Ω–2 kΩ) are optional series termination resistors and are used to mitigate system noise. The recommended value of the resistors is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place the series termination resistors R2-R6 as close to the host controller as possible.

R7 and R8 (4.7 kΩ) are optional pull-up resistors for the SCLK and SDIO lines required only when using an I^2C bus. The size of pull-up resistor value will vary based on the number of devices, capacitance and speed of the bus. Placement location is not critical. Refer to the I^2C specification for additional design information.

R9 (0 Ω) is used to route power to VA/LIN/DFS supply pin 16. R9 is only required to support a layout for all 3x3 mm QFN devices. If designing for the Si4702/03 only R9 may be replaced with trace connections. If designing for Si4704/05/06/07/1x/2x/3x/8x only, R9 is not required. Place resistor R9 as close to VA/LIN/DFS pin 16 as possible. R10 (0 Ω) is an optional jumper used to route the VA pin 16 for Si4702/03. R10 is only required for a universal design which supports BOM options for the Si4702/03 and other Si47xx devices. R10 should be populated when using an Si4702/03 and not populated when using an alternate device.

R11 (0 Ω) is an optional jumper used to route the DFS to VA/LIN/DFS pin 16. R11 is only required for a design in which the Si4702/03 and digital audio output (Si4705/06/21/31/35/37/39/8x) BOM options are desired. Place resistor R11 as close to pin VA/LIN/DFS 16 as possible.

R12 (25 Ω–2 kΩ) is a required series termination resistor when using digital audio output (Si4705/06/21/31/35/37/39/8x) and is used to mitigate noise from the digital data routed from GND/RIN/DOUT pin 15. The recommended value of the resistor is 604 Ω for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place R12 as close to pin 15 as possible.

R13 (25 Ω–2 kΩ) is a required series termination resistor when using digital audio (Si4705/06/1x/2x/31/35/37/39/8x only) and is used to mitigate noise from the digital clock routed to GPO3/DCLK pin 17. The recommended value of the resistor is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place R13 as close to the host controller as possible.

R14 (25 Ω–2 kΩ) is a required series termination resistor when using digital audio output (Si4705/06/21/31/35/37/39/8x) and is used to mitigate noise from the digital frame clock routed to VA/LIN/DFS pin 16. The recommended value of the resistor is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place R14 as close to the host controller as possible.

R15 (25 Ω–2 kΩ) is a required series termination resistor when using digital audio input (Si471x/2x only) and is used to mitigate noise from the digital frame clock routed to LOUT/DFS pin 14. The recommended value of the resistor is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place R15 as close to the host controller as possible.

R16 (25 Ω–2 kΩ) is a required series termination resistor when using digital audio input (Si471x/2x only) and is used to mitigate noise from the digital data routed to ROUT/DIN pin 13. The recommended value of the resistors is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place R16 as close to the host controller as possible.

R17 (0 Ω) is an optional jumper used to route the GND pin 15 for Si4702/03. R17 is only required for a universal design which supports BOM options for the Si4702/03 and other Si47xx devices. R17 should be populated when using an Si4702/03 and not populated when using an alternate device. Place R17 as close to the Si47xx as possible.

R18 (0 Ω) is an optional jumper used to route the GND pin 4 for Si4702/03. R18 is only required for a universal design which supports BOM options for the Si4702/03 and other Si47xx devices. R18 should be populated when using an Si4702/03 and not populated when using an alternate device. Place R18 as close to the Si47xx as possible.

2.2. Emissions Mitigation Components

The following components may be placed to reduce VCO emissions. This is only required if regulatory testing requires measuring emissions at the VCO frequency of 3–4 GHz. Refer to Section “2.6.1. Emissions Mitigation Checklist” for detailed layout and grounding recommendations pertaining to the components described below.

2.2.1. FMI Mitigation Components

Table 2. FMI Mitigation Components

Option	Components	Sensitivity	Mitigation	Cost
1	C5 = NP F1 = BLM15GA750SN1 C14 = 6 pF	Best	Best	Higher
2	C5 = 2.7 pF F1 = 20 nH C14 = 2.7 pF	Less (+1.75 dB vs Option1)	Good	Lower

C5 (NP) is an optional filter capacitor for FMI pin 2 and may be placed to shunt VCO energy to GND and prevent it from radiating from an antenna connected to the FMI pin. This pad is a placeholder for alternate emission mitigation option 2. While it is recommended to select option 1 for best sensitivity and mitigation performance, leaving this pad ensures that there is no redesign necessary between options. Route pin 2 to GND/RFGND if the pin functionality is not used.

F1 (BLM15GA750SN1) is an optional bead for FMI pin 2 and may be placed to prevent VCO energy from radiating from FMI pin. Place F1 as close as possible to FMI pin 2. Route pin 2 to GND/RFGND if the pin functionality is not used.

C14 (6 pF) is an optional filter capacitor for FMI pin 2 and may be placed to shunt VCO energy to GND and prevent it from radiating from an antenna connected to the FMI pin. Place C14 as close as possible to FMI pin 2. The ground path should be optimized on the top layer. Route pin 2 to GND/RFGND if the pin functionality is not used.

2.2.2. AMI Mitigation Components

Table 3. AMI Mitigation Components

Option	Components	Sensitivity	Mitigation	Cost
1	C17 = 3.3 pF L2 = 10 nH C16 = 3.3 pF	Best	Good	Lower
2	C17 = 2.7 pF L2 = 20 nH C16 = 2.7 pF	Less (+3 dB vs Option1)	Better	Lower
3	C17 = NP L2 = BLM15GA750SN1 C16 = NP	Least (+6 dB vs Option1)	Best	Higher

C17 (3.3 pF) is an optional filter capacitor for AMI pin 4 on Si473x devices and may be placed to shunt VCO energy to GND and prevent it from radiating from an antenna connected to the AMI pin. Place C17 as close as possible to AMI pin 4 and RFGND pin 3. The ground path should be optimized on the top layer. Route pin 4 to GND/RFGND if the pin functionality is not used.

L2 (10 nH) is an optional filter inductor for AMI pin 4 on Si473x devices and may be placed to prevent VCO energy from radiating from AMI pin. Place L2 as close as possible to AMI pin 4. Route pin 4 to GND/RFGND if the pin

functionality is not used.

C16 (3.3 pF) is an optional filter capacitor for AMI pin 4 on Si473x devices and may be placed to shunt VCO energy to GND and prevent it from radiating from an antenna connected to the AMI pin. Place C16 as close as possible to AMI pin 4 and RFGND pin 3. The ground path should be optimized on the top layer. Route pin 4 to GND/RFGND if the pin functionality is not used.

2.2.3. GPIO Mitigation Components

Table 4. GPIO Mitigation Components

Option	Components	Sensitivity	Mitigation	Cost
1	C15 = 33 pF R20 = 330 Ω C18 = 33 pF R19 = 330 Ω	Best	Best	Low
2	C15 = 33 pF R20 = 330 Ω C18 = NP R19 = 330 Ω	Best	Good	Low

C15 (33 pF) is an optional filter capacitor for GPO1 pin 19 and may be placed to shunt VCO energy to GND and prevent it from radiating. Place C15 as close as possible to GPO1 pin 19. The ground path should be optimized on the top layer.

R20 (330 Ω) is an optional mitigating resistor for GPO1 pin 19 and may be placed to prevent VCO energy from radiating from GPO1 pin. Place R20 as close as possible to GPO1 pin 19. R20 is not required if GPO1 is pulled up/down by design and has no other connections.

C18 (33 pF) is an optional filter capacitor for GPO2 pin 18 and may be placed to shunt VCO energy to GND and prevent it from radiating. Place C18 as close as possible to GPO2 pin 18. The ground path should be optimized on the top layer.

R19 (330 Ω) is an optional mitigating resistor for GPO2 pin 18 and may be placed to prevent VCO energy from radiating from GPO2 pin. Place R19 as close as possible to GPO2 pin 18. R19 is not required if GPO2 is pulled up/down by design and has no other connections.

2.2.4. LPI Mitigation Components

Table 5. LPI Mitigation Components

Option	Components	Sensitivity	Mitigation	Cost
1	C4 = 3.3 pF L1 = 15 nH	Best	Best	Low

C4 (3.3 pF) is an optional filter capacitor for TXO/LPI pin 4 on Si4704/05/06/1x/2x devices and may be placed to shunt VCO energy to GND and prevent it from radiating from an antenna connected to the TXO/LPI pin. Make measurements with different C4 and L1 values in-system to optimize the filter's performance for the antenna design chosen. Place C4 as close as possible to TXO/LPI pin 4 and RFGND pin 3. The ground path should be optimized on the top layer. Route pin 4 to GND/RFGND if the pin functionality is not used.

L1 (15 nH) is an optional filter inductor for TXO/LPI pin 4 on Si4704/05/06/1x/2x devices and may be placed to prevent VCO energy from radiating from an antenna connected to the TXO/LPI pin. Make measurements with different C4 and L1 values in-system to optimize the filter's performance for the antenna design chosen. Place L1 as close as possible to TXO/LPI pin 4. Route pin 4 to GND/RFGND if the pin functionality is not used.

2.3. Si47xx 3x3 mm Schematic

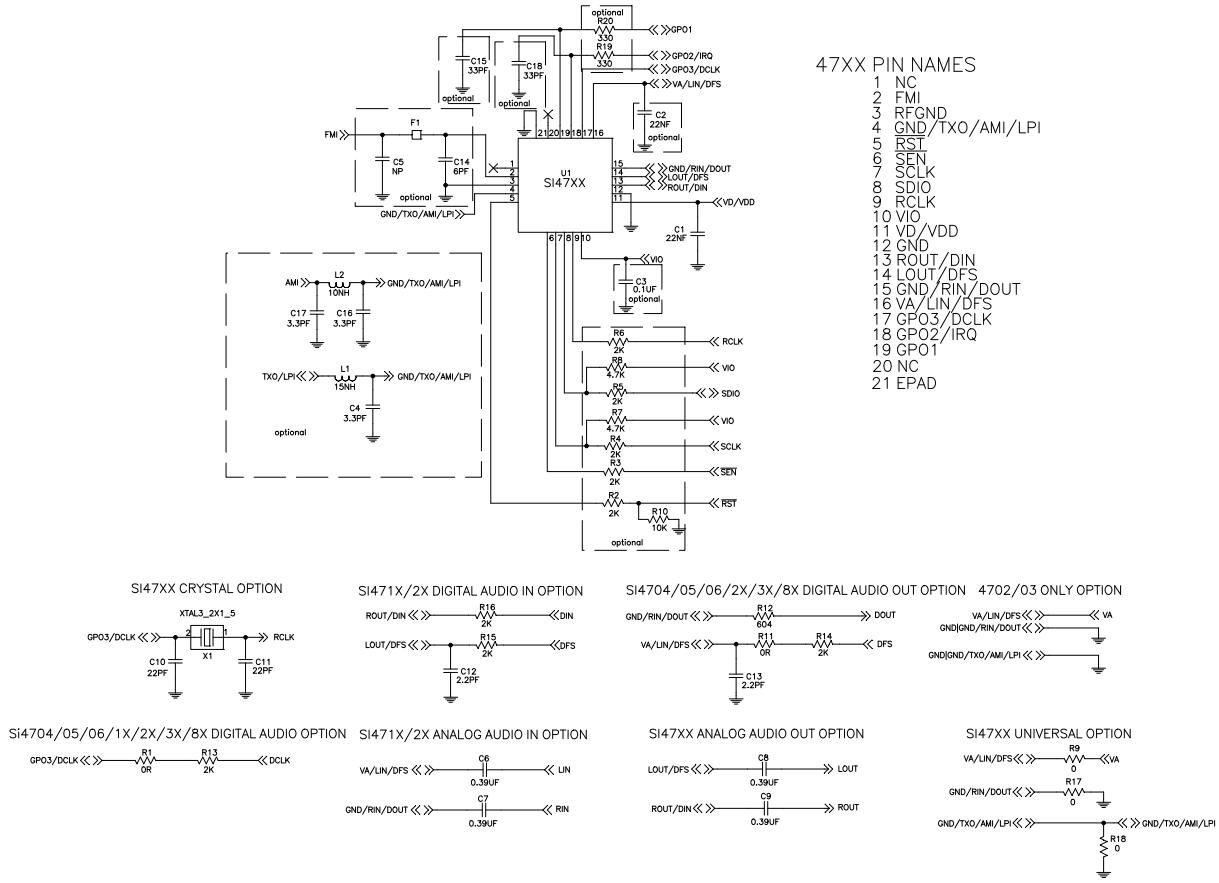


Figure 1. Si47xx 3x3 mm QFN Schematic

2.4. Si47xx 3x3 mm Bill of Materials

The required bill of materials for Figure 1 is shown in Table 6.

Table 6. Required Bill of Materials

Designator	Description	Note
C1	VD/VDD Supply bypass capacitor, 22 nF, 10%, Z5U/X7R	
C3	VI0 Supply bypass capacitor, 100 nF, 10%, Z5U/X7R	For supply noise mitigation. Optional for Si47xx rev C and earlier parts. For Si47xx rev D parts, C3 is required.
R12	DOUT current limiting resistor, 604 Ω	For digital audio output (Si4705/06/21/31/35/37/39/8x only)
R13	DCLK current limiting resistor, 25 Ω–2 kΩ	For digital audio (Si4705/06/1x/2x/31/35/37/39/8x only)
R14	DFS current limiting resistor, 25 Ω–2 kΩ	For digital audio output (Si4705/06/21/31/35/37/39/8x only)
R15	DFS current limiting resistor, 25 Ω–2 kΩ	For digital audio input (Si471x/2x only)
R16	DIN current limiting resistor, 25 Ω–2 kΩ	For digital audio input (Si471x/2x only)
U1	Silicon Laboratories Si47xx, 3x3 mm, 20 pin, QFN	

The optional bill of materials for Figure 1 is shown in Table 7.

Table 7. Optional Bill of Materials

Designator	Description	Note
C2	VA Supply bypass capacitor, 22 nF, 10%, Z5U/X7R	For supply noise mitigation (Si4702/03 only)
C6, C7	AC coupling capacitor, 0.39 µF, X7R/X5R	For analog audio input (Si471x/2x only)
C8, C9	AC coupling capacitor, 0.39 µF, X7R/X5R	For analog audio output
C10, C11	Crystal load capacitor, 22 pF, 5%, C0G	For internal oscillator option
C12, C13	Noise mitigation capacitor 2.2 pF, C0G	For DFS noise mitigation purpose
R2–R6	Current limiting resistor, 25–2 kΩ	For digital system noise mitigation
R7,R8	Pullup resistor, 4.7 kΩ	For I^2C bus mode communication
R1, R9, R10, R11, R17, R18	0 Ω jumper	For universal layout design supporting all Si47xx
X1	Crystal, Epson FC-135	For internal oscillator feature

Table 8. Optional Bill of Materials: Emissions Mitigation

Designator	Description	Note
C4	VCO filter capacitor 3.3 pF, 0402, C0G	For filtering of VCO energy (Si4704/05/06/1x/2x only)
C5	VCO filter capacitor NP, 0402, C0G	Placeholder pad for alternate FMI VCO filter configuration
C14	VCO filter capacitor 6 pF, 0402, C0G	For filtering of VCO energy
C15, C18	VCO filter capacitor 33 pF, 0402, C0G	For filtering of VCO energy
C16, C17	VCO filter capacitor 3.3 pF, 0402, C0G	For filtering of VCO energy (Si473x only)
F1	VCO filter bead Murata BLM15GA750SN1	For filtering of VCO energy
L1	VCO filter inductor 15 nH (Murata LQW18ANR15NJ00D)	For filtering of VCO energy (Si4704/05/06/1x/2x only)
L2	VCO filter inductor 10 nH (Murata LQW18AN10NJ00D)	For filtering of VCO energy (Si473x only)
R19, R20	VCO mitigating resistor, 330 Ω, 0402	For filtering of VCO energy

2.5. Si47xx 3x3 mm Layout

The following layout example selector guide provides guidance for selecting the proper example based on placement, routing, option, and device requirements. Layout examples 1, 2, and 3 show the critical component layout of the most common layout configurations. Layout example 4 shows a universal layout which supports all 3x3 mm QFN devices and features.

Table 9. Layout Example Selector Guide by Place and Route Requirements

Placement and Routing	Layout Example			
	1	2	3	4
Top Side Routing	X	X	X	X
Inner/Bottom Side Routing	X	X	X	X
Top Side Placement	X	X	X	X
Bottom Side Placement		X		X

Table 10. Layout Example Selector Guide by Option

Feature	Layout Example			
	1	2	3	4
Crystal	X	X		X
Analog Input			X	X
Analog Output	X	X	X	X
Digital Input			X	X
Digital Output			X	X

Table 11. Layout Example Selector Guide by Device

Device	Layout Example			
	1	2	3	4
Si4702/03	X	X		X
Si4704/05/06/07	X	X	X	X
Si471x			X	X
Si472x	X	X	X	X
Si473x	X	X	X	X
Si478x	X	X	X	X

The following layout rules are used:

- Layer 1 top side placement and routing (shown)
- Layer 2 GND (not shown)
- Power routed by trace (not shown)
- 0402 component size or larger
- 6 mil traces
- 6 mil trace spacing
- 15 mil component spacing

Figure 2 shows critical component layout with top side placement, top and bottom side routing, crystal and analog output support, and support for all devices except the Si471x transmitter family. The Si471x transmitter family can be supported in this example if VA bypass cap C2 is removed and audio input is routed to pin 15 and pin 16. Digital audio is not available when the crystal is used due to the multipurpose role of GPO3/DCLK pin 17. VIO bypass cap C3 is not included in this example in order to optimize routing of the crystal oscillator. Route the RCLK trace as far from the SDIO pin 8 and trace as possible by routing the SDIO trace on the bottom layer. If bottom side placement is possible, Figure 3 is preferred for optimal oscillator performance.

F1, C14, C15, C18, R19 and R20 are placed as close to the chip as possible. For the Si4704/05/06/2x with the short antenna option, pin 4 is populated with L1 and C4, C17 is not populated; for the Si473x AM receiver, C4 is replaced with C16, L1 is replaced with L2, and C17 is populated.

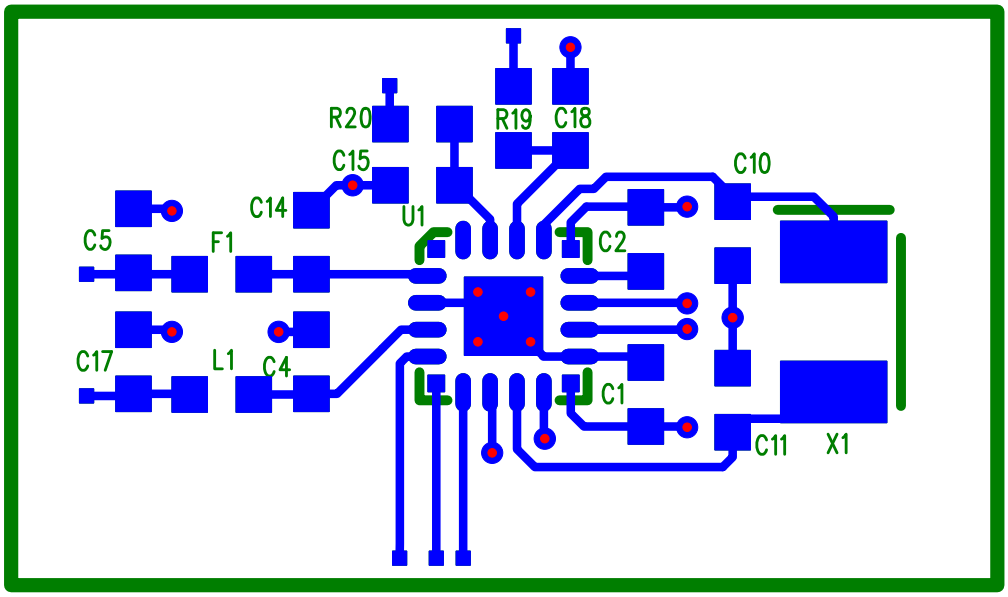


Figure 2. Layout Example 1

Figure 3 shows critical component layout with top and bottom side placement, top and bottom side routing, crystal and analog output support, and support for all devices except the Si471x transmitter family. The Si471x transmitter family can be supported in this example if VA bypass cap C2 is removed and audio input is routed to GND/RIN/DOUT pin 15 and VA/LIN/DFS pin 16. Digital audio is not available when the crystal is used due to the multipurpose role of GPO3/DCLK pin 17. Route the RCLK trace as far from the SDIO pin 8 and trace as possible by routing the RCLK trace on the bottom layer. This example is preferred for optimal oscillator performance.

F1, C14, C15, C18, R19, and R20 are placed as close to the chip as possible. For the Si4704/05/06/2x with the short antenna option, pin 4 is populated with L1 and C4, C17 is not populated; for the Si473x AM receiver, C4 is replaced with C16, L1 is replaced with L2, and C17 is populated.

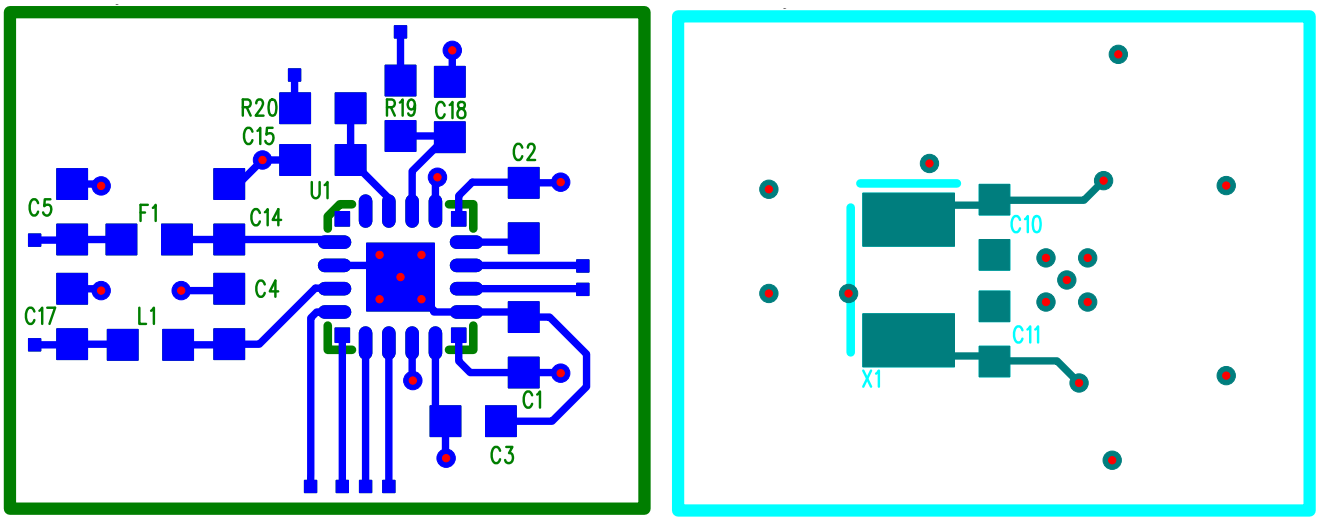


Figure 3. Layout Example 2

Figure 4 shows critical component layout with top and bottom side placement, top and bottom side routing, analog and digital input and output support, and support for all devices except the Si4702/03 receiver family. The Si4702/03 receiver family can be supported in this example if the VA supply is routed to VA/LIN/DFS pin 16 and R12 is removed. The crystal is not available when digital audio is used due to the multipurpose role of GPO3/DCLK pin 17. Note that the RCLK trace is not a sensitive node when an external reference clock is used instead of the crystal. For this reason, an external reference clock allows more routing flexibility.

F1, C14, C15, C18, R19, and R20 are placed as close to the chip as possible. For the Si4704/05/06/2x with the short antenna option, pin 4 is populated with L1 and C4, C17 is not populated; for the Si473x AM receiver, C4 is replaced with C16, L1 is replaced with L2, and C17 is populated.

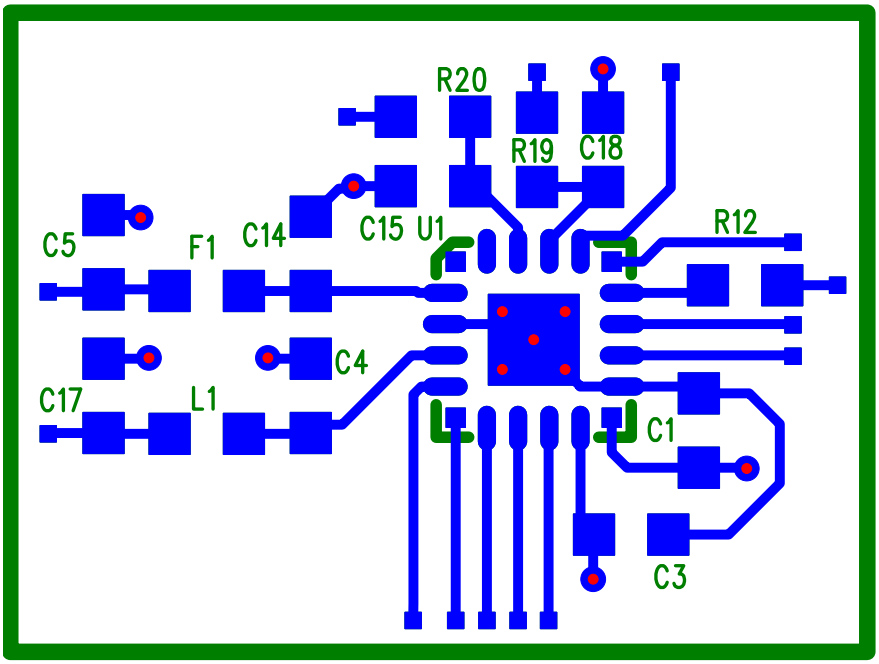


Figure 4. Layout Example 3

Figure 5 shows critical component layout with top and bottom side placement, top and bottom side routing, crystal support, analog and digital input and output support, and support for all devices. For this reason it is referred to as a universal layout. Either crystal or digital audio operation must be selected due to the multipurpose role of GPO3/DCLK pin 17. Note that the RCLK trace is not a sensitive node when an external reference clock is used instead of the crystal. For this reason, an external reference clock allows more routing flexibility. To support the crystal oscillator feature, route the RCLK trace as far from the SDIO pin 8 and trace as possible by routing the RCLK trace on the bottom layer.

F1, C14, C15, C18, R19 and R20 are placed as close to the chip as possible. For the Si4704/05/06/2x with the short antenna option, pin 4 is populated with L1 and C4, C17 is not populated; for the Si473x AM receiver, C4 is replaced with C16, L1 is replaced with L2, and C17 is populated.

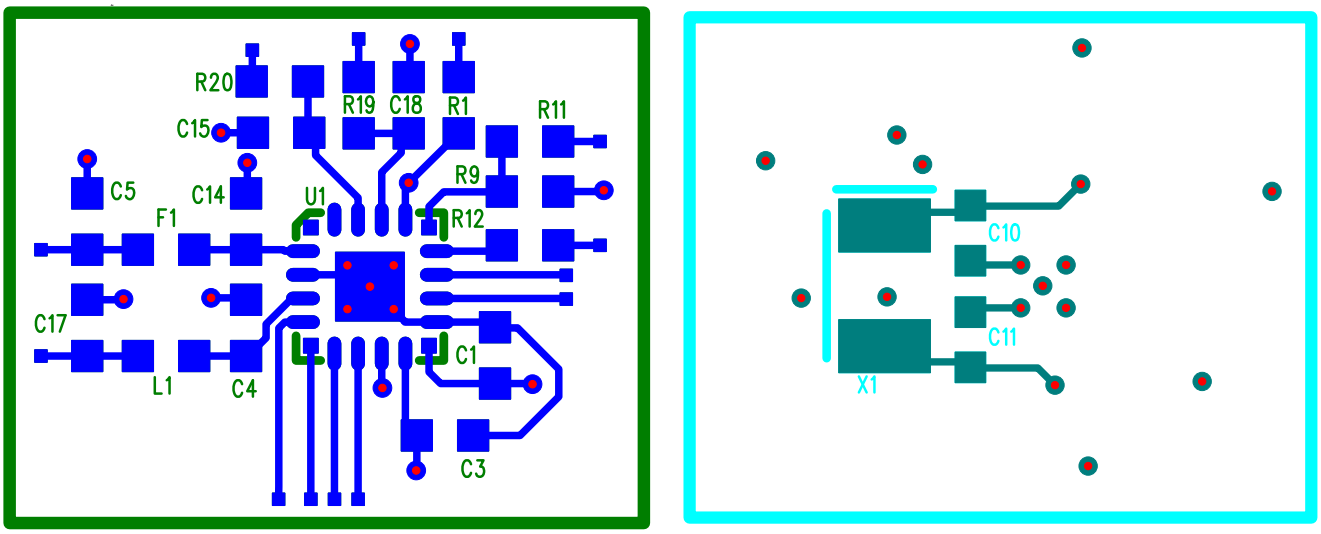


Figure 5. Layout Example 4

Place a ground plane under the Si47xx as shown in Figure 6, “Two Layer Stackup” or Figure 7, “Four Layer Stackup”. For designs in which a continuous ground plane is not possible, place a local ground plane directly under the Si47xx. Do not route signal traces on the ground layer under the Si47xx and do not route signal traces under the Si47xx without a ground plane between the Si47xx and signal trace. Flood the primary and secondary layers with ground and place stitching vias to create a low impedance connection between planes.

Do not route digital or RF traces over breaks in the ground plane. Route all traces to minimize inductive and capacitive coupling by keeping digital traces away from analog and RF traces, minimizing trace length, minimizing parallel trace runs, and keeping current loops small. In particular, care should be taken to avoid routing digital signals or reference clock traces near or parallel to the VCO pins 1, 20 or LOUT/ROUT pins 14, 13. Digital traces should be routed in between ground planes (on the inner layers) for best performance. If that is not possible, route digital traces on the opposite side of the chip.

Route all GND (including RFGND) pins to the ground pad. The ground pad should be connected to the ground plane using multiple vias to minimize ground potential differences. The exception is GND/RIN/DOUT when designing for a universal layout.

Route power to the Si47xx by trace, ensuring that each trace is rated to handle the required current. Some trace impedance is preferable so that the decoupling currents are forced to flow through decoupling caps C1, C2, and C3 directly to the ground pins and not by alternate pathways.

Place the Si47xx close to the antenna(s) to minimize antenna trace length and capacitance and to minimize inductive and capacitive coupling. This recommendation must be followed for optimal device performance. Route the antenna trace over an unobstructed ground plane to minimize antenna loop area and inductive coupling. Design, Place, and Route other circuits such that radiation in the band of interest is minimized.



Figure 6. Two Layer Stackup

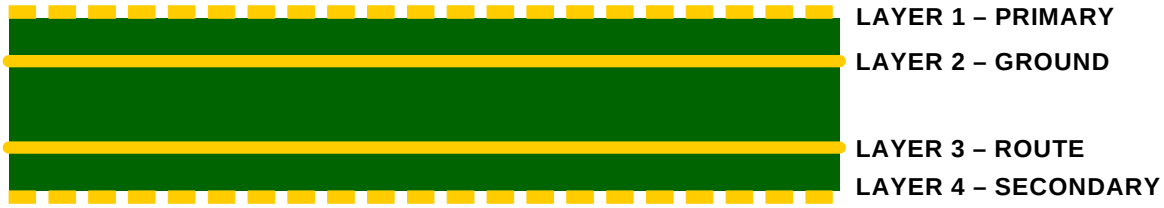


Figure 7. Four Layer Stackup

2.6. Si47xx 3x3 mm Design Checklist

The following design checklist summarizes the guidelines presented in this section:

- ☐ Place bypass caps C1, C2 and C3 as close as possible to the supply and ground pins.
- ☐ Place a via connecting C1, C2, and C3 to the power supplies such that the cap is between the Si47xx and the via.
- ☐ Route a wide, low inductance return current path from the C1, C2, and C3 to the Si47xx GND pins.
- ☐ Route GND/LIN/DOUT pin 15 to the GND pad if designing only for the Si4702/03.
- ☐ Route C1 GND directly and only to GND pin 12. Do not connect GND via to C1.
- ☐ Place resistor R1 as close to pin GPO3/DCLK 17 as possible.
- ☐ Place R9 as close as possible to VA/LIN/DFS pin16 as possible.
- ☐ Place resistor R11 as close to pin VA/LIN/DFS 16 as possible.
- ☐ Place resistor R12 as close to pin GND/RIN/DOUT 15 as possible.
- ☐ Place the series termination resistors R2–R6, R13–R16 as close to the host controller as possible.
- ☐ Place caps C12 or C13 close to the chip if digital audio is used.
- ☐ Place the crystal X1 as close to GPO3/DCLK pin 17 and RCLK pin 9 as possible.
- ☐ Route the SDIO trace and RCLK trace as far away from each other as possible when using crystal X1.
- ☐ Place caps C10 and C11 such that they share a common GND connection.
- ☐ Place a ground plane under the device as shown in Figure 6, “Two Layer Stackup” or Figure 7, “Four Layer Stackup”.
- ☐ Place a local ground plane directly under the device for designs in which a continuous ground plane is not possible.
- ☐ Route all traces to minimize inductive and capacitive coupling by keeping digital traces away from analog and RF traces, minimizing trace length, minimizing parallel trace runs, and keeping current loops small.
- ☐ Route digital traces in between ground plane for best performance. If that is not possible, route digital traces on the opposite side of the chip.
- ☐ Route all GND (including RFGND) pins to the ground pad. The ground pad should be connected to the ground plane using multiple vias minimize ground potential differences. The exception is GND/RIN/DOUT when designing for the universal layout.
- ☐ Route power to the Si47xx by trace, ensuring that each trace is rated to handle the required current.
- ☐ Do not route signal traces on the ground layer directly under the Si47xx.
- ☐ Do not route signal traces under the Si47xx without a ground plane between the Si47xx and signal trace.
- ☐ Do not route digital or RF traces over breaks in the ground plane.
- ☐ Do not route digital signals or reference clock traces near to the VCO pin 1 and 20 or the LOUT/ROUT output pin 14 and 13.

- ☐ Do not route VCO pin 1 and 20 (NC). These pins must be left floating to guarantee proper operation.
- ☐ Place the Si47xx close to the antenna(s) to minimize antenna trace length and capacitance and to minimize inductive and capacitive coupling. This recommendation must be followed for optimal device performance.
- ☐ Route the antenna trace over an unobstructed ground plane to minimize antenna loop area and inductive coupling.
- ☐ Design, place, and route other circuits such that radiation in the band of interest is minimized.
- ☐ Tie unused pin(s) to GND, but do not tie No Connect (NC) pins to GND. For example, in Si471x FM transmitter analog audio input mode, DFS pin 14 and DIN pin 13 are not used; therefore, these two pins should be tied to GND.

2.6.1. Emissions Mitigation Checklist

The following design checklist summarizes the guidelines for mitigating emissions in the 3–4 GHz range, if applicable.

- ☐ Place F1 as close as possible to FMI pin 2.
- ☐ Place C14 as close as possible to FMI pin 2.
- ☐ Place C5 even though it is designated as NP, it should be as close as possible to FMI pin2.
- ☐ On the Si4704/05/06/1x/2x products:
  - Place C4 as close as possible to LPI/TXO pin 4 and RFGND pin 3.
  - Place L1 as close as possible to LPI/TXO pin 4.
- ☐ On Si473x products:
  - Place C16 as close as possible to AMI pin 4 and RFGND pin 3.
  - Place L2 as close as possible to AMI pin 4.
  - Place C17 as close as possible to AMI pin 4 and RFGND pin 3.
- ☐ Place C15 and C18 as close as possible to GPO1 & GPO2 pins.
- ☐ Place R19 and R20 as close as possible to GPO1 & GPO2 pins.
- ☐ Route FMI pin 2 to GND/RFGND if the pin functionality is not used.
- ☐ Route TXO/AMI/LPI pin 4 to GND/RFGND if the pin functionality is not used.
- ☐ Flood the primary and secondary layers with ground and place stitching vias between the GND fill and GND plane.
- ☐ Shunt capacitors C4, C5, C14, C15, C16, C17, and C18 should be connected directly to the GND plane on top layer.
- ☐ Do not use heat relief for these pad's GND connection.
- ☐ Connecting shunt capacitors only to a via to the GND plane is not sufficient; though it is permissible to have such a via if the top GND plane is also connected.
- ☐ If additional space is available, increase the size of RFGND trace by moving FMI and AMI signal paths further apart.
- ☐ Avoid unnecessary breaks in the top ground fill between the Si47xx and the system GND connection. The goal is to have the path from shunt capacitors as direct, unbroken, and wide as possible.
- ☐ Rotate the Si47xx (as necessary) in order to create the best ground path for the FMI and GPO mitigation as these are the greater contributors to emissions.
- ☐ Orient the shunt capacitor(s) on FMI (C14) to the right of the trace (towards pin 1).
- ☐ Orient the shunt capacitors on AMI (C16 & C17) to the right of the trace (toward RFGND, pin 3).

3. Headphone Antenna for FM Receiver on FMI (Si470x/2x/3x/8x Only)

The Si470x/2x/3x FM Receiver component supports a headphone antenna interface through the FMI pin. A headphone antenna with a length between 1.1 and 1.45 m suits the FM application very well because it is approximately half the FM wavelength (FM wavelength is ~3 m).

3.1. Headphone Antenna Design

A typical headphone cable will contain three or more conductors. The left and right audio channels are driven by a headphone amplifier onto left and right audio conductors and the common audio conductor is used for the audio return path and FM antenna. Additional conductors may be used for microphone audio, switching, or other functions, and in some applications the FM antenna will be a separate conductor within the cable. A representation of a typical application is shown in Figure 8, “Typical Headphone Antenna Application”.

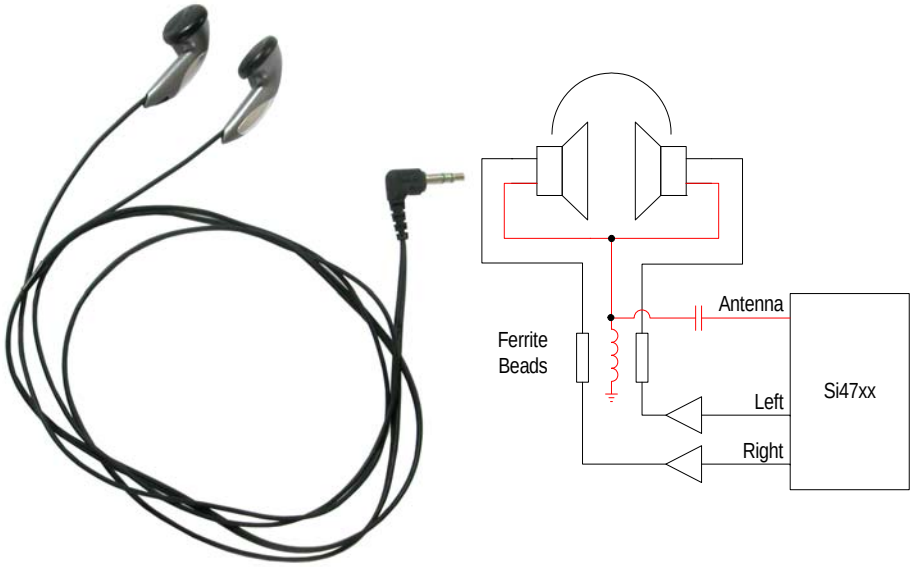


Figure 8. Typical Headphone Antenna Application

3.2. Headphone Antenna Schematic

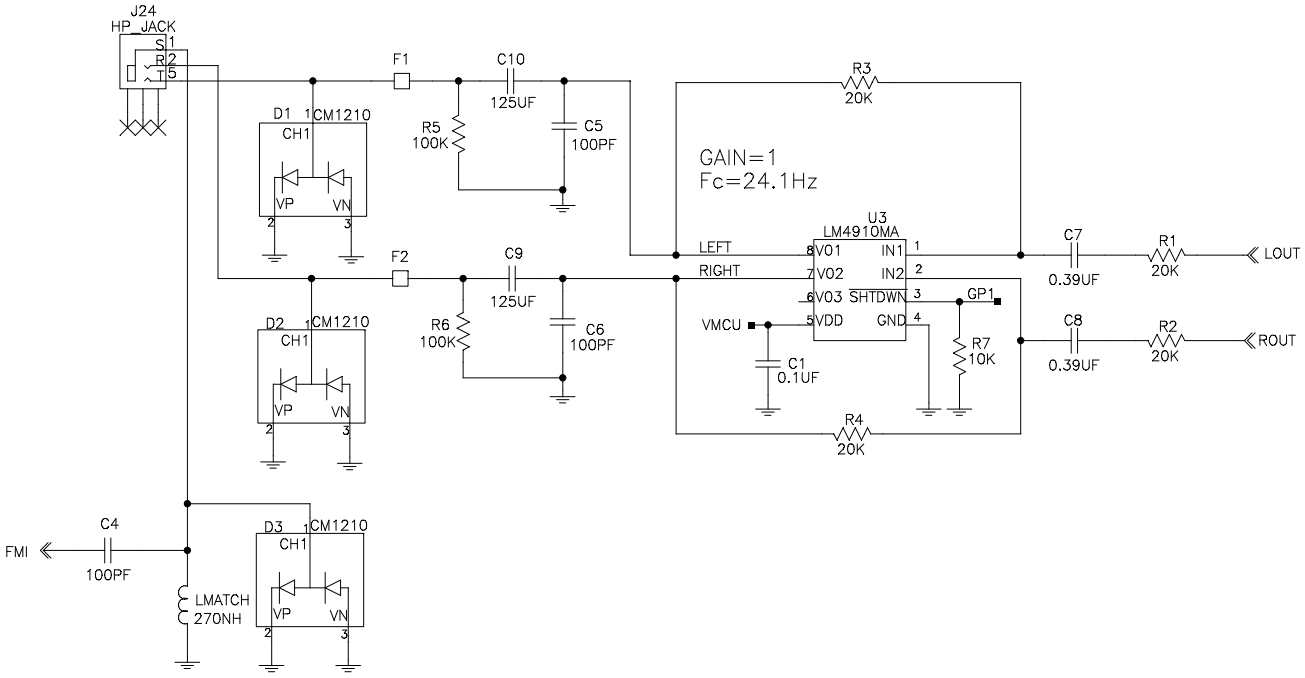


Figure 9. Headphone Antenna Schematic

The headphone antenna implementation requires components L_{MATCH}, C4, F1, and F2 for a minimal implementation. The ESD protection diodes and headphone amplifier components are system components that will be required for proper implementation of any tuner.

Inductor L_{MATCH} is selected to maximize the voltage gain across the FM band. L_{MATCH} should be selected with a Q of 15 or greater at 100 MHz and minimal dc resistance.

AC-coupling capacitor C4 is used to remove a dc offset on the FMI input. This capacitor must be chosen to be large enough to cause negligible loss with an LNA input capacitance of 4–6 pF. The recommended value is 100 pF–1 nF.

Ferrite beads F1 and F2 provide a low-impedance audio path and high-impedance RF path between the headphone amplifier and the headphone. Ferrite beads should be placed on each antenna conductor connected to nodes other than the FMIP such as left and right audio, microphone audio, switching, etc. In the example shown in Figure 9, these nodes are the left and right audio conductors. Ferrite beads should be 2.5 kΩ or greater at 100 MHz, such as the Murata BLM18BD252SN1. High resistance at 100 MHz is desirable to maximize R_{SHUNT}, and therefore, R_P. Refer to " Appendix A—FM Receive Headphone Antenna Interface Model" on page 50 for a complete description of R_{SHUNT}, R_P, etc.

ESD diodes D1, D2, and D3 are recommended if design requirements exceed the ESD rating of the headphone amplifier and the Si47xx. Diodes should be chosen with no more than 1 pF parasitic capacitance, such as the California Micro Devices CM1210. Diode capacitance should be minimized to minimize C_{SHUNT}, and therefore, C_P. If D1 and D2 must be chosen with a capacitance greater than 1 pF, they should be placed between the ferrite beads F1 and F2 and the headphone amplifier to minimize C_{SHUNT}. This placement will, however, reduce the effectiveness of the ESD protection devices. Diode D3 may not be relocated and must therefore have a capacitance less than 1 pF. Note that each diode package contains two devices to protect against positive and negative polarity ESD events.

C9 and C10 are 125 µF ac coupling capacitors required when the audio amplifier does not have a common mode output voltage and the audio output is swinging above and below ground.

Optional bleed resistors R5 and R6 may be desirable to discharge the ac-coupling capacitors when the headphone cable is removed.

Optional RF shunt capacitors C5 and C6 may be placed on the left and right audio traces at the headphone amplifier output to reduce the level of digital noise passed to the antenna. The recommended value is 100 pF or greater, however, the designer should confirm that the headphone amplifier is capable of driving the selected shunt capacitance.

This schematic example uses the National Semiconductor LM4910 headphone amplifier. Passive components R1–R4 and C7–C8 are required for the LM4910 headphone amplifier as described in the LM4910 data sheet. The gain of the right and left amplifiers is –R3/R1 and –R4/R2, respectively. These gains can be adjusted by changing the values of resistors R3 and R4. As a general guide, gain between 0.6 and 1.0 is recommended for the headphone amplifier, depending on the gain of the headphone elements. Capacitors C7 and C8 are ac-coupling capacitors required for the LM4910 interface. These capacitors, in conjunction with resistors R1 and R2, create a high-pass filter that sets the audio amplifier's lower frequency limit. The high-pass corner frequencies for the right and left amplifiers are:

$$f_{CRIGHT} = \frac{1}{2\pi \cdot R1 \cdot C7}, f_{CLEFT} = \frac{1}{2\pi \cdot R2 \cdot C8}$$

With the specified BOM components, the corner frequency of the headphone amplifier is approximately 20 Hz.

Capacitor C1 is the supply bypass capacitor for the audio amplifier. The LM4910 can also be shut down by applying a logic low voltage to the number 3 pin. The maximum logic low level is 0.4 V and the minimum logic high level is 1.5 V.

The bill of materials for the typical application schematic shown in Figure 6 is provided in Table 12. Note that manufacturer is not critical for resistors and capacitors.

3.3. Headphone Antenna Bill of Materials

Table 12. Headphone Antenna Bill of Materials

Designator	Description	Note
LMATCH	IND, 0603, SM, 270 nH, MURATA, LQW18ANR27J00D	
C4	AC coupling cap, SM, 0402, X7R, 100 pF	
D1, D2, D3	IC, SM, ESD DIODE, SOT23-3, California Micro Devices, CM1210-01ST	
U3	IC, SM, HEADPHONE AMP, National Semiconductor, LM4910MA	
R1, R2, R3, R4	RES, SM, 0603, 20 kΩ	
C7, C8	CAP, SM, 0603, 0.39UF, X7R	
C5, C6	CAP, SM, 0402, C0G, 100 pF	
R5, R6	RES, SM, 0603, 100 kΩ	
F1, F2	FERRITE BEAD, SM, 0603, 2.5 kΩ, Murata, BLM18BD252SN1D	
C1	CAP, SM, 0402, X7R, 0.1 µF	
R7	RES, SM, 0402, 10 kΩ	

3.4. Headphone Antenna Layout

To minimize inductive and capacitive coupling, inductor L_{MATCH} and headphone jack J24 should be placed together and as far from noise sources such as clocks and digital circuits as possible. L_{MATCH} should be placed near the headphone connector to keep audio currents away from the Si47xx.

To minimize C_{SHUNT} and C_P, place ferrite beads F1 and F2 as close as possible to the headphone connector.

To maximize ESD protection diode effectiveness, place diodes D1, D2 and D3 as close as possible to the headphone connector. If capacitance larger than 1 pF is required for D1 and D2, both components should be placed between FB1 and FB2 and the headphone amplifier to minimize C_{SHUNT}.

Place the chip as close as possible to the headphone connector to minimize antenna trace capacitance, CPCBANT. Keep the trace length short and narrow and as far above the reference plane as possible, restrict the trace to a microstrip topology (trace routes on the top or bottom PCB layers only), minimize trace vias, and relieve ground fill on the trace layer. Note that minimizing capacitance has the effect of maximizing characteristic impedance. It is not necessary to design for 50 Ω transmission lines.

To reduce the level of digital noise passed to the antenna, RF shunt capacitors C5 and C6 may be placed on the left and right audio traces close to the headphone amplifier audio output pins. The recommended value is 100 pF or greater, however, the designer should confirm that the headphone amplifier is capable of driving the selected shunt capacitance.

3.5. Headphone Antenna Design Checklist

- ☐ **Select** an antenna length of 1.1 to 1.45 m.
- ☐ **Select** matching inductor L_{MATCH} to maximize signal strength across the FM band.
- ☐ **Select** matching inductor L_{MATCH} with a Q of 15 or greater at 100 MHz and minimal dc resistance.
- ☐ **Place** inductor L_{MATCH} and headphone connector together and as far from potential noise sources as possible to reduce capacitive and inductive coupling.
- ☐ **Place** the Si47xx close to the headphone connector to minimize antenna trace length. Minimizing trace length reduces CP and the possibility for inductive and capacitive coupling into the antenna by noise sources. This recommendation must be followed for optimal device performance.
- ☐ **Select** ferrite beads F1–F2 with 2.5 kΩ or greater resistance at 100 MHz to maximize RSHUNT and, therefore, RP.
- ☐ **Place** ferrite beads F1-F2 close to the headphone connector.
- ☐ **Select** ESD diodes D1-D3 with minimum capacitance.
- ☐ **Place** ESD diodes D1-D3 as close as possible to the headphone connector for maximum effectiveness.
- ☐ **Place** optional RF shunt capacitors near the headphone amplifier's left and right audio output pins to reduce the level of digital noise passed to the antenna.

4. Cable Antenna for FM Receive on FMI (Si470x/2x/3x/8x Only)

The charger cable of a consumer product can be used as an FM antenna. This section describes how to interface the Si47xx FMI input to a cable antenna.

4.1. Cable Antenna Design



Figure 10. Sample Cigarette Lighter Adapter for Cable Antenna

A typical cable antenna contains multiple inner wires/conductors, which are covered with a protective ground shield. The coupling between the wires and the shield can cause the antenna to have large capacitance in the several hundred pico farad range. In order to boost the received FM voltage, it is necessary to minimize this capacitance. This reduction can be achieved by placing ferrite beads in series with each of the antenna's conductors.

4.2. Cable Antenna Schematic

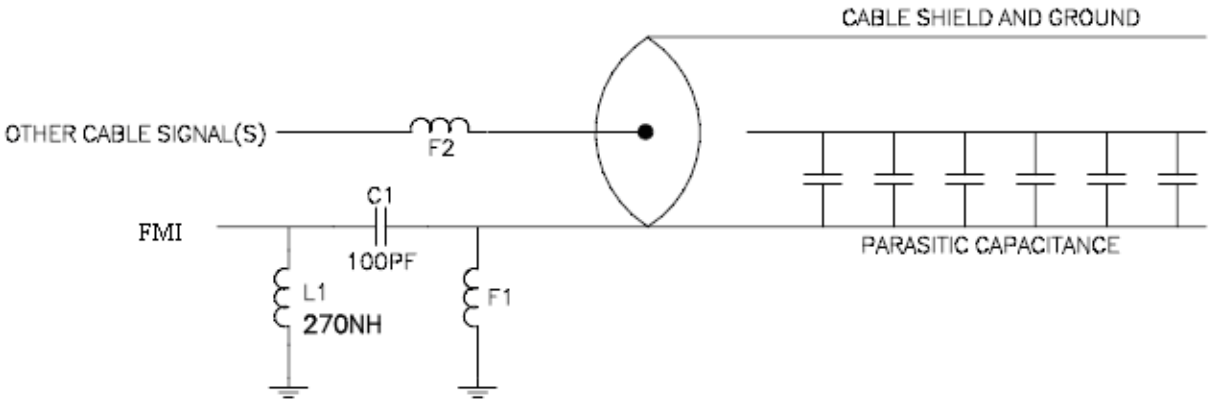


Figure 11. Cable Antenna Schematic

To resonate the cable antenna within the FM band, the antenna's capacitance needs to be reduced. As described in Section "4.2. Cable Antenna Schematic", this reduction can be achieved by placing the ferrite beads in series with each of the antenna's conductors. The capacitance should be further controlled by limiting the trace length from the cable ground shield and the RF input pin (FMI input) on the Si47xx FM tuner. Each of the components in the schematic above is explained in detail below:

L1 (27 0nH) is the tuning inductor. This is the typical value used to resonate the cable antenna in the center of the FM band.

F1 (2.5 kΩ at 100 MHz) is a shunt ferrite to ground at the cable antenna side. A substantial amount of ground return current may flow through the cable antenna shield/ground because there are multiple conductors inside the cable along with power supply conductors. The ferrite will divert the ground return current of the cable antenna to go through the shunt ferrite rather than going through the tuning inductor and/or Si47xx chip.

C1 (100 pF) is a dc blocking cap placed between the FMI pin and the cable antenna ground. The capacitor is used to isolate the cable return currents from the FMI pin.

F2 (2.5 kΩ at 100 MHz) is a series ferrite placed on the signal conductor in the cable antenna. Note that series ferrites should be placed on each signal conductor in the cable. The ferrite is used to isolate the signal conductors from the shield/ground of the cable antenna and reduce parasitic capacitance seen by the shield/ground. The choice of the ferrite is dependent upon the type of signal on each individual conductor. If the conductor is used to carry power, then a ferrite with a large dc current carrying capability should be used. If the conductor is used to carry high frequency digital signals, make sure that the ferrite does not block the high frequency component of these signals. Likewise if the conductor is used to carry high frequency analog signals, make sure that the ferrite does not filter the high frequency.

4.3. Cable Antenna Bill of Materials

The required bill of materials is shown below:

Table 13. Bill of Materials

Designator	Description	Notes
L1	IND, 0603, SM, 270 nH, MURATA, LQW18ANR27J00D	
C1	DC blocking capacitor, SM, 0402, X7R, 100 pF	
F1	Shunt Ferrite bead, FERRITEBEAD, SM, 0603, 470 Ω, 1 A, Murata, BLM18PG471SN1J	Rated dc current > max expected ground return current
F2	Series Ferrite bead, various types. Recommended ferrite for power lines: FERRITEBEAD, SM, 0603, 470 Ω, 1 A, Murata, BLM18PG471SN1J Recommended ferrite for signals: FERRITEBEAD, SM, 0603, 2.5 kΩ, 50 mA Murata, BLM18BD252DN1D	For power signals, make sure the rated dc current > max expected ground return current. For all other signals, make sure ferrite does not block/filter the high frequency component of the signals.

4.4. Cable Antenna Layout

Place the chip as close to the cable antenna as possible. This will minimize the trace length going to the cable antenna which will minimize the parasitic capacitance. Place the shunt ferrite for the ground return current as close to the cable as possible. Putting the shunt ferrite for the ground return current close to the cable ensures that the ground return current has minimal loop which will reduce noise coupling. The series ferrites also should be put as close as possible to the cable. This will minimize the parasitic capacitance seen by the FMI pin.

4.5. Cable Antenna Design Checklist

- Place the chip as close as possible to the cable antenna to minimize parasitic capacitance.
- Place the tuning inductor, L1, as far away from noise sources as possible.
- Make sure that the shunt ferrite has a dc rating that exceeds the expected max ground return current of the cable.
- Place the shunt ferrite close to the cable.
- Choose series ferrite that is appropriate for each type of signal in the conductor.
- Place the series ferrite(s) close to the cable.

5. Embedded Antenna for FM Transmit on TXO and Receive on LPI (Si4704/05/06/1x/2x Only)

The FM Transmitter component on the Si471x/2x and the FM Receiver component on the Si4704/05/06/2x support an embedded antenna interface through the TXO/LPI pin. In the case of the Si472x FM Transceiver, the same embedded antenna can be used for both FM Transmit and Receive.

5.1. Embedded Antenna Design

An embedded antenna can be designed using a loose wire, flex circuit, or PCB trace and can be categorized into two types: stub antenna and loop antenna. For the purpose of this application note, three types of embedded antenna will be covered in detail:

- Embedded stub (wire)
- Embedded loop (wire)
- Embedded stub (PCB trace)

The following table summarizes the advantages and disadvantages of these implementations.

Antenna	Description	Advantages	Disadvantages
Embedded Stub (Wire)	■ Wire attached to or molded inside product case ■ Connect to pin 4 for TX/RX	■ Placement flexibility ■ Minimum PCB space ■ Easy to adjust length during design testing	■ Mechanical attachment to case required ■ Performance can be impacted by case shielding
Embedded Loop (Wire)	■ Wire loop attached to or molded inside product case ■ Connect to pin 4 for TX/RX	■ Can achieve high efficiency per length ■ Placement flexibility ■ Minimum PCB space ■ Easy to adjust length during design testing	■ Mechanical attachment to case required ■ Performance can be impacted by case shielding
Embedded Stub (PCB Trace)	■ Wire trace fabricated on outer PCB copper layer ■ Connect to pin 4 for TX/RX	■ No mechanical attachment to case ■ Ease of product assembly	■ PCB keep out regions required around antenna ■ Additional PCB space ■ Performance can be impacted by case shielding

Figure 12 is an example of a stub antenna in wire implementation buried inside a cellular handset. Explanations of the dimensions A, B, C, and D are included later in this document.

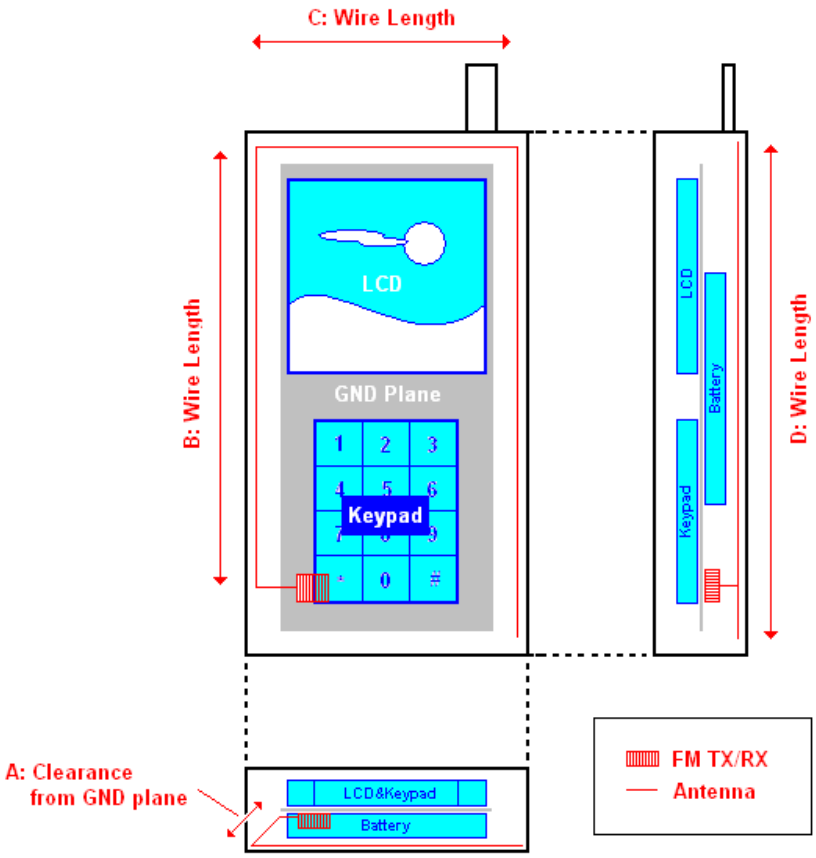


Figure 12. Stub Antenna in Wire Implementation

5.1.1. Embedded Stub Antenna—Wire Implementation

A stub (wire) antenna is typically a floating wire that is approximately 10 cm in length and is embedded inside the device with FM functionality. The antenna can be longer if the device's industrial design will accommodate it. The material for a stub (wire) antenna can be an actual wire or a PCB trace. PCB traces can be either in flexible packaging (flexible PCB trace) or as a trace on the PCB. The 24AWG wire has been experimentally proven to have optimal performance.

The stub (wire) antenna should be placed such that it is not obstructed by a ground plane or shield. This requirement can be met by placing the antenna on an extremity of the device (e.g., top or bottom) or on the perimeter. The antenna can also be embedded in the device plastic or outside the plastic with a protective covering. The flexible PCB antenna should be between a PCB and the device plastic such that the antenna trace is not obstructed by a ground plane or shield. The antenna is connected to pin 4 and resonated with the on-chip variable capacitor.

5.1.1.1. Matching

A 10 cm stub (wire) antenna has a capacitive impedance, typically more than 1~2 pF. The antenna is matched by resonating it with a shunt inductor and the on-chip shunt variable capacitor. See Appendix B for inductor value calculation.

5.1.1.2. Configuration

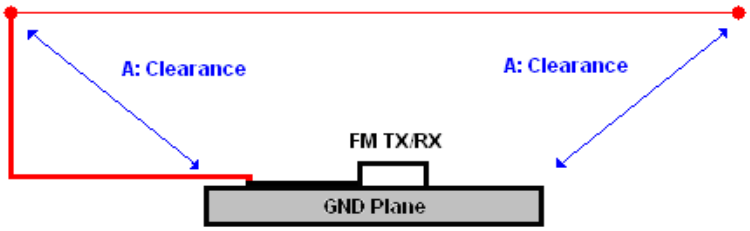


Figure 13. Stub (Wire) Antenna - Side View

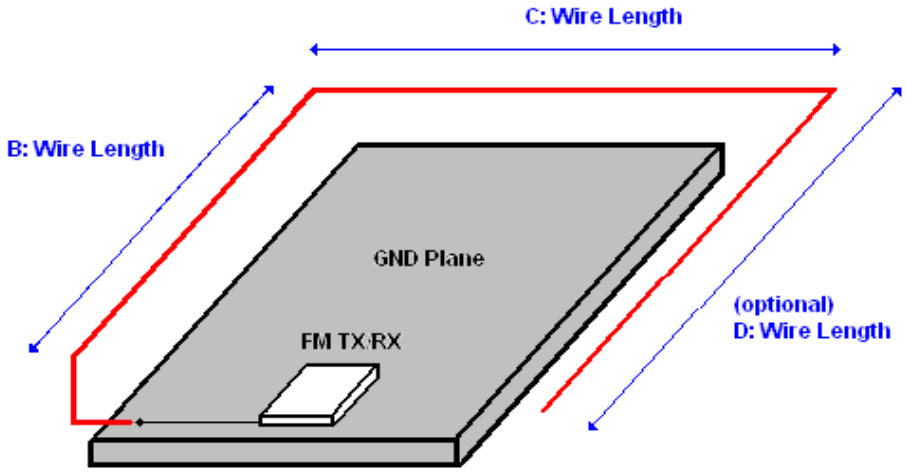


Figure 14. U-Shaped Stub (Wire) Antenna—Orthogonal View

5.1.1.3. Antenna Layout Guidelines

- Route the antenna as a "U" shape as shown in Figure 14.
  - A > 5 mm
  - B + C > 10 cm
- Route the antenna as an "L" by removing segment D if a "U" is not possible.
- Maximize antenna length (B+C >10 cm) to provide sufficient radiating power for transmit and maximize incident voltage for receive.
- Keep the antenna as far from the ground plane, shield, and other metal structures (e.g., batteries) as possible (A > 5 mm), and make the enclosure from non-conductive material, such as plastic, to minimize parasitic capacitance and maximize radiation for transmit or maximize incident voltage for receive.
- Antenna capacitance for an ideal wire antenna is approximated by Cant = L/(198 x c), where L is length of wire in meters and c is speed of light (3.0×10^8 m/s). A general guideline to follow is to assume that each centimeter of wire antenna adds ~0.17 pF of capacitance (for L << λ/20).

Length (cm)	C Ant (pF)
10	1.68
11	1.85
12	2.02
13	2.19
14	2.36
15	2.53

- Use an ideal vertical wire antenna as a reference point to measure the performance of the wire antenna. Antenna capacitance will be larger and antenna performance will degrade in a practical application where the wire antenna is bent parallel to the GND plane.

5.1.2. Embedded Loop Antenna—Wire Implementation

A loop (wire) antenna is typically a floating wire that is approximately 13 cm or greater in circumference and is embedded inside the device with FM functionality. It is constructed with a floating wire or flexible PCB trace. The shape of the antenna can be circular or rectangular with the goal of maximizing the enclosed area. The 24AWG has been experimentally proven to have optimal performance. A floating wire antenna is typically embedded in the plastics, or outside of the plastics (with protective covering), at the perimeter of the device such that the antenna trace is not obstructed by the ground plane, shield, or other metal structures (e.g., batteries).

Placement of the flexible PCB is typically between the main PCB and plastics such that the antenna trace is not obstructed by a ground plane or shield. A loop antenna is similar to a short wire antenna with the exception that the other end of the antenna is grounded. Because the other end is grounded, a loop antenna by itself is an inductor.

5.1.2.1. Antenna Matching

A loop (wire) antenna is an inductor of high impedance. The antenna is matched by resonating it with a shunt inductor or capacitor and the on-chip shunt variable capacitor.

5.1.2.2. Configuration

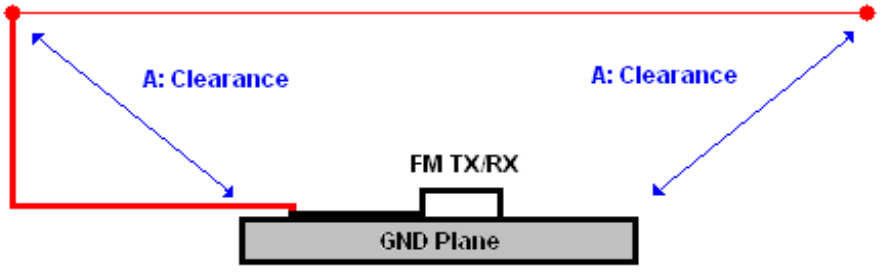


Figure 15. Loop (Wire) Antenna—Side View

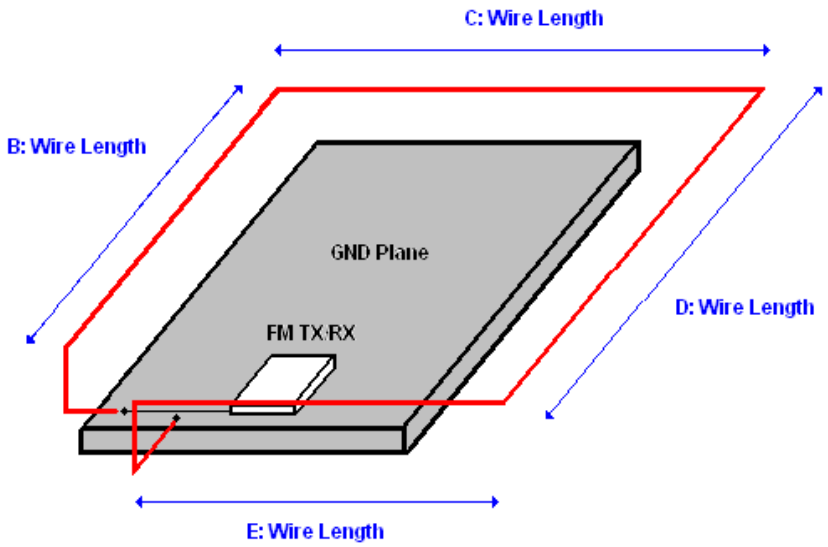


Figure 16. Rectangular Loop (Wire) Antenna—Orthogonal View

5.1.2.3. Design Guidelines

- Route the antenna as shown in Figure 16.
  - A > 5 mm
  - B + C + D + E > 13 cm
  - C > 3 cm
- Maximize antenna length (B+C+D+E >13 cm) to provide sufficient radiating power for transmit and maximize incident voltage for receive.
- Keep the antenna as far from the ground plane and shield as possible (A > 5 mm), and make the enclosure from non-conductive material (plastic), to minimize parasitic capacitance and maximize radiation for transmit or maximize incident voltage for receive.
- Antenna inductance for an ideal loop antenna is given by $L_{ant} = n^2\mu_0 r[\ln(8r/b)]$.

r: loop radius (m)

n: number of turns

μ_0: permeability ($4\pi \times 10^{-7}$ N/A^2)

b: wire radius (m)

Number of turns greater than one usually results in a high inductance loop with which the varactor cannot resonate. It is acceptable to place two loops in a parallel structure to reduce the effective inductance.

For a loop with a small radius used in cellular handset or mp3 applications, the loop antenna equation can be approximately applied to a rectangular loop of the same circumference.

Radius (cm)	Turns	Total Length (cm)	L_{ant} (nH)
2	1	12.6	111.5
3	1	18.8	182.6
4	1	25.1	257.9

- Use an ideal vertical loop (wire) antenna as a reference point to measure the performance of the loop antenna. Antenna performance will degrade in a practical application where the loop antenna is bent parallel to the GND plane.

5.1.3. Embedded Stub Antenna—PCB Trace Implementation (Pin 4)

A stub antenna (PCB trace) is constructed using a 10 cm or longer PCB trace. The material can be any standard PCB. The PCB trace must be routed in an area without any copper fill, such as ground or power planes or other traces. The antenna is connected to pin 4 and resonated with the on-chip variable capacitor.

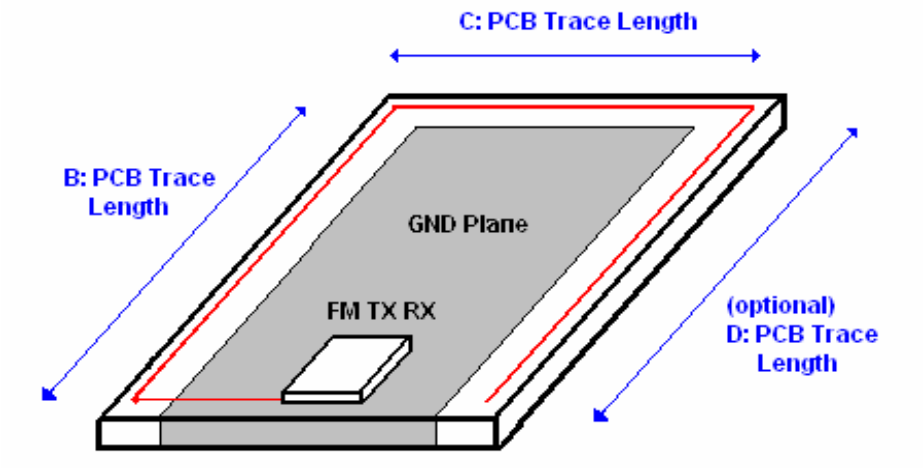


Figure 17. Stub (PCB Trace) Antenna—Orthogonal View

5.1.3.1. Antenna Matching

A 10 cm stub (wire) antenna is capacitive, typically more than 1~2 pF. The antenna is matched by resonating it with a shunt inductor and the on-chip shunt variable capacitor. See Appendix A and Appendix B for inductor value calculation.

5.1.3.2. Configuration

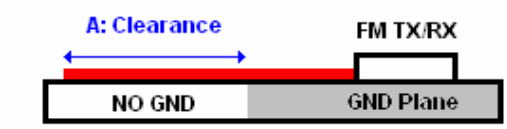


Figure 18. Stub (PCB Trace) Antenna—Side View

5.1.3.3. Design Guidelines

- Route the antenna as a "U" shape as shown in Figure 7.
  - A > 5 mm
  - B + C > 10 cm
- Route the antenna as an "L" by removing segment D if a "U" is not possible.
- Maximize antenna length (B + C >10 cm) to provide sufficient radiating power for transmit and maximize incident voltage for receive.
- It is not important to match D = B.
- Keep the antenna as far from the ground plane and shield as possible (A > 5 mm), and make the enclosure from non-conductive material (plastic), to minimize parasitic capacitance and maximize radiation for transmit or maximize incident voltage for receive.
- Antenna capacitance for an ideal PCB trace antenna is given by Cant = L/(198 x c), where L is length of wire in meters and c is speed of light (3.0×10^8 m/s). A general guideline to follow is to assume that each centimeter of wire antenna adds ~0.17 pF of capacitance (for L << λ/20).

Length (cm)	C_{ant} (pF)
10	1.68
11	1.85
12	2.02
13	2.19
14	2.36
15	2.53

5.2. Embedded Antenna Schematic

Figure 19 shows the embedded antenna schematic.

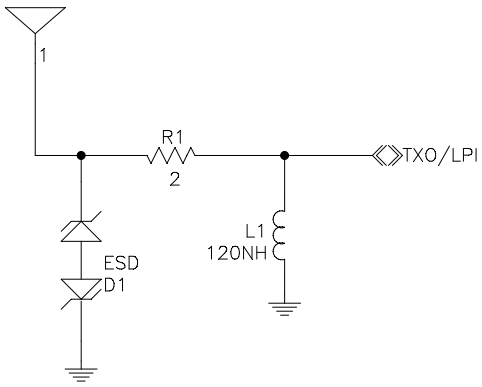


Figure 19. Embedded Antenna Schematic

L1 is the tuning inductor and typical value is 120nH. L1 needs to be chosen such that the resonant circuit of L1 and the total capacitance at the TXO/LPI pin will resonate at the FM band (76-108MHz). The total capacitance at the TXO/LPI pin includes the internal on-chip varactor, the antenna and all of the parasitic capacitance at that node. Therefore it is important to check the READANTCAP value as described below when the product is in fully assembled configuration.

There are two steps to select the value of L1: calculate L1 using the formula below, and then monitor the on-chip varactor value READANTCAP by sending the TX_TUNE_STATUS or FM_TUNE_STATUS command to make sure the on-chip varactor is still in-range.

The first step is approximating the value of L1 (which can be skipped). The formula to calculate L1 is as follows:

$$L1 = \frac{1}{(2\pi f)^2 Ctotal}$$

where:

f = frequency of FM band

Ctotal = total capacitance at the TXO/LPI pin

Note that Ctotal will vary because of the automatic tuning of the internal on-chip varactor. The internal on-chip varactor has value from 1-191 for 0.25pF step which equals to 0.25pF to 47.75pF. Knowing the other capacitance at the TXO/LPI pin which is layout and component dependent will give a range of Ctotal. After the approximate Ctotal has been calculated, L1 can be chosen to satisfy the formula above for the FM band.

After choosing the right L1 value, the user is still required to check the on-chip varactor value READANTCAP by sending the TX_TUNE_STATUS or FM_TUNE_STATUS command to make sure that the on-chip varactor has not gone out-of-range. User also can jump to this second step right away and skip the first step of approximating L1 by trying different values of L1.

The procedure to monitor the READANTCAP is as follows:

- Select at least three frequencies in the bottom, middle and top of the FM band (e.g. 88, 98, and 108 MHz) and get the READANTCAP values.
- It is even better if user sweeps the entire FM band and gets the READANTCAP values.
- L1 has a correct inductance value if
  - 1 < READANTCAP < 191
  - READANTCAP at 88 MHz > READANTCAP at 98 MHz > READANTCAP at 108 MHz
  - Be suspicious when READANTCAP returns the middle value of 97. It may be an indication that the inductor value is not correct.
- L1 is not the right value and needs to be changed if either one of these three conditions occur:
  - READANTCAP returns the bottom value of 1: it indicates that there is too much capacitance at the TXO/LPI pin. L1 needs to be adjusted to a smaller value or the better solution is to try to reduce the parasitic capacitance at the TXO/LPI pin
  - READANTCAP returns a middle value of 97: it indicates that there is way too much capacitance at the TXO/LPI pin. L1 needs to be adjusted to a smaller value or the better solution is to try to reduce the parasitic capacitance at the TXO/LPI pin
  - READANTCAP returns the top value of 191: it indicates that there is too little of a capacitance at the TXO/LPI pin (unlikely to happen). L1 needs to be adjusted to a bigger value.

The rest of the components in the embedded antenna schematic are optional.

D1 is the ESD diode and it is only necessary when there is an exposed pad going to the TXO/LPI pin.

R1 is the ESD current limiting resistor and used in conjunction with D1. It is only necessary when there is an exposed pad going to the TXO/LPI pin.

Note: When using an electrically short monopole antenna for Transmit, the radiated power varies with frequency. Specifically, as the transmit frequency increases, the monopole antenna becomes more efficient and hence the radiated power increases. This is important when testing for FCC limit because the transmit power level of the chip needs to be adjusted across the FM band.

5.3. Embedded Antenna Bill of Materials

Table 14. Embedded Antenna Bill of Materials

Designator	Description	Note
L1	Tuning inductor (typically 120 nH)	
R1	Current limiting resistor for ESD, 2 Ω	Optional, only needed if there is any exposed pad going to the TXO/LPI pin.
D1	ESD diode	Optional, only needed if there is any exposed pad going to the TXO/LPI pin.

5.4. Embedded Antenna Layout

The placement of the chip going into the embedded antenna is critical. Place the chip as close as possible to the embedded antenna feedline. This will minimize the trace going to the embedded antenna which in turn will minimize parasitic capacitance. If long trace is needed between the TXO/LPI pin to the embedded antenna, keep the trace as a microstrip topology where the trace is on the top or bottom layer. Do not bury the trace on the inner layer. Relieve the ground fill along the trace which includes the ground fill on the inner layer. Note that the goal is to minimize the parasitic capacitance as much as possible, it is not necessary to design a 50 Ω transmission lines in this applications because the embedded antenna is a high impedance antenna, and the parallel resonant circuit is also high impedance at the resonant frequency.

Put the optional ESD diode D1 and ESD current limiting resistor R1 as close to the embedded antenna as possible to ensure optimal ESD performance.

5.5. Embedded Antenna Design Checklist

- ☐ **Place** the chip as close as possible to the embedded antenna feedline to minimize parasitic capacitance.
- ☐ **Select** tuning inductor L1 with a Q>30 to maximize radiated power and received voltage.
- ☐ **Select** tuning inductor L1 as large as possible to maximize radiated power and incident voltage.
- ☐ **Place** the antenna, and in particular the end of the antenna opposite the Si47xx as far from the ground plane as possible to maximize radiated and received power.
- ☐ **Place** inductor L1 and the Si47xx chip as far from potential noise sources as possible to reduce capacitive and inductive coupling.
- ☐ **Place** optional components L2 to filter VCO spurs if needed.
- ☐ **Place** optional components D1 and R1 to achieve 8 kV contact discharge ESD protection if the antenna is exposed.
- ☐ **Select** ESD diode D1 with minimum capacitance.

6. Cable Antenna for FM Transmit on TXO and Receive on LPI (Si4704/05/06/1x/2x Only)

This section describes how to interface the Si47xx TXO output and LPI input to a cable antenna. An example of a cable antenna would be a cigarette light adapter (CLA) cable or a bundled cable going to the consumer product that may contain power conductors, audio signals, control signals, or any other auxiliary signals.

6.1. Cable Antenna Design

Using a cable as the antenna for FM usually means that the signal has to be driven to and/or received from the cable shield or ground. This is because most cable will have a protective shield covering the inner wires. In this case, the capacitive coupling between the ground shield and all other conductors can be very large. As a comparison, capacitance of a three-conductor headphone cable is approximately 10–20 pF because headphone cable does not have ground shield and only has two conductors plus a ground conductor. However, the capacitance from a cable antenna can be greater than 100–200 pF because of the ground shield and multiple conductors. This antenna capacitance can be reduced by placing ferrite beads on all conductor traces as shown in Figure 21. Minimizing antenna capacitance will maximize transmit and receive voltage.

The following picture shows a Cigarette Light Adapter (CLA) cable that can be used as a cable antenna for FM.



Figure 20. Cigarette Lighter Adapter (CLA)

6.2. Cable Antenna Schematic

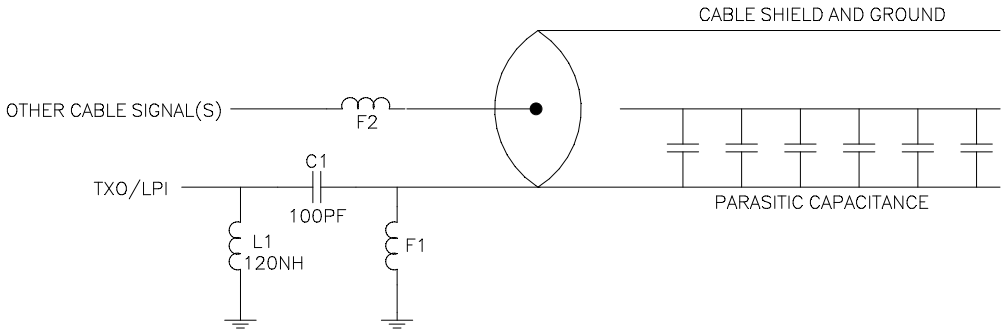


Figure 21. Cable Antenna Schematic

L1 (12 0nH) is the tuning inductor for the transmitter and receiver and the return current path for transmitter. The on-chip varactor can be configured to automatically resonate with the tuning inductor. Because of the large capacitance, it is also generally hard to have a high-Q system with a cable antenna. A high-Q system is generally desirable when using short antenna to maximize transmit and receive voltage. Fortunately, a high-Q system may not be necessary for a cable antenna since the cable antenna is an efficient radiator and receiver.

F1 (2.5 kΩ at 100 MHz) is a shunt ferrite to ground at the cable antenna side. A substantial amount of ground return current may flow through the cable antenna shield/ground because there are multiple conductors inside the cable along with power supply conductors. The ferrite will divert the ground return current of the cable antenna to go through the shunt ferrite rather than going through the tuning inductor and/or Si47xx chip.

The important property of the shunt ferrite is its dc current carrying capability and this depends on what is the maximum current that the cable antenna can deliver. For example if the cable antenna can charge the accessory connected to it with a 1 A of current, then the shunt ferrite should have a dc current rating of greater than 1 A (e.g., 3 A).

C1 (100 pF) is a dc blocking cap placed between the TXO/LPI pin and the cable antenna ground. The capacitor is used to isolate the cable return currents from the TXO/LPI pin.

F2 (2.5 kΩ at 100 MHz) is a series ferrite placed on the signal conductor in the cable antenna. Note that series ferrites should be placed on each signal conductor in the cable. The ferrite is used to isolate the signal conductors from the shield/ground of the cable antenna and reduces parasitic capacitance seen by the shield/ground. The choice of the ferrite is dependent upon the type of signal on each individual conductor. If the conductor is used to carry power, then a ferrite with a large dc current carrying capability should be used. If the conductor is used to carry high frequency digital signals, make sure that the ferrite does not block the high frequency component of these signals. Likewise if the conductor is used to carry high frequency analog signals, make sure that the ferrite does not filter the high frequency.

6.3. Cable Antenna Bill of Materials

The required bill of materials for the Figure 21 is shown in Table 15.

Table 15. Cable Antenna Bill of Materials

Designator	Description	Notes
L1	Tuning inductor, IND, 0603, SM, 120 nH, MURATA, LQW18ANR12J00D, Q>35	
C1	DC blocking capacitor, SM, 0402, X7R, 100 pF	
F1	Shunt Ferrite bead, FERRITEBEAD, SM, 0603, 470 Ω, 1 A, Murata, BLM18PG471SN1J	Rated dc current > max expected ground return current
F2	Series Ferrite bead, various types. Recommended ferrite for power lines: FERRITEBEAD, SM, 0603, 470 Ω, 1 A, Murata, BLM18PG471SN1J Recommended ferrite for signals: FERRITEBEAD, SM, 0603, 2.5 kΩ, 50 mA Murata, BLM18BD252DN1D	For power signals, make sure the rated dc current > max expected ground return current. For all other signals, make sure ferrite does not block/filter the high frequency component of the signals.

6.4. Cable Antenna Layout

Place the chip as close to the cable antenna as possible. This will minimize the trace length going to the cable antenna which will minimize the parasitic capacitance.

Place the shunt ferrite for the ground return current as close to the cable as possible. Putting the shunt ferrite for the ground return current close to the cable ensures that the ground return current has minimal loop which will reduce noise coupling. The series ferrites also should be put as close as possible to the cable. This will minimize the parasitic capacitance seen by the TXO/LPI pin.

6.5. Cable Antenna Design Checklist

- ☐ **Place** the chip as close as possible to the cable antenna to minimize parasitic capacitance.
- ☐ **Place** the tuning inductor, L1, as far away from the noise source as possible.
- ☐ **Make** sure that the shunt ferrite has a dc rating that exceeds the expected max ground return current of the cable.
- ☐ **Place** the shunt ferrite close to the cable.
- ☐ **Choose** series ferrite that is appropriate for each type of signal in the conductor.
- ☐ **Place** the series ferrite(s) close to the cable.

7. Whip Antenna for FM/WB Receiver on FMI (Si4707/3x Only)

A whip antenna is a typical monopole antenna, which is used in portable weather band receivers. It can also be used for SW applications. For additional details, see "10. Whip Antenna for SW Receive on AMI (Si4734/35 Only)" on page 45.

7.1. FM/WB Whip Antenna Design

A whip antenna is a monopole antenna with a stiff but flexible wire mounted vertically with one end adjacent to the ground plane.

There are various types of whip antenna including long non-telescopic metal whip antenna, telescopic metal whip antenna, and rubber whip antenna. Figure 22 shows the telescopic whip antenna.



Figure 22. Telescopic Whip Antennas

The whip antenna is capacitive, and its output capacitance depends on the length of the antenna (maximum length ~56 cm). At 56 cm length, the capacitance of the whip antenna ranges from 18 pF to 32 pF for the US FM band. The antenna capacitance is about 22 pF in the center of the US FM band (98 MHz).

7.2. FM/WB Whip Antenna Schematic

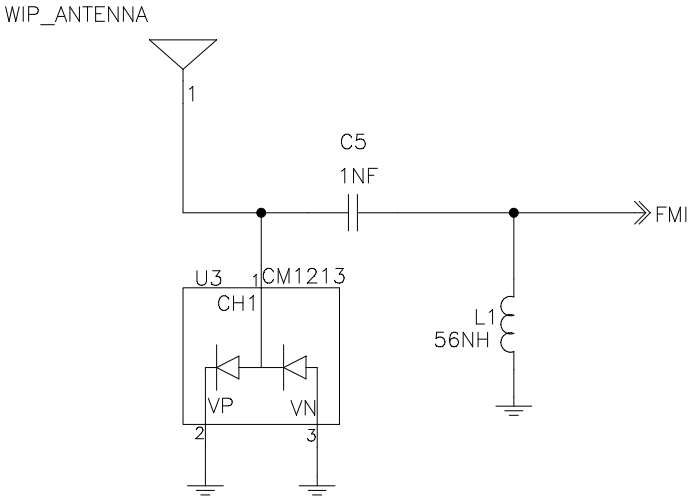


Figure 23. FM/WB Whip Antenna

L1 (56nH) is the matching inductor and it combines with the antenna impedance and the FMI impedance to resonate in the FM band.

C5 (1nF) is the ac coupling cap going to the FMI pin.

U3 is a required ESD diode since the antenna is exposed. The diode should be chosen with no more than 1pF parasitic capacitance, such as the California Micro Device CM1213.

7.3. FM/WB Whip Antenna Bill of Materials

Table 16. FM/WB Whip Antenna Bill of Materials

Designator	Description
WIP_ANTENNA	Whip Antenna
L1	Tuning Inductor, 0603, SM, 56 nH, MURATA, LQW18AN56nJ00D
C5	AC coupling capacitor, 1 nF, 10%, COG
U3	IC, SM, ESD DIODE, SOT23-3, California Micro Devices, CM1213-01ST

7.4. FM/WB Whip Antenna Layout

Place the chip as close as possible to the whip antenna. This will minimize the trace length between the device and whip antenna which in turn will minimize parasitic capacitance and the possibility of noise coupling. Place inductor L1 and the antenna connector together and as far from potential noise sources as possible and away from the I/O signals of the Si4736/37/38/39. Place the ac coupling capacitor, C5, as close to the FMI pin as possible. Place ESD diode U3 as close as possible to the whip antenna input connector for maximum effectiveness.

7.5. FM/WB Whip Antenna Design Checklist

- ☐ Maximize whip antenna length for optimal performance.
- ☐ Select matching inductor L1 with a Q of 15 or greater at 100MHz and minimal DC resistance.
- ☐ Select L1 inductor value to maximize resonance gain from FM frequency (88 MHz) to WB frequency (~162 MHz)
- ☐ Place L1 and whip antenna close together and as far from potential noise sources as possible to reduce capacitive and inductive coupling.
- ☐ Place the chip as close as possible to the whip antenna to minimize the antenna trace length. This reduces parasitic capacitance and hence reduces coupling into the antenna by noise sources. This recommendation must be followed for optimal device performance.
- ☐ Place ESD U3 as close as possible to the whip antenna for maximum effectiveness.
- ☐ Select ESD diode U3 with minimum capacitance.
- ☐ Place the ac coupling capacitor, C5, as close to the FMI pin as possible.

8. Ferrite Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only)

There are two types of antenna that will work well for an AM receiver: a ferrite loop antenna or an air loop antenna. A ferrite loop antenna can be placed internally on the device or externally to the device with a wire connection. When the ferrite loop antenna is placed internally on the device, it is more susceptible to picking up any noise within the device. When the ferrite loop antenna is placed outside a device, e.g., at the end of an extension cable, it is less prone to device noise activity and may result in better AM reception.

8.1. Ferrite Loop Antenna Design

Figure 24 shows an example of ferrite loop antennas. The left figure is the standard size ferrite loop antenna. It is usually used in products with a lot of space, such as desktop radios. The right figure is the miniature size of the loop antenna. It is usually used in small products where space is at a premium, such as cell phones. If possible, use the standard size ferrite loop antenna as it has a better sensitivity than the miniature one.

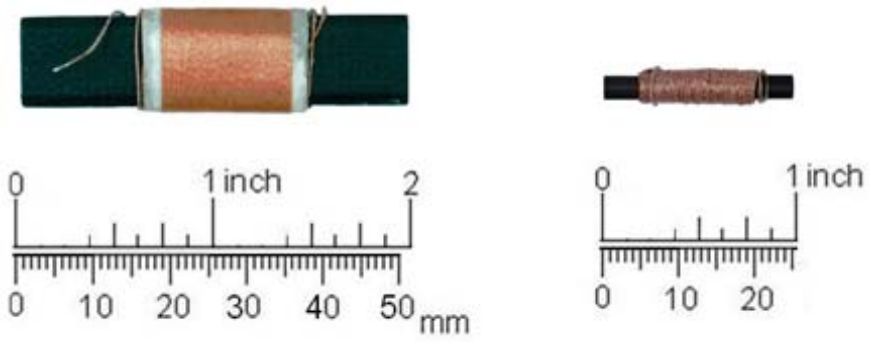


Figure 24. Standard and Miniature Ferrite Loop Antennas

A loop antenna with a ferrite inside should be designed such that the inductance of the ferrite loop is between 180 and 450 µH for the Si473x AM Receiver.

Table 17 lists the recommended ferrite loop antenna for the Si473x AM Receiver.

Table 17. Recommended Ferrite Loop Antenna

Part #	Diameter	Length	Turns	Ui	Type	Application
SL8X50MW70T	8 mm	50 mm	70	400	Mn-Zn	Desktop Radios
SL4X30MW100T	4 mm	30 mm	100	300	Ni-Zn	Portable Radios (MP3, Cell, GPS, …)
SL3X30MW105T	3 mm	30 mm	105	300	Ni-Zn	
SL3X25MW100T	3 mm	25 mm	110	300	Ni-An	
SL5X7X100MW70T	5 x 7 mm	100 mm	70	400	Mn-Zn	Desktop Radios

The following is the vendor information for the ferrite loop antennas:

Guangzhou Jiaxin Electronics Shenzhen Sales Office

email:sales@firstantenna.com

Web:www.firstantenna.com

8.2. Ferrite Loop Antenna Schematic

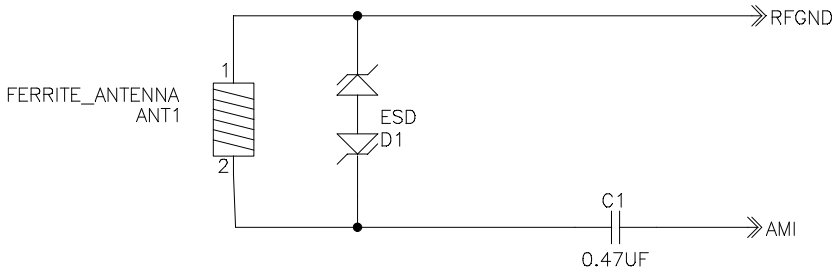


Figure 25. AM Ferrite Loop Antenna Schematic

C1 is the ac coupling cap going to the AMI pin and its value should be 0.47 µF.
D1 is an optional ESD diode if there is an exposed pad going to the AMI pin.

8.3. Ferrite Loop Antenna Bill of Materials

Table 18. Ferrite Loop Antenna Bill of Materials

Designator	Description	Note
ANT1	Ferrite loop antenna, 180–450 µH	
C1	AC coupling capacitor, 0.47 µF, 10%, Z5U/X7R	
D1	ESD diode, IC, SM, SOT23-3, California Micro Devices, CM1213-01ST	Optional; only needed if the there is any exposed pad going to the AMI pin.

8.4. Ferrite Loop Antenna Layout

Place the chip as close as possible to the ferrite loop antenna feedline. This will minimize the trace going to the ferrite antenna which in turn will minimize parasitic capacitance, and also will minimize the possibility of noise sources coupling to the trace.

The placement of the AM antenna is critical, since AM is susceptible to noise sources causing interference in the AM band. Noise sources can come from clock signals, switching power supply, and digital activities (e.g., MCU). When the AM input is interfaced to a ferrite loop stick antenna, the placement of the ferrite loop stick antenna is critical to minimize inductive coupling. Place the ferrite loop stick antenna as far away from interference sources as possible. In particular, make sure the ferrite loop stick antenna is away from signals on the PCB and away from even the I/O signals of the Si473x. Do not route any signal under or near the ferrite loop stick. Route digital traces in between ground plane for best performance. If that is not possible, route digital traces on the opposite side of the chip. This will minimize capacitive coupling between the plane(s) and the antenna.

To tune correctly, the total capacitance seen at the AMI input needs to be minimized and kept under a certain value. The total acceptable capacitance depends on the inductance seen by the Si4730/31 at its AM input. The acceptable capacitance at the AM input can be calculated using the formula shown in Equation 2.

$$C_{Total} = \frac{1}{(2\pi f_{max})^2 L_{effective}}$$

Equation 2. Expected Total Capacitance at AMI

Where:

C_{Total} = Total capacitance at the AMI input

$L_{effective}$ = Effective inductance at the AMI input

f_{max} = Highest frequency in AM band

The total allowable capacitance, when interfacing a ferrite loop stick antenna, is the effective capacitance resulting from the AMI input pin, the capacitance from the PCB, and the capacitance from the ferrite loop stick antenna. The inductance seen at the AMI in this case is primarily the inductance of the ferrite loop stick antenna. The total allowable capacitance in the case of an air loop antenna is the effective capacitance resulting from the AMI input pin, the capacitance of the PCB, the capacitance of the transformer, and the capacitance of the air loop antenna. The inductance in this case should also take all the elements of the circuit into account. The input capacitance of the AMI input is 8 pF. The formula shown in Equation 2 gives a total capacitance of 29 pF when a 300 µH ferrite loop stick antenna is used for an AM band with 10 kHz spacing, where the highest frequency in the band is 1710 kHz.

8.5. Ferrite Loop Antenna Design Checklist

- ☐ **Place** the chip as close as possible to the ferrite loop antenna feedline to minimize parasitic capacitance and the possibility of noise coupling.
- ☐ **Place** the ferrite loop stick antenna away from any sources of interference and even away from the I/O signals of the Si473x. Please make sure that the AM antenna is as far away as possible from circuits that switch at a rate which falls in the AM band (520–1720 kHz).
- ☐ **Place** optional component D1 if the antenna is exposed.
- ☐ **Select** ESD diode D1 with minimum capacitance.
- ☐ **Do Not Place** any ground plane under the ferrite loop stick antenna if the ferrite loop stick antenna is mounted on the PCB. The recommended ground separation is 1/4 inch or the width of the ferrite.
- ☐ **Route** traces from the ferrite loop stick connectors to the AMI input via the ac coupling cap C1 such that the capacitance from the traces and the pads is minimized.

9. Air Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only)

An air loop antenna is an external AM antenna (because of its large size) typically found on home audio equipment. An air loop antenna is placed external to the product enclosure making it more immune to system noise sources. It also will have a better sensitivity compared to a ferrite loop antenna.

9.1. Air Loop Antenna Design

Figure 26 shows an example of an air loop antenna.



Figure 26. Air Loop Antenna

Unlike a ferrite loop, an air loop antenna will have a smaller equivalent inductance because of the absence of ferrite material. A typical inductance is on the order of 10 to 20 µH. Therefore, in order to interface with the air loop antenna properly, a transformer is required to raise the inductance into the 180 to 450 µH range.

T1 is the transformer to raise the inductance to within 180 to 450 µH range. A simple formula to use is as follows:

$$L_{equivalent} = N^2 L_{AIRLOOP}$$

Typically a transformer with a turn ratio of 1:5 to 1:7 is good for an air loop antenna of 10–20 µH to bring the inductance within the 180 to 450uH range.

Choose a high-Q transformer with a coupling coefficient as close to 1 as possible and use a multiple strands Litz wire for the transformer winding to reduce the skin effect. All of this will ensure that the transformer will be a low loss transformer.

Finally consider using a shielded enclosure to house the transformer or using a torroidal shape core to prevent noise pickup from interfering sources.

A few recommended transformers are listed in Table 19.

Table 19. Recommended Transformers

	Transformer 1	Transformer 2	Transformer 3
Vendor	Jiaxin Dianzi	UMEC	UMEC
Part Number	SL9x5x4MWTF1	TG-UTB01527S	TG-UTB01526
Type	Surface Mount	Surface Mount	Through Hole
Primary Coil Turns (L1)	12T	10T	10T
Secondary Coil Turns (L2)	70T	55T	58T
Wire Gauge	ULSA / 0.07mm x 3	n/a	n/a
Inductance (L2)	380 µH ±10% @ 796 kHz	184 µH min, 245 µH typ @ 100 kHz	179 µH min, 263 µH typ @ 100 kHz
Q	130	50	75

The following is the vendor information for the above transformer:

Vendor #1:

Jiaxin Dianzi

Guangzhou Jiaxin Electronics Shenzhen Sales Office

email: sales@firstantenna.com

Web: www.firstantenna.com

Vendor #2:

UMEC USA, Inc.

Website: www.umec-usa.com

www.umec.com.tw

9.2. Air Loop Antenna Schematic

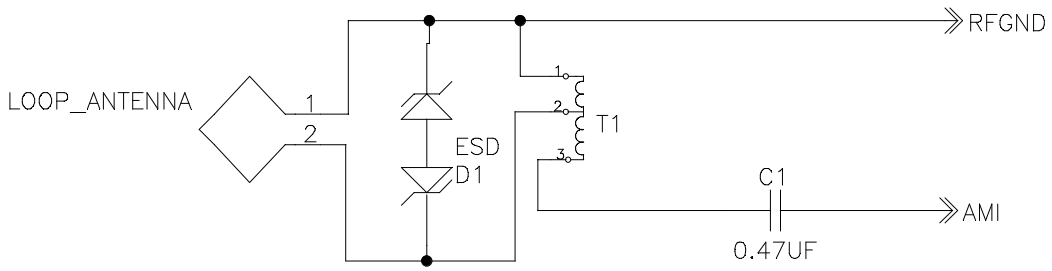


Figure 27. AM Air Loop Antenna Schematic

C1 is the ac coupling cap going to the AMI pin and its value should be 0.47 µF.

D1 is a required ESD diode since the antenna is exposed.

9.3. Air Loop Antenna Bill of Materials

Table 20. Air Loop Antenna Bill of Materials

Designator	Description	Note
LOOP_ANTENNA	Air loop antenna	
T1	Transformer, 1:6 turns ratio	
C1	AC coupling capacitor, 0.47 µF, 10%, Z5U/X7R	
D1	ESD diode, IC, SM, SOT23-3, California Micro Devices, CM1213-01ST	

9.4. Air Loop Antenna Layout

Place the chip and the transformer as close as possible to the air loop antenna feedline. This will minimize the trace going to the air loop antenna which in turn will minimize parasitic capacitance and the possibility of noise coupling.

When an air loop antenna with a transformer is used with the Si473x, minimize inductive coupling by making sure that the transformer is placed away from all sources of interference. Keep the transformer away from signals on the PCB and away from even the I/O signals of the Si473x. Do not route any signals under or near the transformer. Use a shielded transformer if possible.

9.5. Air Loop Antenna Design Checklist

- ☐ **Select** a shielded transformer or a torroidal shape transformer to prevent noise pickup from interfering sources
- ☐ **Select** a high-Q transformer with coupling coefficient as close to 1 as possible
- ☐ **Use** multiple strands Litz wire for the transformer winding
- ☐ **Place** the transformer away from any sources of interference and even away from the I/O signals of the Si473x. Please make sure that the AM antenna is as far away as possible from circuits that switch at a rate which falls in the AM band (520–1720 kHz).
- ☐ **Route** traces from the transformer to the AMI input via the ac coupling cap C1 such that the capacitance from the traces and the pads is minimized.
- ☐ **Select** ESD diode D1 with minimum capacitance.

10. Whip Antenna for SW Receive on AMI (Si4734/35 Only)

The whip antenna is a typical monopole antenna used in portable SW receivers. Additionally, it can be used for FM applications as covered in Section 6. This whip antenna schematic in this section will include the circuit for FM and ferrite loop antenna for AM. In-depth analysis of the whip antenna for FM is covered in Section 6, while in-depth analysis for the AM ferrite loop antenna is covered in Section 7.

10.1. SW Whip Antenna Design

The whip antenna is a monopole antenna with a stiff but flexible wire mounted vertically with one end adjacent to the ground plane. The whip antenna is capacitive and its output capacitance depends on the length of the antenna (maximum length ~56 cm). At 56 cm length, the capacitance of the whip antenna is about 12 pF at SW frequencies and approximately 22 pF at the center of the FM band.

There are various types of whip antennas including the long non-telescopic metal whip antenna, telescopic metal whip antenna, and rubber whip antenna. The following figure shows the rubber and the telescopic whip antenna.



Figure 28. Telescopic Whip Antenna

10.2. SW Whip Antenna Schematic

The following figure shows the SW whip antenna schematic along with the FM whip antenna interface and AM ferrite loop antenna interface.

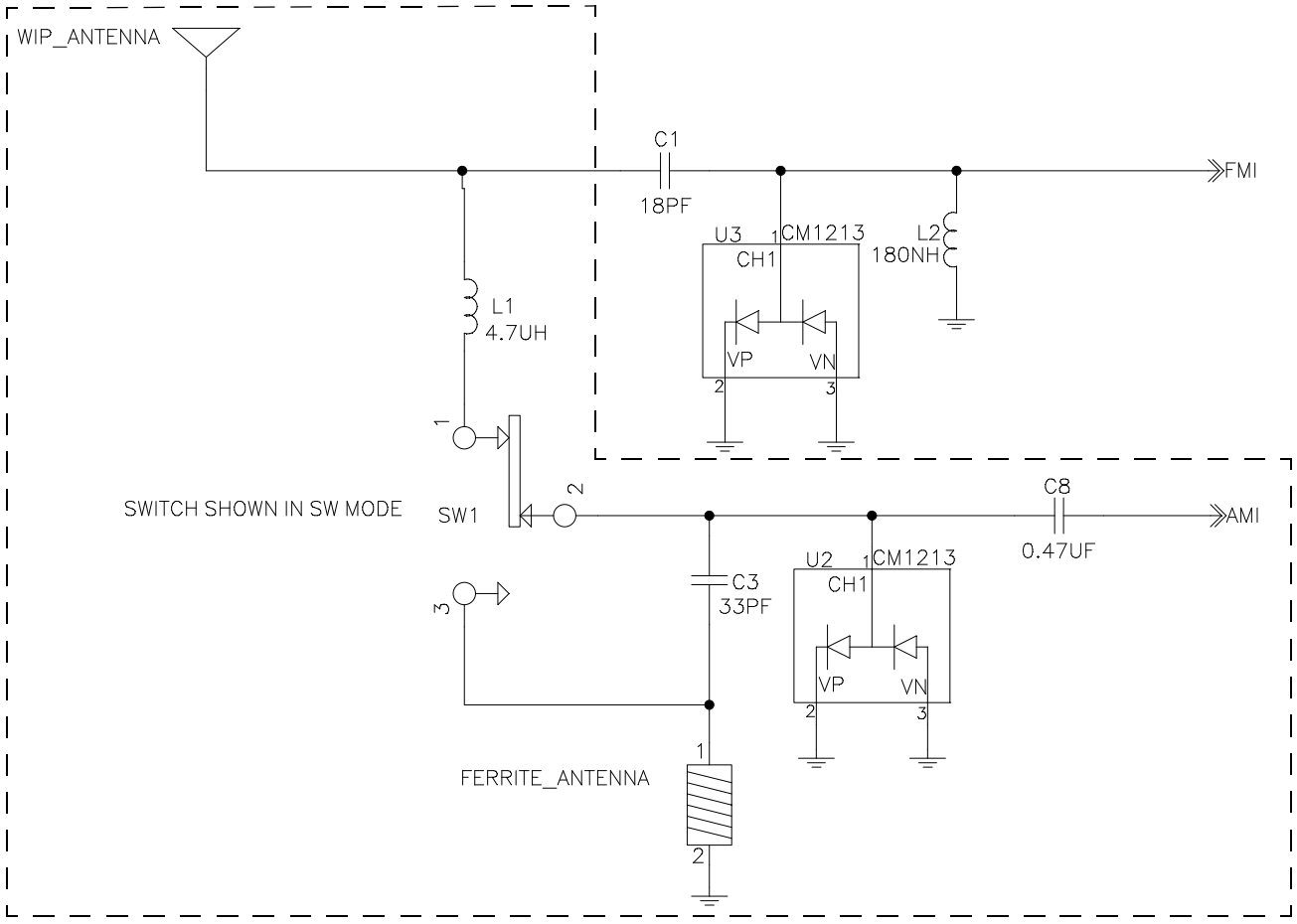


Figure 29. Whip Antenna Schematic plus FM Circuit and AM Ferrite Antenna

L1 (4.7 µH) is an inductor, which together with the Si4734/35 varactor (varactor set to 1) acts as a low-pass filter with peaking in the SW band. This inductor value is chosen assuming 12 pF capacitance of the whip antenna, 18 pF ac coupling cap (C1) to FMI, 7 pF AMI input capacitance (CAMI) and 8 pF parasitic capacitance on the board (CPAR). If either of these values changes, the inductor has to be tweaked to achieve peaking in the SW band (desired peaking at 23 MHz). The equivalent schematic model is shown below:

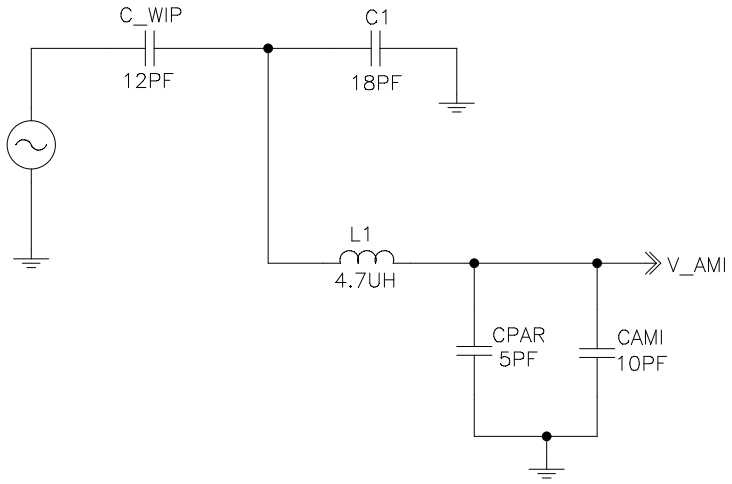


Figure 30. SW Whip Antenna Equivalent Model

FERRITE_ANTENNA is a ferrite loop antenna that has a dual purpose. In SW application, the FERRITE_ANTENNA serves as an inductor to ground, while in AM application it serves as an antenna. FERRITE_ANTENNA can be replaced with a 220 µH real inductor if AM is not used.

C8 (0.47 µF) is the ac coupling cap going to the AMI pin.

U2 and U3 are required ESD diodes since the antenna is exposed. The diodes should be chosen with no more than 1 pF parasitic capacitance, such as the California Micro Device CM1213. (U3 needs to be considered for FM application only)

C3 (33 pF) is a capacitor, which together with the ferrite antenna (or a 220 µH shunt inductor) provides a trap for the AM frequencies. Center frequency of the trap is calculated using the following equation:

$$f_{CTRAP} = \frac{1}{2 \times \pi \times \sqrt{(C3 \times L_{FERRITE})}}$$

C1 (18 pF) is the ac coupling cap going to FMI pin (Optional—for FM application only)

L2 (180 nH) is the tuning inductor for FM (Optional—for FM application only). This inductor together with the whip antenna capacitance (~22 pF at the center of FM band), 18 pF ac coupling cap (C1) and 5 pF typical FMI input capacitance (CFMI) resonates in the FM band. If either of the capacitance values changes, the inductor has to be tweaked to achieve peaking in the FM band (desired peaking at 100 MHz). The equivalent schematic to model is shown below:

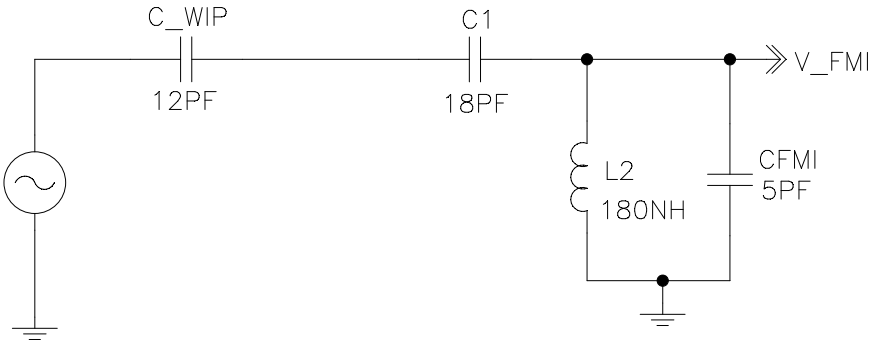


Figure 31. FM Whip Antenna Schematic Model

When switch SW1 is on the other position (pin 2 connected to pin 3), the whip antenna is disconnected and the ferrite acts as an antenna for AM. Go to Section 7 for in-depth analysis of AM ferrite loop antenna.

10.3. SW Whip Antenna Bill of Materials

Designator	Description	Notes
WIP_ANTENNA	Whip Antenna	
L1	Low Pass Filter Inductor, 1008, SM, 4.7 µH, COILCRAFT, 1008CS-472GLB	Q of 20 or greater at 25 MHz and minimal DC resistance.
SW1	SPDT Switch	Optional, only needed if the design requires switching between AM and SW. Not required for SW only applications.
C3	Capacitor, 33 pF, 5%, COG	
C8	AC coupling capacitor, 0.47 µF, 10%, Z5U/X7R	
FERRITE_ANTENNA	AM Antenna	Optional, can be replaced with a 220 µH shunt inductor for SW only applications
U2, U3	IC, SM, ESD DIODE, SOT23-3, California Micro Devices, CM1213-01ST	
C1	Capacitor, 18 pF, 5%, COG	Optional, only for FM
L2	Ind, 0603, SM, 180 nH, MURATA, LQW18ANR18J00D	Optional, only for FM

10.4. SW Whip Antenna Layout

Place the chip as close as possible to the whip antenna. This will minimize the trace length between the device and whip antenna which in turn will minimize parasitic capacitance and the possibility of noise coupling. Place the whip antenna away from any sources of interference and away from the I/O signals of the Si4734/35. Place the ac coupling capacitor, C8, as close to the AMI pin as possible. Place the ac coupling capacitor, C1, as close as possible to the FMI pin. Place ESD diodes U2 and U3 as close as possible to the whip antenna input connector for maximum effectiveness.

10.5. SW Whip Antenna Design Checklist

- ☐ Maximize whip antenna length for optimal performance.
- ☐ Select matching inductor L1 with a Q of 20 or greater at 25 MHz and minimal dc resistance.
- ☐ Select L1 inductor value to maximize signal strength across the FM band.
- ☐ Place L1 and whip antenna close together and as far from potential noise sources as possible to reduce capacitive and inductive coupling.
- ☐ Place the chip as close as possible to the whip antenna to minimize the antenna trace length. This reduces parasitic capacitance and hence reduces coupling into the antenna by noise sources. This recommendation must be followed for optimal device performance.
- ☐ Place ESD diodes U2 and U3 as close as possible to the whip antenna for maximum effectiveness.
- ☐ Select ESD diodes U2 and U3 with minimum capacitance.
- ☐ Place the ac coupling capacitor, C8, as close to the AMI pin as possible.
- ☐ Follow the design checklist in "8. Ferrite Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only)" on page 39 for the ferrite antenna to optimize AM performance (if AM is used in addition to SW).

APPENDIX A—FM RECEIVE HEADPHONE ANTENNA INTERFACE MODEL

The simplified circuit model for the headphone antenna interface shown in Figure 32, “Headphone Antenna and Matching Network Model”, and includes the headphone antenna, matching inductor, PCB and Si4700/01 LNA. This section discusses maximizing voltage gain across the FM band at the LNA input by varying headphone antenna and PCB parameters, and selecting the optimal matching inductor. It is very important to note that the performance is optimized by maximizing input voltage, not power.

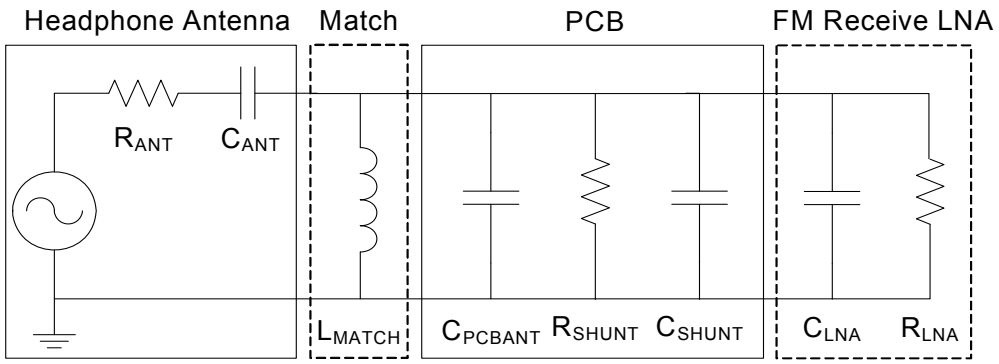


Figure 32. Headphone Antenna and Matching Network Model

R_{ANT} Antenna Resistance
C_{ANT} Antenna Capacitance
L_{MATCH} Inductance Match
C_{PCBANT} PCB Antenna Trace Capacitance
R_{SHUNT} Shunt Resistance of Ferrites
C_{SHUNT} Audio Conductor Shunt Capacitance
C_{LNA} LNA Capacitance
R_{LNA} LNA Resistance

The headphone antenna and matching network model can be further simplified and represented in the form of a parallel resonant RLC circuit as shown in Figure 33, “Parallel Resonant RLC Circuit Model”. In this simplified model the parallel resistance, R_P, represents the antenna resistance, R_{ANT}, the shunt resistance of ferrites on the left and right audio conductors, R_{SHUNT}, and the LNA resistance, R_{LNA}. The parallel capacitance, C_P, represents the antenna capacitance, C_{ANT}, PCB antenna trace capacitance, C_{PCBANT}, audio conductor shunt capacitance, C_{SHUNT}, and LNA capacitance, C_{LNA}.

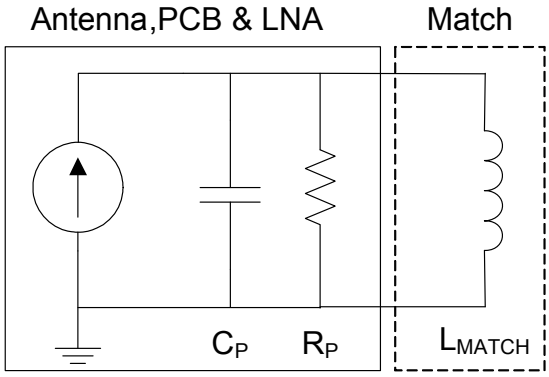


Figure 33. Parallel Resonant RLC Circuit Model

C_P = Parallel capacitance

R_P = Parallel resistance

L_{MATCH} = Inductance Match

L_{MATCH} is required to prevent the antenna from being shorted to ground at RF frequencies and to provide a path to ground at audio frequencies for return current from the headphone amplifier. Selecting the proper value of L_{MATCH} will maximize voltage gain across the FM band for optimal RF performance.

To maximize voltage gain across the FM band:

1. The value of R_P should be maximized to maximize the voltage at the LNA input.
2. The Q of the circuit should be minimized to maintain a flat response across the FM band.
3. The value of L_{MATCH} should be chosen such that the circuit resonates in the center of the FM band.

The value of R_P should be maximized to maximize the voltage at the LNA input. The parallel resistance, R_P, shown in Figure 33, “Parallel Resonant RLC Circuit Model” is defined as:

$$R_P = R_{LNA} \| R_{SHUNT} \| R_{ANT}^*$$

The LNA resistance, R_{LNA}, will range from 4 to 6 kΩ during normal operation. The shunt resistance, R_{SHUNT}, is the parallel addition of ferrite resistance on the left and right audio conductors, and other conductors for microphone audio, switching or other circuits, if applicable. R_{SHUNT} should be as large as possible to maximize RP. Specific recommendations for ferrite values can be found in Section "3.2. Headphone Antenna Schematic" on page 19. The antenna source resistance, R_{ANT}, will range from approximately 500 Ω for shorter antennas to several thousand ohms for longer antennas. R_{ANT}^* is the parallel circuit model for R_{ANT} near the resonant frequency, f, of the RLC circuit, and is approximated as:

$$R_{ANT}^* \approx R_{ANT}(Q_{ANT}^2 + 1) = R_{ANT}\left(\left(\frac{1}{2\pi f R_{ANT} C_{ANT}}\right)^2 + 1\right)$$

The antenna length should be 1.1 to 1.45 m, with optimal performance at 1.45 m to maximize R_{ANT}^*.

The Q of the parallel resonant RLC circuit shown in Figure 33, “Parallel Resonant RLC Circuit Model” is defined as:

$$Q_P = \frac{R_P}{\sqrt{\frac{L_P}{C_P}}}$$

The Q of the circuit should be minimized to maintain a flat response across the FM band. To minimize the Q of the circuit with a parallel resistance, R_P, that is maximized, the parallel capacitance, C_P, should be minimized and L_{MATCH} should be maximized.

The parallel capacitance, C_P, shown in Figure 33, “Parallel Resonant RLC Circuit Model” is defined as follows:

$$C_P = C_{PCBANT} \| C_{SHUNT} \| C_{LNA} \| C_{ANT}^*$$

The PCB antenna trace capacitance, C_{PCBANT}, is determined by the structure of the trace and is typically 3 to 4 pF per inch as a rule of thumb. The audio conductor shunt capacitance, C_{SHUNT}, is the parallel addition of PCB trace and component capacitance with respect to ground on the left and right audio conductors, and other conductors such as the microphone and switch if applicable. Both C_{PCBANT} and C_{SHUNT} should be as small as possible to minimize C_P. Specific schematic and layout recommendations minimizing C_{SHUNT} can be found in Section "3.2. Headphone Antenna Schematic" on page 19 and Section "3.4. Headphone Antenna Layout" on page 21. Specific layout recommendation for minimizing C_{PCBANT} can be found in Section “3.4. Headphone Antenna Layout”. The LNA capacitance, C_{LNA}, will range from 4 to 6 pF during normal operation. The antenna capacitance, C_{ANT}, will range from zero to several picofarads, depending on antenna length. C_{ANT}^* is the parallel circuit model of C_{ANT} near the resonant frequency, f, of the RLC circuit, and is approximated as follows:

$$C_{ANT}^* \approx C_{ANT}\left(\frac{Q_{ANT}^2}{Q_{ANT}^2 + 1}\right) \approx C_{ANT} \text{ ,for } Q \gg 1$$

For a given value of parallel capacitance C_P, the inductor value L_{MATCH} should be chosen such that the circuit resonates at the center of the FM band. The resonant frequency, f, of the parallel RLC circuit shown in Figure 33, “Parallel Resonant RLC Circuit Model” is defined as follows:

$$f = \frac{1}{2\pi \cdot \sqrt{L_{MATCH} C_P}}$$

Normally it is difficult to reliably measure all of the impedances required to calculate an optimal value for L_{MATCH}. An easier approach is to measure the system performance with different values of L_{MATCH} and choose the best values based on these measurements. Typical L_{MATCH} values range from 100 to 400 nH.

There are two test methods available for selecting the correct value of L_{MATCH} to properly tune the headphone antenna interface circuit. Both methods require injecting a test signal from a signal generator into the network through a source resistance, R_{TEST}, and adjusting the matching inductor, L_{MATCH}, to maximize the voltage at the LNA input at several points across the FM band. R_{TEST} should be 20 kΩ or larger to prevent loading of the resonant antenna circuit. Figure 34, “Parallel Resonant RLC Circuit Model Test Circuit” shows the parallel resonant RLC model test circuit required for both test methods.

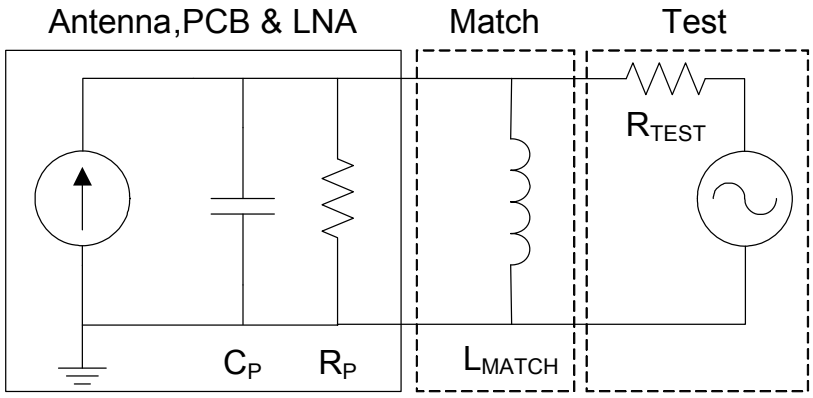


Figure 34. Parallel Resonant RLC Circuit Model Test Circuit

The first test method requires reading the received signal strength (RSSI) measured by the FM Receiver and the second method requires probing the LNA input with a low-capacitance FET probe and spectrum analyzer. The advantage of the RSSI method is that no external measurement equipment is required; however, a provision must be made for reading RSSI from the device. The advantage of the FET probe method is that reading the RSSI from the FM Receiver is not necessary, and measurement accuracy by using a spectrum analyzer and probe will be improved; however, excess capacitive loading of the FET probe may affect the measurement results. Care should be taken to select a probe with minimum capacitance when using this approach. Figure 35, “Headphone Antenna Example Test Signal Injection Frequency Response” shows the frequency response for four values of L_{MATCH} using the RSSI tuning method.

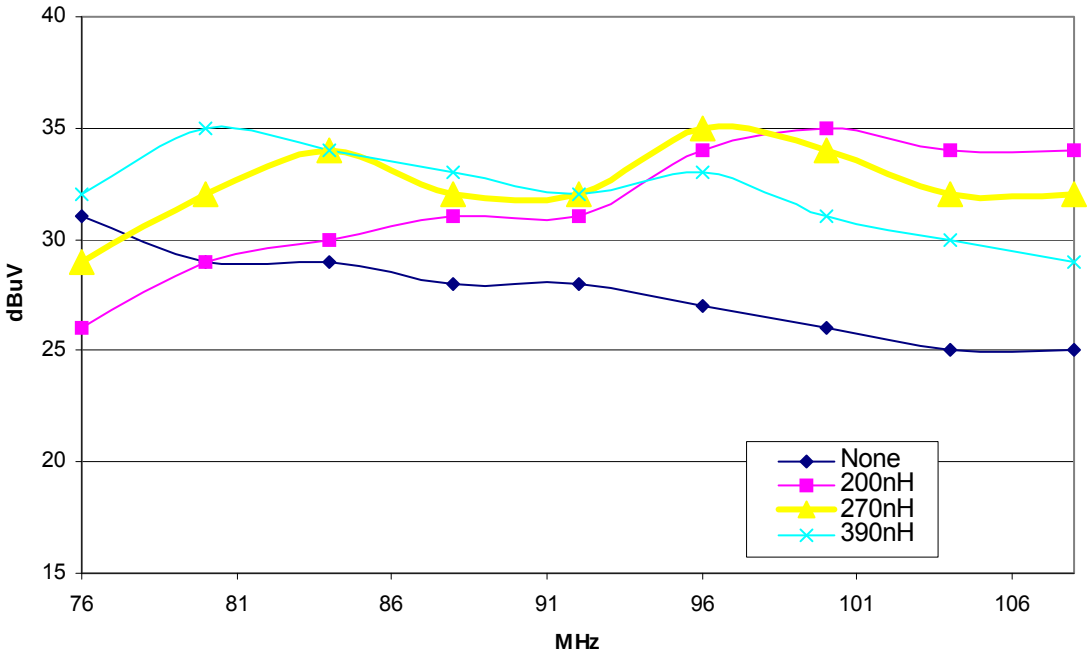


Figure 35. Headphone Antenna Example Test Signal Injection Frequency Response

It is clear from Figure 35, “Headphone Antenna Example Test Signal Injection Frequency Response” that the matching inductor, LMATCH, is preferred to no matching inductor, however, selecting the best value for LMATCH can be difficult by inspection.
Select the optimal value for LMATCH by following these guidelines:

1. The mean value of RSSI should be maximized.
2. The standard deviation of RSSI should be minimized.

Table 21 shows 270 nH is the optimal choice for LMATCH because it maximizes the mean RSSI and minimizes the RSSI standard deviation.

Table 21. Headphone Antenna Example Test Signal Injection Mean and Standard Deviation

	200 nH	270 nH	390 nH
Mean (dB)	31.5	32.4	32.1
Standard Deviation (dB)	3.0	1.7	1.9

APPENDIX B—FM TRANSMIT EMBEDDED ANTENNA INTERFACE MODEL

This application note describes the circuit required for interfacing the FM Transmitter to a short monopole PCB trace or wire antenna. It is strongly recommended that customers follow these schematic and layout recommendations in their designs to optimize transmitter radiated power and noise performance. A representation of a typical application is shown in Figure 36.

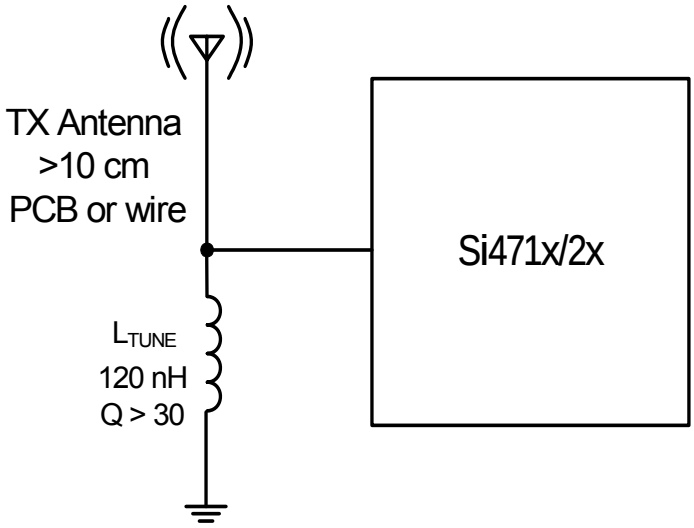


Figure 36. Typical Application

Electrically Short Vertical Monopole Antenna over an Infinitely Large Ground Plane

Radiated power from the FM Transmitter is maximized when using a long wire antenna, resonated with a low loss tuning inductor and positioned vertically above an infinitely large ground plane. A longer antenna performs better than a shorter one because radiated power increases with antenna length. Antennas should be 6 cm in length at a minimum to ensure that the FM Transmitter can deliver sufficient current to the antenna to meet maximum radiated power limits. A tuning inductor is required to resonate the antenna and should be low loss so that minimal current is dissipated in the inductor and delivered instead to the antenna. For practical purposes, the vertical monopole above an infinitely large ground plane is replaced with the requirement that the distance between the antenna and the ground and power planes be maximized.

In summary, to maximize antenna radiated power:

1. Maximize antenna length.
2. Maximize antenna current.
3. Maximize distance between the end of the antenna and the ground and power planes.

Electrically Short Vertical Monopole Antenna over an Infinitely Large Ground Plane

The model of an electrically short vertical monopole antenna over an infinitely large ground plane is shown in Figure 37. The term "electrically short" describes an antenna much shorter than one wavelength. Our focus will be on antennas 6 to 15 cm long, whereas at 100 MHz a wavelength is approximately 3 m.

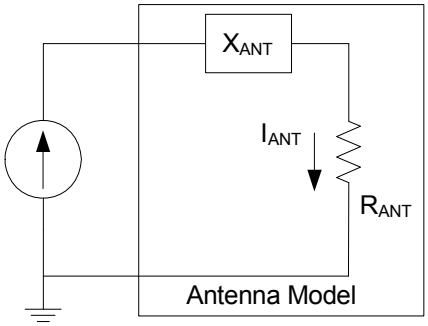


Figure 37. Model of an Electrically Short Vertical Monopole Antenna over an Infinitely Large Ground Plane

X_{ANT} = Antenna Reactance
R_{ANT} = Antenna Radiation Resistance
I_{ANT} = Antenna Current

The antenna radiation resistance models the antenna power dissipating element and is given as:

$$R_{ANT} = 20\left(\frac{2\pi fL}{c}\right)^2$$

, where L = meters, c = 3 x 10^8 m/s

The radiated power is given as:

$$P_{ANT} = I^2R_{ANT} = I^2 20\left(\frac{2\pi fL}{c}\right)^2$$

, where L = meters, c = 3 x 10^8 m/s

This equation shows that radiated power increases as the square of the antenna length and as the square of the delivered current. Every effort should therefore be made to maximize the length of the antenna and maximize antenna current. Minimizing circuit losses will maximize antenna current and can best be achieved by selecting a tuning inductor with a Q > 30. Note maximizing antenna current is equivalent to maximizing antenna voltage, a point that will be discussed later in this section.

The antenna reactance models the antenna capacitance for electrically short monopole antennas and is given as follows:

$$X_{ANT} = \frac{198c}{2\pi fL}$$

where L = meters, c = 3 x 10^8 m/s

This equation shows that antenna reactance decreases, and therefore capacitance increases, linearly with increasing antenna length. This capacitance should be kept in the range that can effectively be resonated by the tuning inductor. In practice this is easily achieved and is only mentioned for completeness.

The following section, " Electrically Short Monopole Interface Model", discusses the ranges of capacitance and inductance that should be expected.

As the name suggests, the electrically short vertical monopole antenna over an infinite ground plane assumes an antenna oriented vertically, or perpendicularly, to a ground plane that is infinite in size. As the antenna implementation deviates from this model, the effective antenna length decreases, resulting in a decrease in radiated power. As a practical matter, the geometry of the antenna and ground plane is dictated by physical dimensions of the device and the closest approximation to the ideal model is achieved by keeping the antenna as far away from ground and power planes as possible. This applies equally to a wire antenna and a PCB trace antenna. For brevity, the remainder of this document refers to this model as simply the "electrically short monopole."

Electrically Short Monopole Interface Model

The electrically short monopole model can be extended to incorporate the FM Transmitter output buffer capacitance, external tuning inductor and PCB capacitance as shown in Figure 38. At lengths below 1/2 wavelength, the antenna reactance X_{ANT} is capacitive and is replaced with capacitance C_{ANT}.

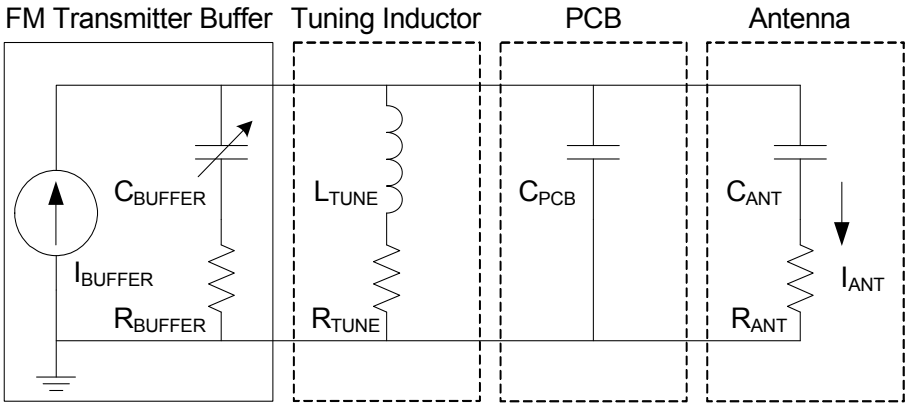


Figure 38. Simplified Model of the Electrically Short Monopole

C_{BUFFER} = Variable Tuning Capacitance (C_{TUNE}) + $C_{on\ chip\ parasitic}$
R_{BUFFER} = Variable Tuning Capacitor Series Resistance
L_{TUNE} = Tuning Inductance
R_{TUNE} = Tuning Inductor Series Resistance
C_{PCB} = PCB Parasitic Capacitance
C_{ANT} = Antenna Capacitance
R_{ANT} = Antenna Series Resistance

X_{ANT} is 1.6 kΩ for a 6 cm antenna at 100 MHz and is approximated as follows:

$$X_{ANT} = \frac{198c}{2\pi fL}$$

where L = 0.06, f = 100 MHz, c = 3 x 10^8

C_{ANT} is 1 pF at 100 MHz for X_{ANT} of 1.6 kΩ and is given as follows:

$$C_{ANT} = \frac{1}{2\pi f X_{ANT}}$$

RANT is 0.31 Ω for a 6 cm antenna at 100 MHz and is approximated as follows:

$$R_{ANT} = 20\left(\frac{2\pi fL}{c}\right)^2$$

, where L = 0.06, f = 100 MHz, c = 3 x 10^8

QANT is approximately 5000 for a 6 cm antenna at 100 MHz and is approximated as follows:

$$Q = \frac{X_{ANT}}{R_{ANT}}$$

The series resistances R_{BUFFER}, R_{TUNE} and R_{ANT} can be transformed to a parallel resistance over a narrow range of frequencies with the following equation if the Q of each of the reactive elements C_{BUFFER}, L_{TUNE}, and C_{ANT} are known:

$$R_P = R_S(Q^2 + 1)$$

The series inductance, L_{TUNE}, can be transformed to a parallel inductance over a narrow range of frequencies if the Q of L_{TUNE} is known with the following approximation:

$$L_P = L_S \frac{Q^2 + 1}{Q^2} \approx L_S$$

for Q >> 1

For sufficiently large Q, the inductive element is approximately the same for a series and parallel model.

The series capacitances C_{BUFFER} and C_{ANT} can be transformed to a parallel capacitance over a narrow range of frequencies if the Q of C_{BUFFER} and C_{ANT} are known with the following approximation:

$$C_P = C_S \frac{Q^2}{Q^2 + 1} \approx C_S$$

for Q >> 1

For sufficiently large Q, the capacitive element is approximately the same for a series and parallel model.

The circuit model shown in Figure 38 can be represented as a parallel resonant RLC circuit by replacing the series models with equivalent parallel models as shown in Figure 39. Note that only the values of the resistances change appreciably. The parallel model for each circuit element is indicated with an asterisk.

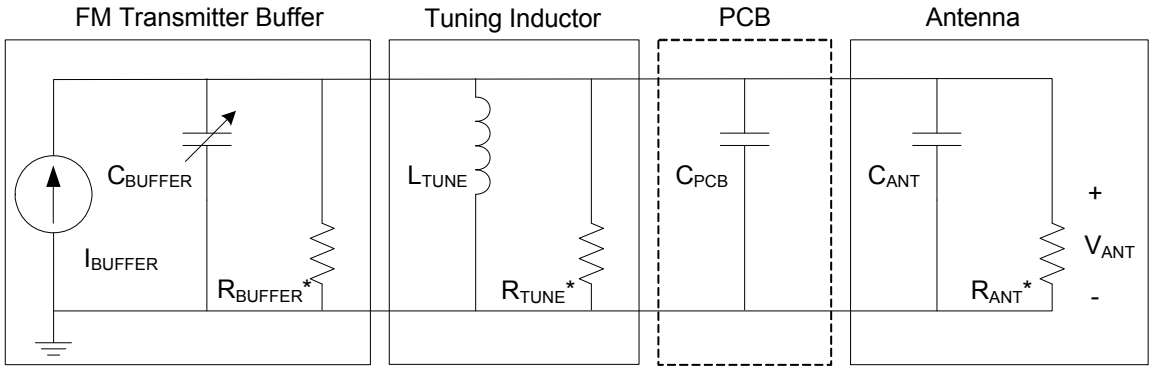


Figure 39. Equivalent RLC Model of the Electrically Short Vertical Monopole

C_{BUFFER} = Variable Tuning Capacitance (C_{TUNE}) + $C_{onchip\ parasitic}$
R_{BUFFER}* = Variable Tuning Capacitor Parallel Resistance
L_{TUNE} = Tuning Inductance
R_{TUNE}* = Tuning Inductor Parallel Resistance
C_{PCB} = PCB Parasitic Capacitance
C_{ANT} = Antenna Capacitance
R_{ANT}* = Antenna Parallel Resistance

C_{TUNE} will range from 0.25 to 47.75 pF.
$C_{onchip\ parasitic}$ is approximately 5 pF.

Therefore,

C_{BUFFER} will range from 5 to 53 pF.
R_{BUFFER}* will range from 1.2 to 1.6 kΩ
R_{TUNE}* will be approximately than 2.3 kΩ when L_{TUNE} is 120 nH with a Q > 30

C_{PCB} should be 4 pF or less to allow sufficient range for C_{BUFFER} to tune across the FM band.

C_{ANT} will be approximately 1 pF.

R_{ANT}* will be approximately 8 MΩ for Q_{ANT} = 5000 and is approximated as follows:

$$R_{ANT}^{*} = R_{ANT}(Q_{ANT}^{2} + 1)$$

Elements can be regrouped and the circuit model shown in Figure 39 can be simplified as shown in Figure 40.

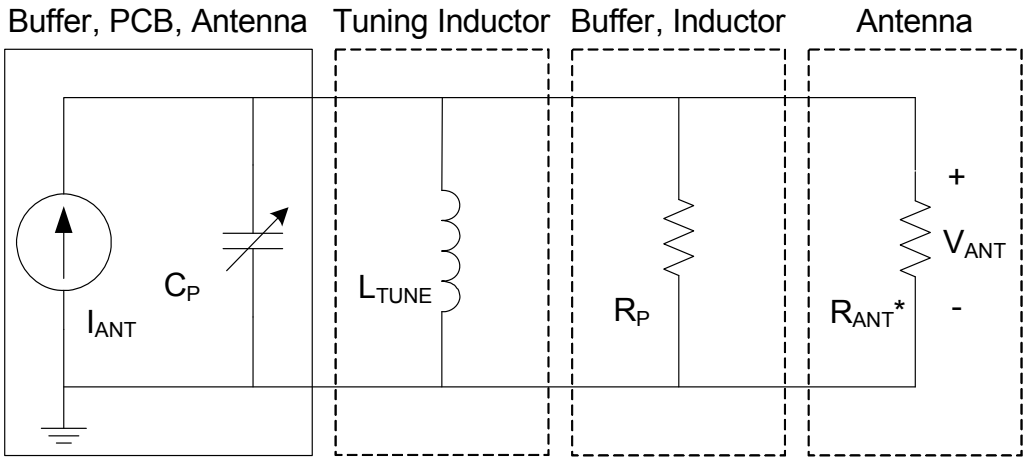


Figure 40. Simplified RLC Model of the Electrically Short Vertical Monopole

$C_P = C_{BUFFER} \parallel C_{PCB} \parallel C_{ANT}$
L_{TUNE} = Tuning Inductance
$R_P = R_{TUNE}^* \parallel R_{BUFFER}^*$
R_{ANT}^* = Antenna Parallel Resistance

C_P will range from 10 to 58 pF.

L_{TUNE} should be 120 nH with a Q > 30 to maintain R_{TUNE}^* > 2 kΩ

R_P will be approximately 800 Ω.

R_{ANT}^* will be approximately 8 MΩ.

Figure 40 shows that in order to maximize antenna voltage V_{ANT}, and therefore radiated power, R_P should be maximized by choosing an inductor with a Q > 30 and R_{ANT} should be maximized by maximizing the antenna length.

Choosing Tuning Inductance

The recommended value for the tuning inductance is 120 nH and it is based on a typical total parasitic capacitance of 10 pF. In the event where the parasitic capacitance differs quite significantly from this number, it may be necessary to make L_{TUNE} lower or higher.

The total capacitance needed to tune to a particular frequency is given with this formula:

$$\omega = \frac{1}{L.C}$$

$$(2\pi f)^2 = \frac{1}{L.Ctotal}$$

Actual CTUNE needed on the chip then can be calculated by subtracting all of the parasitic capacitance including the Si471x on chip parasitic capacitance, PCB capacitance, and antenna capacitance.

CTUNE = Ctotal – Conchip parasitic – CPCB – CANT

The actual CTUNE needed then has to be well within the available range of CTUNE, which is:

CTUNE min = 0.25 pF

CTUNE max = 47.75 pF

CTUNE can be read from the chip and the range will be 1–191. Each number represents 0.25 pF, so the range is 0.25 to 47.75 pF.

Example 1

Conchip parasitic = 5 pF

CPCB = 4 pF

CANT = 1 pF

Ctotal parasitic capacitance = 5 + 4 + 1 = 10 pF

LTUNE = 120 nH

Desired FM frequency = 76–108 MHz

At 76 MHz > Ctotal = 37 pF, CTUNE = 37 – 10 = 27 pF

At 108 MHz > Ctotal = 18 pF, CTUNE = 18 – 10 = 8 pF

In this case at the FM frequency of interest (76 MHz to 108 MHz), the needed CTUNE range (8–27 pF) is within the available CTUNE range on the chip (0.25–47.75 pF) which means that the 120 nH inductor value is a good choice.

Example 2

Conchip parasitic = 5 pF

CPCB = 10 pF

CANT = 1 pF

Ctotal parasitic capacitance = 5 + 10 + 1 = 16 pF

At 76 MHz > Ctotal = 37 pF, CTUNE = 37 – 16 = 21 pF

At 108 MHz > Ctotal = 18 pF, CTUNE = 18 – 16 = 2 pF

In this case at 108 MHz even though CTUNE needed (2 pF) is still higher than the min CTUNE (0.25 pF), it is not advisable to keep LTUNE at 120 nH. Variation in the parasitic capacitance from the PCB and different components may result in the CTUNE needed to be equal or less than 0.25 pF. It is advisable then to lower the LTUNE value to 100 nH.

Solution

Make LTUNE = 100 nH

At 76 MHz > Ctotal = 44 pF, CTUNE = 28 pF

At 108 MHz > Ctotal = 22 pF, CTUNE = 6 pF

In this case the needed CTUNE range (6–28 pF) is well within the available CTUNE (0.25 to 47.75 pF).

APPENDIX C—AM FERRITE LOOP STICK ANTENNA INTERFACE MODEL

This appendix describes how to interface a ferrite loop stick antenna to the AM receiver input. The application note begins with an overview of AM ferrite loop antennas followed by the interface to a ferrite loop stick antenna. The last section of the application note presents designers with guidelines for designing ferrite loop stick antennas.

AM Ferrite Loop Stick Antenna Overview

An AM antenna works on the basis of Faraday's Law. Faraday's law dictates that a varying magnetic field through a wire loop induces an EMF (Electro-Motive Force) in the loop and is expressed as:

$$EMF = -\frac{d\varphi}{dt}$$

Where ϕ = magnetic flux.
The negative sign in Equation indicates that the current generated in the loop is in a direction which generates a magnetic field that opposes the magnetic field causing the induced EMF. An AM loop antenna is made of a single loop or many loops of a conducting material wrapped around an air core or a ferrite core. In the case of radio transmissions, the induced voltage represents the AM signal being transmitted by a radio station as electromagnetic waves.

A ferrite loop stick antenna is a coil wrapped around a ferrite core. Ferrite is a ferromagnetic material which does not display any magnetic properties till it is excited by a magnetic field. A ferrite multiplies the applied magnetic field by a factor that is known as the effective permeability of the ferrite material. Since the permeability of a ferrite material is orders of magnitude higher than air, the voltage induced in a loop antenna wound around a ferrite core is also orders of magnitude greater than the voltage that would be induced in an air loop antenna of the same size. All ferrite loop stick antennas have an inductance associated with them and this can be expressed as:

$$L_{ant} = \frac{k\mu_r\mu_o N^2 A}{l_r}$$

Equation 3. Trap Frequency Calculation

Where:

L_{ant} = Antenna inductance

k = Permeability modifier constant

μ_r = Relative permeability of ferrite rod

μ_o = Permeability of air/free space

N = Number of turns in coil

A = Cross-sectional area of ferrite rod

l_r = Length of ferrite rod

In Equation 3, μ_r is the relative permeability of the ferrite rod. The rod dimensions play an important role in determining the relative permeability of the rod. The permeability modifier constant is based on the ratio of ferrite rod length to the coil length. The relative permeability of the rod and the permeability modifier constant are combined together to yield the effective permeability of the antenna and are used to reduce Equation 3 to the following:

$$L = \frac{\mu_o \mu_e N^2 A}{l_r}$$

Equation 4. Ferrite Loop Inductance Calculation

Where μ_e = Effective relative permeability of antenna

Signal receiving capability of an antenna is defined by its antenna height. Antenna height of a loop antenna is derived from Equation by replacing the flux with the inner product of the magnetic field and the surface area of the coil and is expressed as follows:

$$h_e = \frac{2\pi NA\mu_e}{\lambda}$$

Equation 5. Simplified Ferrite Loop Inductance Calculation

Where:

h_e = Effective antenna height

N = Number of turns in coil

A = Cross-sectional area of ferrite rod

μ_e = Relative effective permeability of antenna

λ = Wavelength of signal

Equation 6 is used to rewrite the antenna height in terms of antenna inductance as follows:

$$h_e = \frac{2\pi f L_{ant} l_r}{c\mu_o N}$$

Equation 6. Effective Antenna Height Calculation

Where:

f = Signal frequency

L_{ant} = Antenna inductance

l_r = Length of ferrite rod

c = speed of light

μ_o = Permeability of air/free space

N = Number of turns in coil

Equation 6 tells us the relationship between antenna height and the factors that affect antenna height. The induced voltage can be calculated simply by multiplying the antenna height with the electric field strength for an AM signal (denoted by E) with dimensions of Volts/unit length. Equation 7 expresses this relationship:

$$V_{induced} = E \times \frac{2\pi f L_{ant} l_r}{c\mu_o N}$$

Equation 7. Induced Voltage Calculation

AM Ferrite Loop Stick Antenna Interface

The front-end of the AM RX is an LC tuned circuit, the purpose of which is to gain the received signal from any tuned AM station. The LC tuned circuit comprises of an inductance which comes form the attached antenna and a variable capacitance that is provided by a tunable capacitor inside the AM RX. Figure 41 shows the model circuit for the front-end of a loop antenna attached to the AM RX.

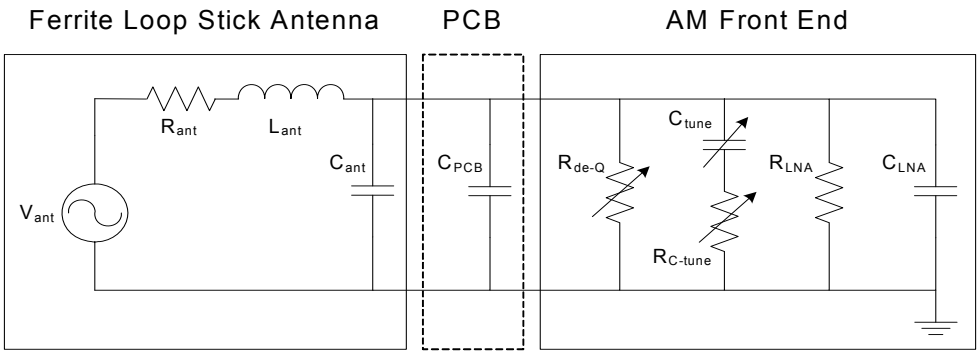


Figure 41. AM Front-End with Ferrite Loop Antenna

The purpose of the variable tuning capacitor (C_{tune}) is to resonate the front-end such that the resonance frequency is the same as the frequency of the AM station one wants to listen to. In order to tune to a specific station, the C_{tune} capacitor is adjusted such that the front-end achieves resonance and the voltage received from the antenna is gained up before entering the AM front end. C_{tune} also has a stray resistance ($R_{C\text{-}tune}$) associated with it which affects the Q of the tuning capacitor. The Q of the on-chip tuning capacitor is given as follows:

$$Q_{C-tune} = \frac{1}{\omega_o R_{C-tune} C_{tune}}$$

Equation 8. On-chip Capacitor Q Calculation

Where:

$Q_{C\text{-}tune}$ = Quality factor of on-chip tuning capacitor

ω_o = Resonance frequency

$R_{C\text{-}tune}$ = Stray resistance of on-chip tuning capacitor

C_{tune} = Capacitance of on-chip tuning capacitor

The reason the stray resistance is shown as a variable resistance in Figure 41 is because the on-chip capacitor is implemented as a bank of capacitors and as capacitors are switched in or out, the stray resistance also changes.

The purpose of the variable resistor ($R_{De\text{-}Q}$) in the front-end is to reduce the gain of the front-end circuit. Being able to reduce gain is helpful if the received signal is too strong and does not need to be gained by the front-end circuit. It will be shown later that the gain of the circuit at resonance is equal to Q of the circuit and is directly proportional to the total resistance between the AM input and ground. Since the variable resistor ($R_{De\text{-}Q}$) is part of the total resistance between the AM input and ground and is the only variable resistor, it can be stated that the gain of the front-end can be controlled by the De-Q resistor.

C_{PCB} is the capacitance associated with the PCB. R_{LNA} and C_{LNA} are the impedance and the capacitance from the Low-Noise Amplifier (LNA). The circuit in Figure 41 can be reduced to a simpler circuit by assuming that the circuit is tuned to a certain AM station and the front-end is in resonance, which allows the conversion of R_{ant} to a parallel resistance and $R_{C\text{-}tune}$ to a parallel capacitance. The new circuit is shown in Figure 42:

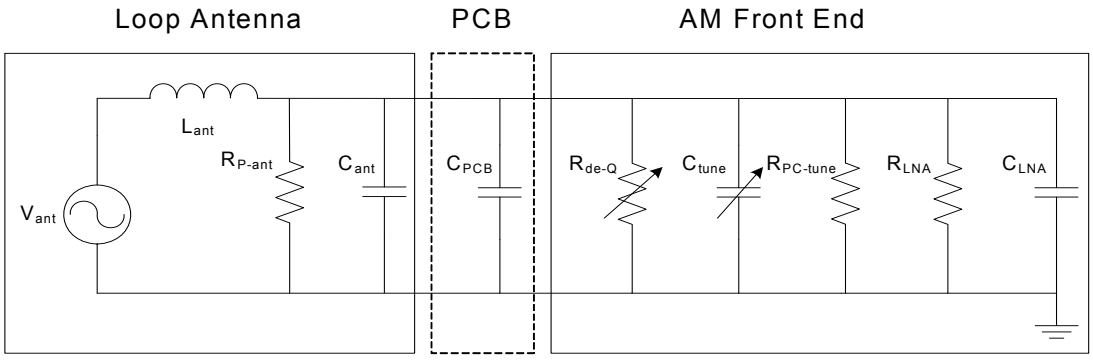
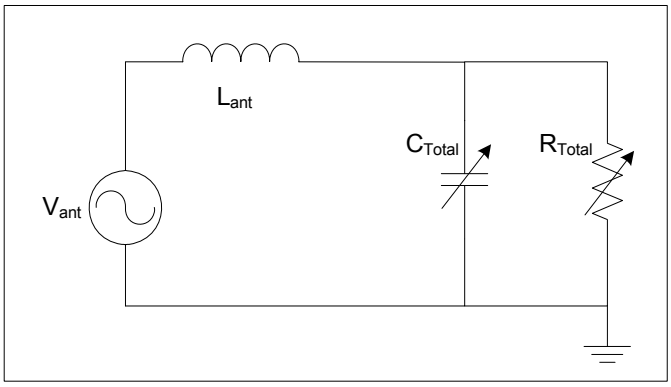


Figure 42. AM Front-end with Series Antenna and On-chip Resistances Converted to Parallel Resistances

The circuit can be further simplified because at resonance R_{De-Q} and C_{tune} are fixed and the resistance and capacitances can be lumped together. The new circuit is shown in Figure 43.



Where:

$1/R_{Total} = 1/R_{P-ant} + 1/R_{de-Q} + 1/R_{PC-tune} + 1/R_{LNA}$

$C_{Total} = C_{ant} + C_{PCB} + C_{tune} + C_{LNA}$

Figure 43. Circuit Elements have been Lumped Together to Simplify Circuit Further

Analyzing this circuit is a mathematical exercise and is not covered in this document. It can be easily shown that the resonant frequency for this circuit is equal to the following:

$$\omega_{resonance} = \frac{1}{\sqrt{L_{ant}C_{Total}}}$$

Equation 9. Resonant Frequency Calculation

The Q of the circuit at resonance can be calculated by finding the magnitude of the transfer function and substituting ω with $\omega_{resonance}$. The Q of the circuit at resonance is expressed as follows:

$$Q_{circuit} = R_{Total}\sqrt{\frac{L_{ant}}{C_{Total}}}$$

Equation 10. Overall Circuit Q Calculation

Document Change List

Revision 0.3 to Revision 0.4

- Updated "2. Si47xx 3x3 mm QFN Schematic and Layout" on page 5 with latest recommendation on schematic, layout and design guidelines.
- Added "6. Cable Antenna for FM Transmit on TXO and Receive on LPI (Si4704/05/06/1x/2x Only)" on page 34.
- Added "7. Whip Antenna for FM/WB Receiver on FMI (Si4707/3x Only)" on page 37.
- Updated "8. Ferrite Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only)" on page 39 with ferrite loop antenna pictures, recommendation and vendor information.
- Updated "9. Air Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only)" on page 42 with air loop antenna pictures, transformer recommendation and vendor information.
- Added "10. Whip Antenna for SW Receive on AMI (Si4734/35 Only)" on page 45.

Revision 0.4 to Revision 0.5

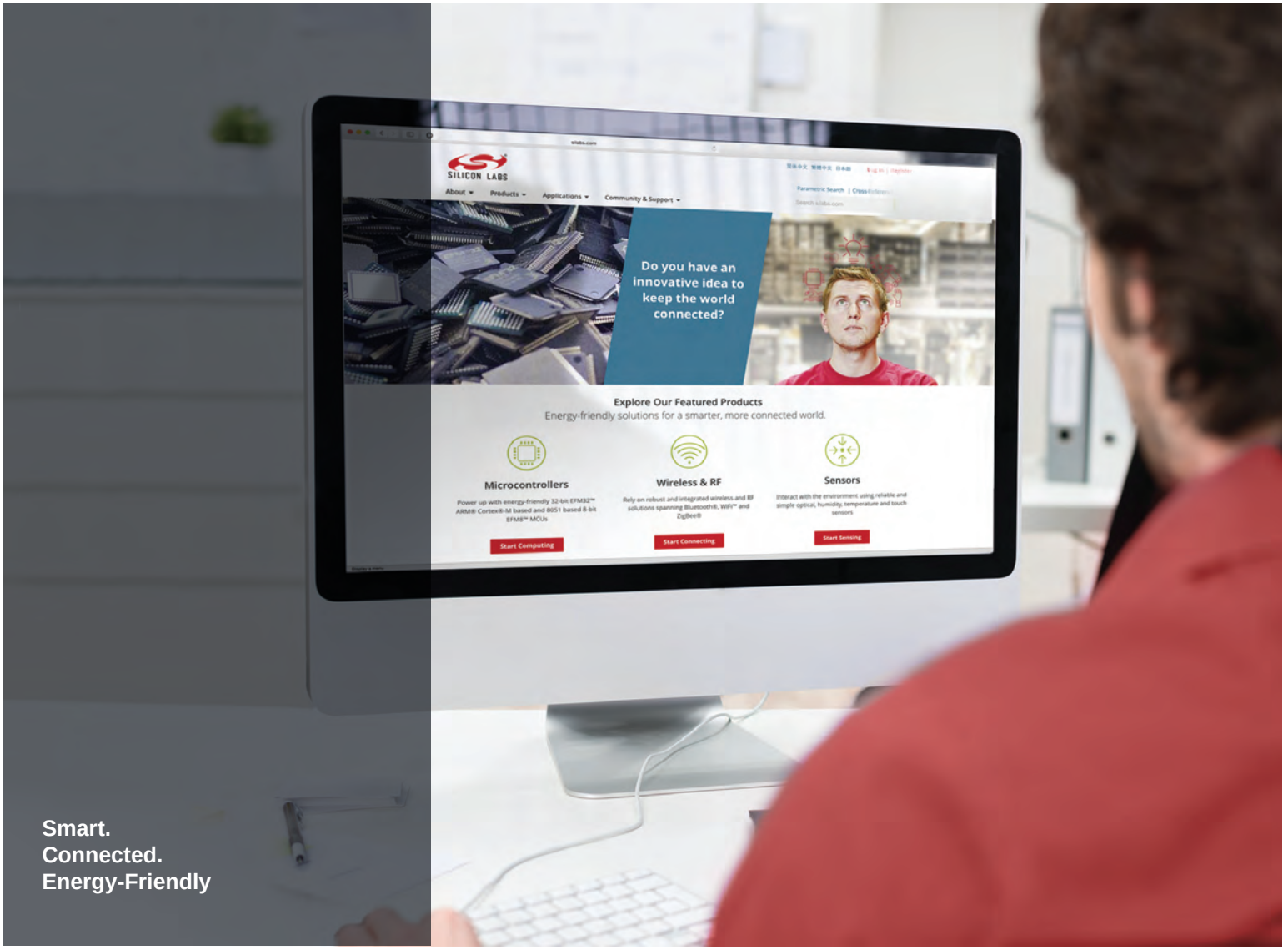
- Updated "2. Si47xx 3x3 mm QFN Schematic and Layout" on page 5 with latest recommendation on schematic, layout and design guidelines.
- Added "4. Cable Antenna for FM Receive on FMI (Si470x/2x/3x/8x Only)" on page 22.
- Updated "5. Embedded Antenna for FM Transmit on TXO and Receive on LPI (Si4704/05/06/1x/2x Only)" on page 25.
- Added "6. Cable Antenna for FM Transmit on TXO and Receive on LPI (Si4704/05/06/1x/2x Only)" on page 34.
- Added "7. Whip Antenna for FM/WB Receiver on FMI (Si4707/3x Only)" on page 37.
- Updated "8. Ferrite Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only)" on page 39 with vendor information.
- Updated "9. Air Loop Antenna for AM/LW Receive on AMI (Si4730/31/34/35/36/37 Only)" on page 42 with vendor information.

Revision 0.5 to Revision 0.6

- Added Note to “2.1. Si47xx 3x3 mm Design” and updated pin names and pin numbers on page 5.

Revision 0.6 to Revision 0.8

- Removed Note from Section “2.1. Si47xx 3x3 mm Design”.



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

Disclaimer
Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information
Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem ®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

SILICON LABS®

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com

NOTES: