2Gb (x16) DDR2 SDRAM

SEPTEMBER 2012

FEATURES

- Clock frequency up to 333MHz (667 MT/s Data Rate)
- 8 internal banks for concurrent operation
- 4-bit prefetch architecture
- Programmable CAS Latency: 3, 4, 5, 6 and 7
- Programmable Additive Latency: 0, 1, 2, 3, 4, 5 and 6
- Write Latency = Read Latency-1
- Programmable Burst Sequence: Sequential or Interleave
- Programmable Burst Length: 4 and 8
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 7.8 µs (8192 cycles/64 ms)
- OCD (Off-Chip Driver Impedance Adjustment)
- ODT (On-Die Termination)
- Weak Strength Data-Output Driver Option
- Bidirectional differential Data Strobe (Single-ended data-strobe is an optional feature)
- On-Chip DLL aligns DQ and DQs transitions with CK transitions
- DQS# can be disabled for single-ended data strobe
- Differential clock inputs CK and CK#
- VDD and VDDQ = 1.8V ± 0.1V
- PASR (Partial Array Self Refresh)
- SSTL_18 interface
- tRAS lockout supported
- Operating temperature:
  Commercial (T_A = 0°C to 70°C ; T_C = 0°C to 85°C)
  Industrial (T_A = -40°C to 85°C; T_C = -40°C to 95°C)[2]
  Automotive, A1 (T_A = -40°C to 85°C; T_C = -40°C to 95°C)[2]
  Automotive, A2 (T_A = -40°C to 105°C; T_C = -40°C to 105°C)[2]

OPTIONS

- Configuration:
  - 128Mx16 (two stacked 16M x 8 x8 banks)
- Package:
  - 84-ball FBGA

ADDRESS TABLE

Parameter	128Mx16
Row Addressing	A0-A13
Column Addressing	A0-A9
Bank Addressing	BA0-BA2
Precharge Addressing	A10

Clock Cycle Timing

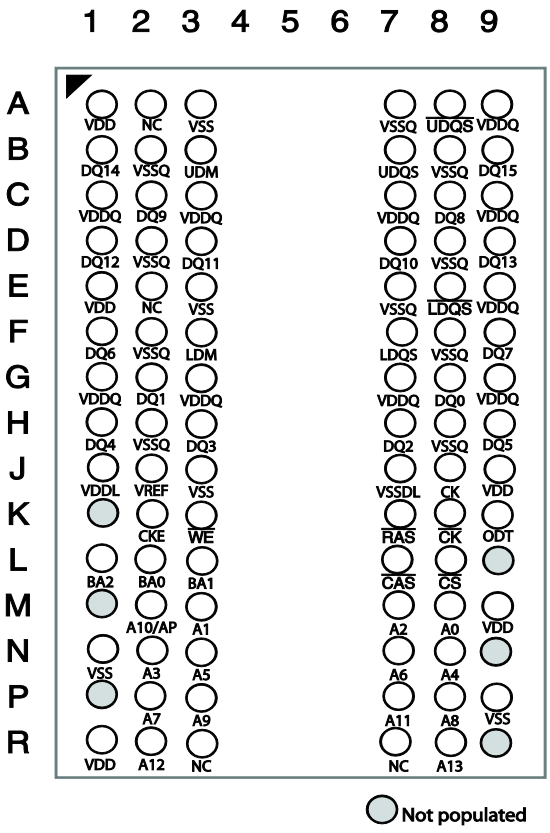
	-37C	-3D	Units
Speed Grade	DDR2-533C	DDR2-667D	
CL-tRCD-tRP	4-4-4	5-5-5	tCK
tCK (CL=3)	5	5	ns
tCK (CL=4)	3.75	3.75	ns
tCK (CL=5)	3.75	3	ns
tCK (CL=6)	3.75	3	ns
tCK (CL=7)	3.75	3	ns
Frequency (max)	266	333	MHz

Note:
1. The -37C device specifications is shown for reference only.
2. Please contact ISSI for availability of Automotive parts.

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a.) the risk of injury or damage has been minimized;
b.) the user assume all such risks; and
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DDR2 SDRAM (128Mx16) BGA Ball-out (Top-View) (10.5mm x 13.5mm Body, 0.8mm pitch)



Symbol	Description
CK, CK#	Input clocks
CKE	Clock enable
CS#	Chip Select
RAS#,CAS#,WE#	Command control inputs
A[13:0]	Address
BA[2:0]	Bank Address
DQ[15:0]	I/O
UDQS, UDQS#	Upper Byte Data Strobe
LDQS, LDQS#	Lower Byte Data Strobe
UDM, LDM	Input data mask
VDD	Supply voltage
VSS	Ground
VDDQ	DQ power supply
VSSQ	DQ ground
VREF	Reference voltage
VDDL	DLL power supply
VSSDL	DLL ground
ODT	On Die Termination Enable
NC	No connect

Note:
VDDL and VSSDL are power and ground for the DLL.

Functional Description

Power-up and Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

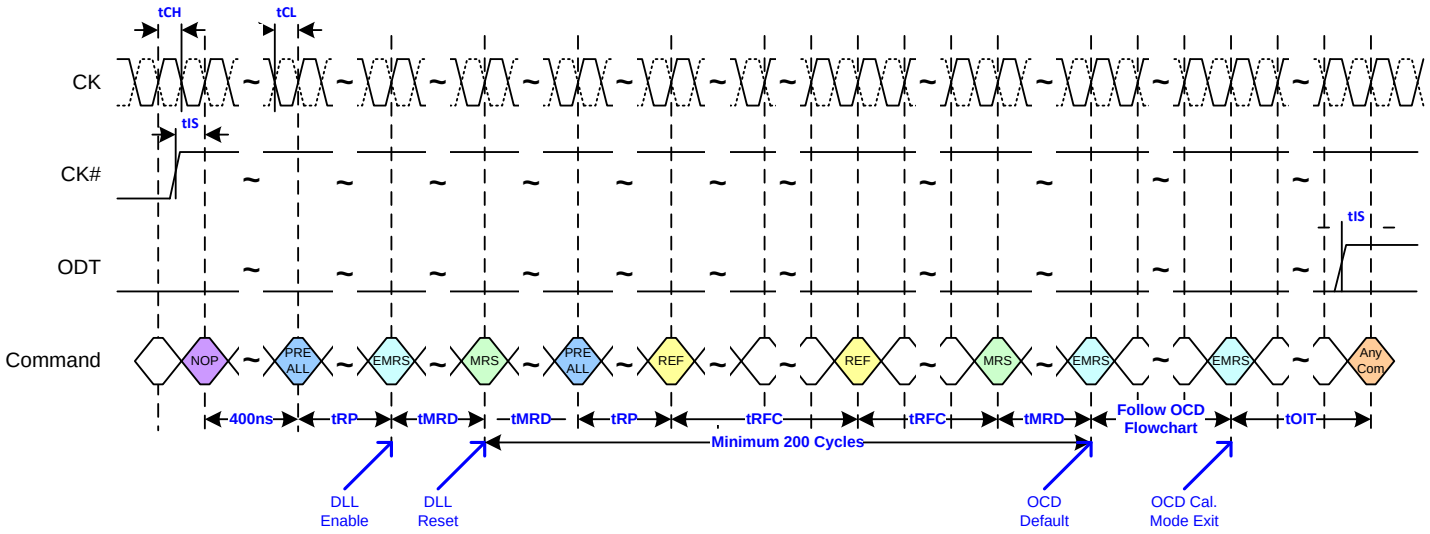
Power-up and Initialization Sequence

The following sequence is required for Power-up and Initialization.

1. Either one of the following sequence is required for Power-up:
   A. While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT[1] at a LOW state (all other inputs may be undefined.) The VDD voltage ramp time must be no greater than 200 ms from when VDD ramps from 300 mV to VDD(Min); and during the VDD voltage ramp, |VDD-VDDQ| ≥ 0.3 V. Once the ramping of the supply voltages is complete (when VDDQ crosses VDDQ(Min)), the supply voltage specifications provided in the table *Recommended DC Operating Conditions (SSTL_1.8)*, prevail.
      – VDD, VDDL and VDDQ are driven from a single power converter output, AND
      – VTT is limited to 0.95V max, AND
      – VREF tracks VDDQ/2, VREF must be within ± 300mV with respect to VDDQ/2 during supply ramp time.
      – VDDQ ≥ VREF must be met at all times
   B. While applying power, attempt to maintain CKE below 0.2 x VDDQ and ODT[1] at a LOW state (all other inputs may be undefined, voltage levels at I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, VDD ≥ VDDL ≥ VDDQ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete, which is when VDDQ crosses VDDQ min. Once the ramping of the supply voltages is complete, the supply voltage specifications provided in the table *Recommended DC Operating Conditions (SSTL-1.8)*, prevail.
      – Apply VDD/VDDL before or at the same time as VDDQ.
      – VDD/VDDL voltage ramp time must be no greater 200 ms from when VDD ramps from 300 mV to VDD(Min) .
      – Apply VDDQ before or at the same time as VTT.
      – The VDDQ voltage ramp time from when VDD(Min) is achieved on VDD to the VDDQ(Min) is achieved on VDDQ must be no greater than 500 ms.
2. Start clock and maintain stable condition.
3. For the minimum of 200 µs after stable power (VDD, VDDL, VDDQ, VREF, and VTT values are in the range of the minimum and maximum values specified in the table *Recommended DC Operating Conditions (SSTL-1.8))* and stable clock (CK, CK#), then apply NOP or Deselect and assert a logic HIGH to CKE.
4. Wait minimum of 400 ns then issue a precharge all command. During the 400 ns period, a NOP or Deselect command must be issued to the DRAM.
5. Issue an EMRS command to EMR(2).
6. Issue an EMRS command to EMR(3).
7. Issue EMRS to enable DLL.
8. Issue a Mode Register Set command for DLL reset.
9. Issue a precharge all command.
10. Issue 2 or more auto-refresh commands.
11. Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. Wait at least 200 clock cycles after step 8 and then execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS Default command (A9=A8=A7=HIGH) followed by EMRS OCD Calibration Mode Exit command (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).
13. The DDR2 SDRAM is now ready for normal operation.

Note:
1. To guarantee ODT off, VREF must be valid and a LOW level must be applied to the ODT pin.

Initialization Sequence after Power-Up Diagram



Programming the Mode Register and Extended Mode Registers

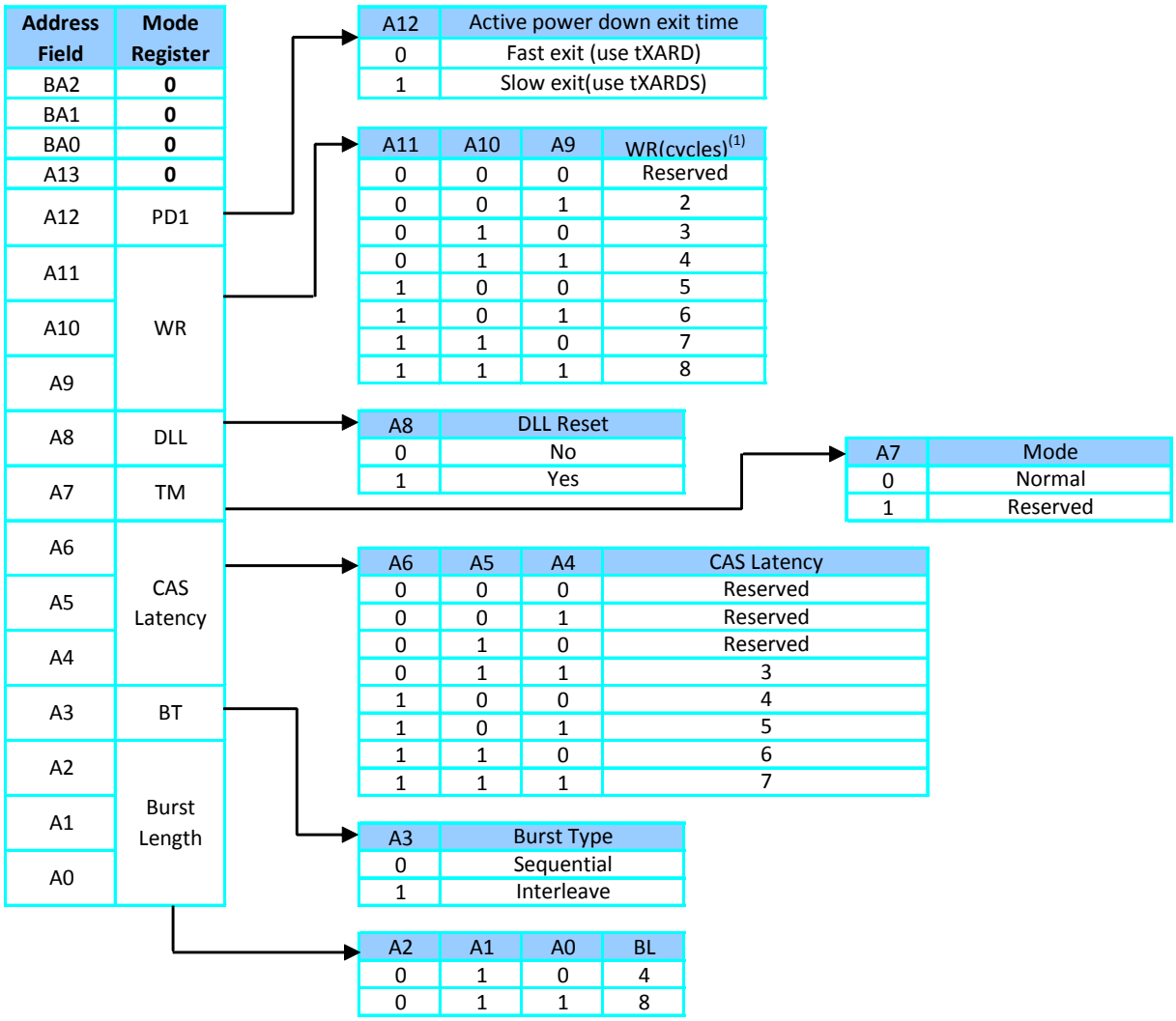
For application flexibility, burst length, burst type, CAS# latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS latency, ODT (On Die Termination), single-ended strobe, and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers EMR[1] and EMR[2] can be altered by re-executing the MRS or EMRS Commands. Even if the user chooses to modify only a subset of the MR, EMR[1], or EMR[2] variables, all variables within the addressed register must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect memory array contents, which mean re-initialization including those can be executed at any time after power-up without affecting memory array contents.

DDR2 Mode Register (MR) Setting

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS# latency, burst length, burst sequence, DLL reset, tWR and active power down exit time to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting LOW on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2 while controlling the state of address pins A0 - A13. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 - A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3; CAS latency is defined by A4 - A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time tWR is defined by A9 - A11. Refer to the table for specific codes.

Mode Register (MR) Diagram



Notes:

1. WR(write recovery for autoprecharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up a non-integer value to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

DDR2 Extended Mode Register 1 (EMR[1]) Setting

The extended mode register 1 stores the data for enabling or disabling the DLL, output driver strength, ODT value selection and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. Extended mode register 1 is written by asserting LOW on CS#, RAS#, CAS#, WE#, BA1, and BA2, and HIGH on BA0, and controlling pins A0 – A13. The DDR2 SDRAM should be in all bank precharge with CKE already HIGH prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling reduced strength data-output driver. A3 - A5 determines the additive latency, A2 and A6 are used for ODT value selection, A7 - A9 are used for OCD control, A10 is used for DQS# disable and A11 is used for RDQS enable.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

Extended Mode Register 1(EMR[1]) Diagram

Address Field	Mode Register
BA2	**0**
BA1	**0**
BA0	**1**
A13	**0**
A12	Qoff
A11	0
A10	DQS#
A9	OCD Program
A8	
A7	
A6	Rtt
A5	Additive Latency
A4	
A3	
A2	Rtt
A1	D.I.C
A0	DLL

A12	Qoff
0	Output buffer enabled
1	Ouput buffer disabled

		Strobe Function Matrix	
A10	DQS#	DQS	DQS#
0	Enable	DQS	DQS#
1	Disable	DQS	Hi-Z

A9	A8	A7	OCD Calibration Program
0	0	0	OCD Calibration mode exit; maintain setting
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode[1]
1	1	1	OCD Calibration default[2]

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reserved

A6	A2	Rtt(NOMINAL)
0	0	ODT Disabled
0	1	75 ohms
1	0	150 ohms
1	1	50 ohms

A1	Output Drive Impedance Control
0	Normal Strength (100%)
1	Reduced strength (60%)

A0	DLL enable
0	Enable
1	Disable

Notes:
1. When Adjust mode is issued, AL from previously set value must be applied.
2. After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000.

DDR2 Extended Mode Register 2 (EMR[2]) Setting

The extended mode register 2 controls refresh related features. The default value of the extended mode register 2 is not defined. Therefore, the extended mode register must be programmed during initialization for proper operation. The extended mode register 2 is written by asserting LOW on CS, RAS, CAS, WE, BA0, BA2, and HIGH on BA1, while controlling pins A0-A13. The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into extended mode register 2. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register 2. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state.

Extended Mode Register 2 (EMR[2]) Diagram

Address Field	Mode Register
BA2	**0**
BA1	**1**
BA0	**0**
A13(1)	**0**
A12(1)	**0**
A11(1)	**0**
A10(1)	**0**
A9(1)	**0**
A8(1)	**0**
A7	SRFt
A6(1)	**0**
A5(1)	**0**
A4(1)	**0**
A3(1)	**0**
A2	PASR(3)
A1	
A0	

A7	High Temperature Self-Refresh Rate Enable
0	Disable
1	Enable(2)

A2	A1	A0	Partial Array Self Refresh for 8 Banks	BA[2:0]
0	0	0	Full Array	All combinations
0	0	1	Half Array	000, 001, 010, 011
0	1	0	Quarter Array	000, 001
0	1	1	1/8 array	000
1	0	0	3/4 array	010, 011, 100, 101, 110, 111
1	0	1	Half array	100, 101, 110, 111
1	1	0	Quarter array	110, 111
1	1	1	1/8 array	111

Notes:
1. A3-A6, and A8-A13 are reserved for future use and must be set to 0 when programming the EMR[2].
2. Only Industrial and Automotive grade devices support the high temperature Self-Refresh Mode. The controller can set the EMR (2) [A7] bit to enable this self-refresh rate if Tc > 85°C while in self-refresh operation. TOPER may not be violated.
3. If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self refresh is entered. Data integrity will be maintained if tREF conditions are met and no Self Refresh command is issued.

DDR2 Extended Mode Register 3 (EMR[3]) Setting

No function is defined in extended mode register 3. The default value of the extended mode register 3 is not defined. Therefore, the extended mode register 3 must be programmed during initialization for proper operation.

DDR2 Extended Mode Register 3 (EMR[3]) Diagram

Address Field	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register	**0***	**1**	**1**	**0***	**0***	**0***	**0***	**0***	**0***	**0***	**0***	**0***	**0***	**0***	**0***	**0***	**0***

Note: All bits in EMR[3] except BA0 and BA1 are reserved for future use and must be set to 0 when programming the EMR[3].

Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Command Truth Table

Function	CKE		CS#	RAS#	CAS#	WE#	BA2-BA0	A13-A11	A10	A9-A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register	H	H	L	L	L	L	BA	Opcode			1, 2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1, 8
Sel Refresh Exit	L	H	H	X	X	X	X	X	X	X	1, 7, 8
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1, 2
Precharge All Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1, 2
Write	H	H	L	H	L	L	BA	X	L	Column	1, 2, 3, 10
Write with Auto Precharge	H	H	L	H	L	L	BA	X	H	Column	1, 2, 3, 10
Read	H	H	L	H	L	H	BA	X	L	Column	1, 2, 3, 10
Read with Auto Precharge	H	H	L	H	L	H	BA	X	H	Column	1, 2, 3, 10
No Operation (NOP)	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					

Notes:

1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, and BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" for details.
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. "X" means "H or L (but a defined logic level)"
7. Self refresh exit is asynchronous.
8. VREF must be maintained during Self Refresh operation.

Clock Enable (CKE) Truth Table

Current State[2]	CKE		Command (N)[3]	Action (N)[3]	Notes
	Previous Cycle[1](N-1)	Current Cycle[1](N)	RAS#, CAS#, WE#, CS#		
Power Down	L	L	X	Maintain Power-Down	11, 13, 15
	L	H	Deselect or NOP	Power Down Exit	4, 8, 11, 13
Self Refresh	L	L	X	Maintain Self-Refresh	11, 15, 16
	L	H	Deselect or NOP	Self-Refresh Exit	4, 5, 9, 16
Bank(s) Active	H	L	Deselect or NOP	Active Power Down Entry	4, 8, 10, 11, 13
All Banks Idle	H	L	Deselect or NOP	Precharge Power Down Entry	4, 8, 10, 11, 13
	H	L	Refresh	Self-Refresh Entry	6, 9, 11, 13
	H	H	Refer to the Command Truth Table		7

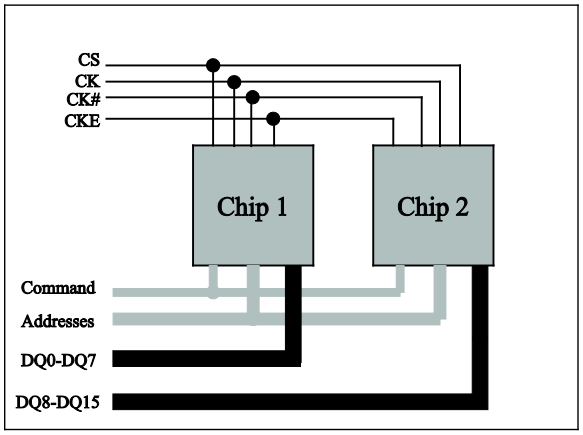
Notes:
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On Self Refresh Exit, DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELECT only.
10. Power Down and Self Refresh cannot be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress.
11. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
13. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in this datasheet.
14. CKE must be maintained HIGH while the DDRII SDRAM is in OCD calibration mode.
15. "X" means "Don't Care (including floating around VREF)" in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMR[1]).
16. VREF must be maintained during Self Refresh operation.

Data Mask (DM) Truth Table

Name (Functional)	DM	DQs	Note
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Note:
1. Used to mask write data, provided coincident with the corresponding data.

Functional Block Diagram



Commands

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected. DESELECT is also referred to as COMMAND INHIBIT.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE (LM)

The mode registers are loaded via bank address and address inputs. The bank address balls determine which mode register will be programmed. See “Mode Register (MR)” in the next section. The LM command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the bank address inputs determines the bank, and the address inputs select the row. This row will remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the bank address inputs determine the bank, and the address provided on address inputs A0–A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses. DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to tRCD(Min) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the bank select inputs selects the bank, and the address provided on inputs A0–A9 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.
DDR2 SDRAM also supports the AL feature, which allows a READ or WRITE command to be issued prior to tRCD(MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

REFRESH

REFRESH is used during normal operation of the DDR2 SDRAM and is analogous to CAS#-before-RAS# (CBR) REFRESH. All banks must be in the idle mode prior to issuing a REFRESH command. This command is nonpersistent, so it must be issued each time a refresh is

required. The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during a REFRESH command.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including VREF) must be maintained at valid levels upon entry/exit and during SELF REFRESH operation.

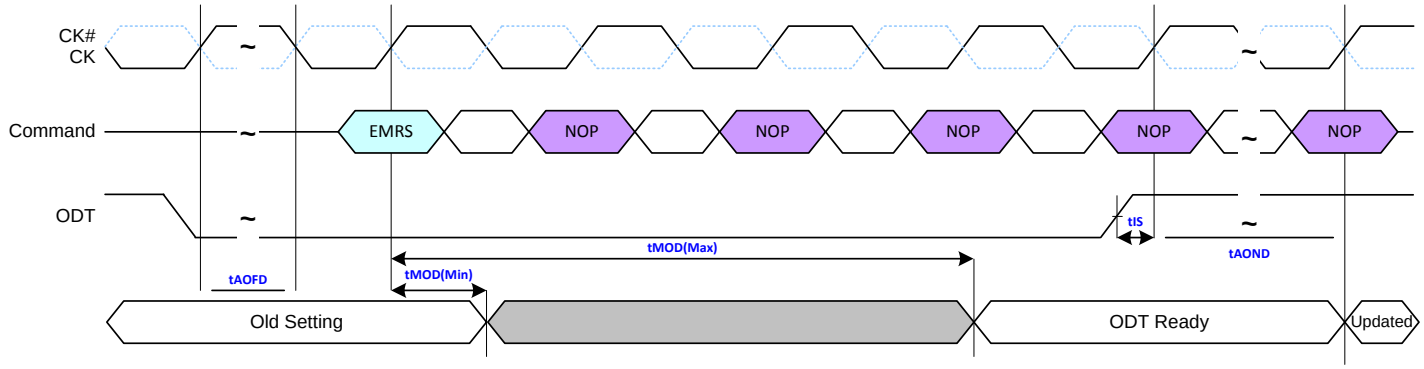
The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh.

ODT (On-Die Termination)

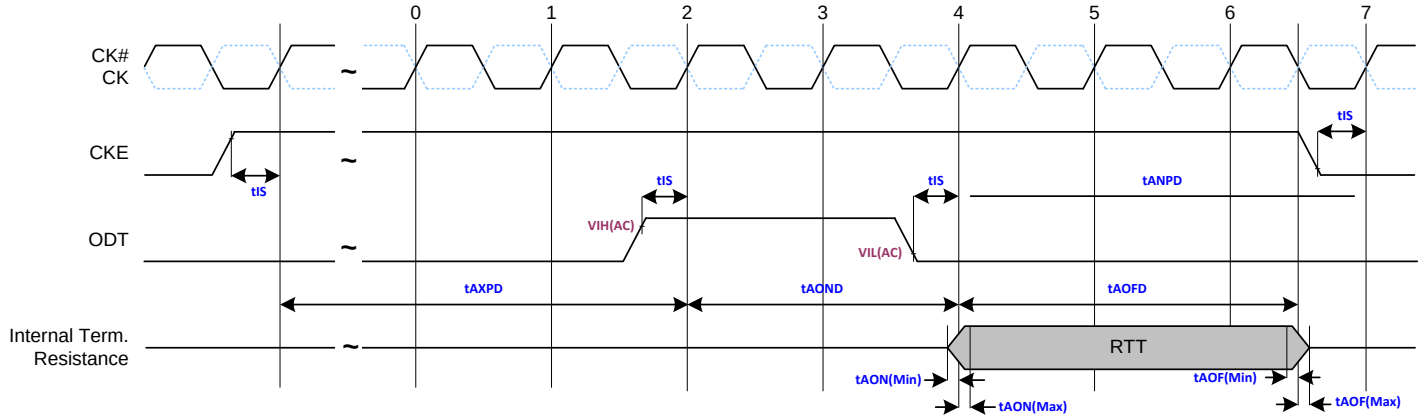
The On-Die Termination feature allows the DDR2 SDRAM to easily implement an internal termination resistance (Rtt). ODT can be configured for DQ[15:0], UDQS, LDQS, UDQS#, LDQS#, and UDM, and LDM signals. The ODT feature can be configured with the Extended Mode Register Set (EMRS) command, and turned on or off using the ODT input signal. Before and after the EMRS is issued, the ODT input must be received with respect to the timings of tAOFD, tMOD(max), tAOND; and the CKE input must be held HIGH throughout the duration of tMOD(max).

The DDR2 SDRAM supports the ODT on and off functionality in Active, Standby, and Power Down modes, but not in Self Refresh mode. ODT timing diagrams follow for Active/Standby mode and Power Down mode.

EMRS to ODT Update Delay



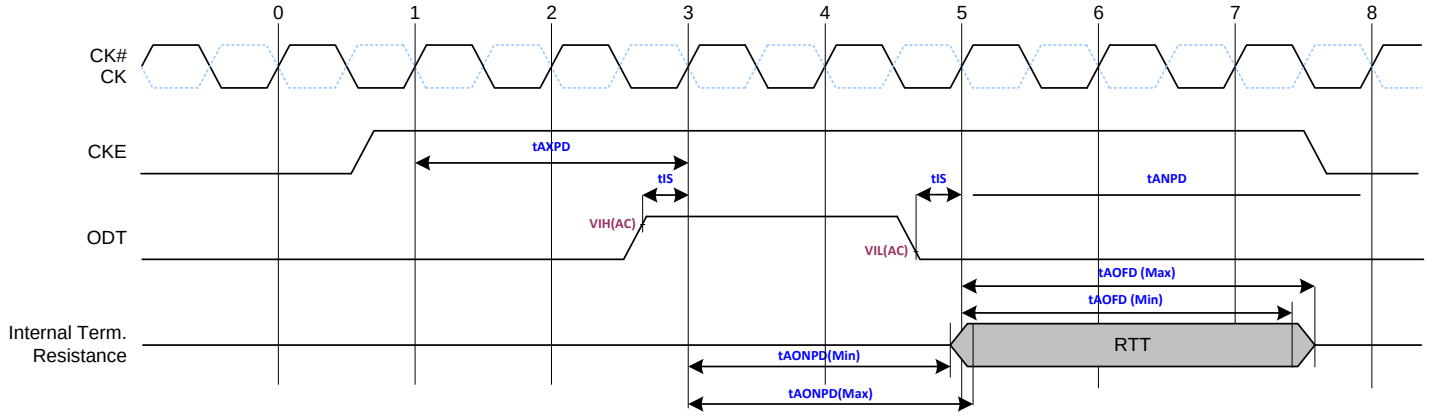
ODT Timing for Active/Standby (Idle) Mode and Standard Active Power-Down Mode



Notes:

1. Both ODT to Power Down Entry and Exit Latency timing parameter tANPD and tAXPD are met, therefore Non-Power Down Mode timings have to be applied.
2. ODT turn-on time, tAON(Min) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max, tAON(Max) is when the ODT resistance is fully on. Both are measured from tAOND.
3. ODT turn off time min, tAOF(Min), is when the device starts to turn off the ODT resistance. ODT turn off time max, tAOF(Max) is when the bus is in high impedance. Both are measured from tAOFD.

ODT Timing for Precharge Power-Down Mode



Note: Both ODT to Power Down Endtry and Exit Latencies tANPD and tAXPD are not met, therefore Power-Down Mode timings have to be applied.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-1.0 to 2.3	V	1, 3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 to 2.3	V	1, 3
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 to 2.3	V	1, 3
Vin, Vout	Voltage on any pin relative to Vss	- 0.5 to 2.3	V	1, 4
Tstg	Storage Temperature	-55 to +150	°C	1, 2

Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ. When VDD and VDDQ and VDDL are less than 500mV, VREF may be equal to or less than 300mV.
4. Voltage on any input or I/O may not exceed voltage on VDDQ.

AC and DC Operating Conditions

Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	2, 3
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	3

Notes:
1. There is no specific device VDD supply voltage requirement for SSTL_1.8 compliance. However, under all conditions VDDQ must be less than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak AC noise on VREF may not exceed +/-2% VREF(DC).
4. VTT of transmitting device must track VREF of receiving device.
5. AC parameters are measured with VDD, VDDQ and VDDL tied together.

Operating Temperature Condition (1, 2, 3)

Symbol	Parameter	Rating	Units
TOPER	Commercial Operating Temperature	Tc = 0 to 85, Ta = 0 to 70	°C
TOPER	Industrial Operating Temperature, Automotive Operating Temperature (A1)	Tc = -40 to 95, Ta = -40 to 85	°C
TOPER	Automotive Operating Temperature (A2)	Tc = -40 to 105, Ta = -40 to 105	°C

Notes:
1. Tc = Operating case temperature at center of package.
2. Ta = Operating ambient temperature immediately above package center.
3. Both temperature specifications must be met.

Thermal Resistance

	Airflow = 0m/s	Airflow = 1m/s	Airflow = 2m/s	Units
Theta-ja	59.4	41.5	35.7	C/W
Theta-jc	0.1	0.4	0.6	C/W

Note: 4-layer PCB

AC and DC Logic Input Levels

Single-ended DC Input Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
VIH(DC)	DC input logic HIGH	VREF + 0.125	VDDQ + 0.3 V	V	
VIL(DC)	DC input logic LOW	- 0.3	VREF - 0.125	V	

Single-ended AC Input logic level

Symbol	Parameter	Min.	Max.	Units
VIH(AC)	AC input logic HIGH	VREF + 0.250	VDDQ + Vpeak	V
VIL(AC)	AC input logic LOW	VSSQ - Vpeak	VREF - 0.250	V

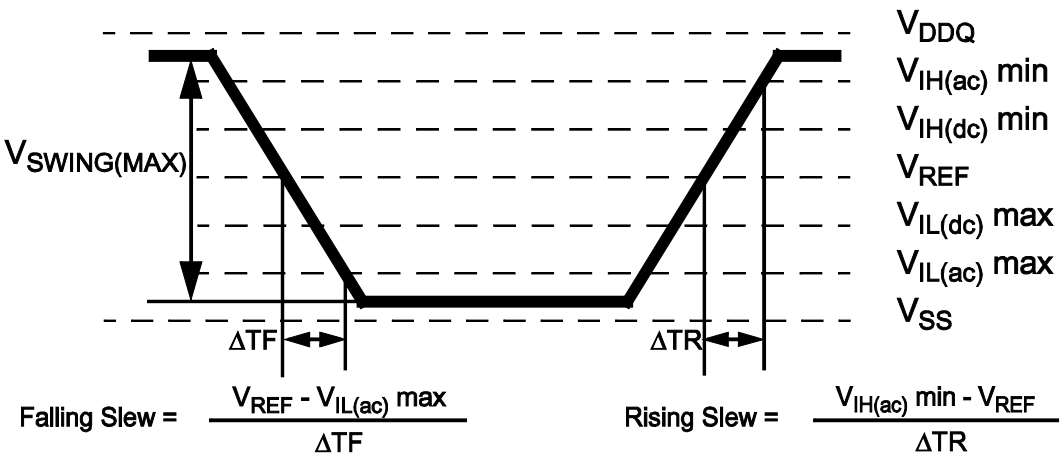
Note: Refer to *Overshoot and Undershoot Specification* for Vpeak value: maximum peak amplitude allowed for overshoot and undershoot.

AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
VREF	Input reference voltage	0.5 x VDDQ	V	1
VREF	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:
1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(AC) min for rising edges and the range from VREF to VIL(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.

AC Input Test Signal Waveform

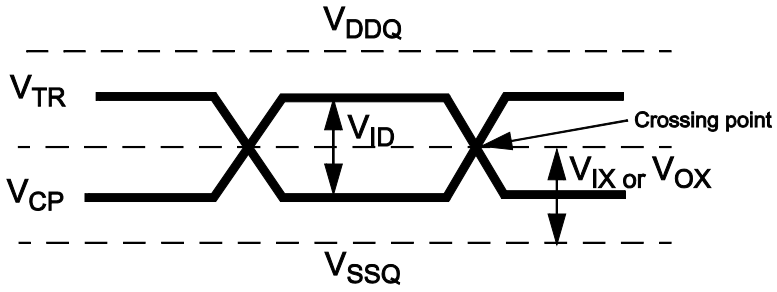


Differential Input AC logic level

Symbol	Parameter	Min.	Max.	Units	Notes
VID(AC)	AC differential input voltage	0.5	VDDQ	V	1, 3
VIX(AC)	AC differential crosspoint voltage	0.5*VDDQ-0.175	0.5*VDDQ+0.175	V	2

Notes:
1. VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as CK#, DQS#, LDQS# or UDQS#). The minimum value is equal to V IH(AC) - V IL(AC).
2. The typical value of VIX(AC) is expected to be about 0.5 x VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ. VIX(AC) indicates the voltage at which differential input signals must cross.
3. Refer to Overshoot and Undershoot Specifications for Vpeak value: maximum peak amplitude allowed for overshoot and undershoot.

Differential Signal Level Waveform



Differential AC Output Parameters

Symbol	Parameter	Min.	Max.	Units
VOX(AC)	AC differential crosspoint voltage	0.5 x VDDQ-0.125	0.5 x VDDQ+0.125	V

Note: The typical value of VOX(AC) is expected to be about 0.5 x VDDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ. VOX(AC) indicates the voltage at which differential output signals must cross.

Overshoot and Undershoot Specification

AC Overshoot and Undershoot Specification for Address and Control Pins

Parameter	DDR2-533	DDR2-667	Unit
Maximum peak amplitude allowed for overshoot area	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	V
Maximum overshoot area above VDD*	0.8	0.8	V-ns
Maximum undershoot area below VSS*	0.8	0.8	V-ns

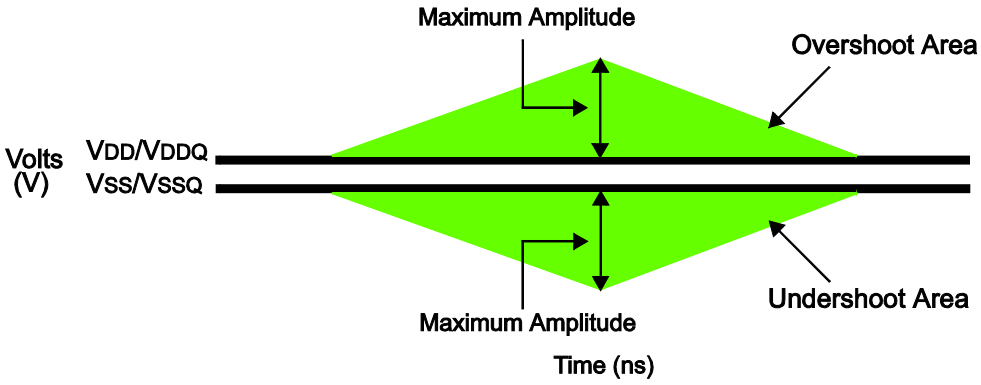
Note: Please refer to *AC Overshoot and Undershoot Definition Diagram*.

AC Overshoot and Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	DDR2-533	DDR2-667	Unit
Maximum peak amplitude allowed for overshoot area	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	V
Maximum overshoot area above VDDQ*	0.23	0.23	V-ns
Maximum undershoot area below VSSQ*	0.23	0.23	V-ns

Note: Please refer to *AC Overshoot and Undershoot Definition Diagram*.

AC Overshoot and Undershoot Definition Diagram



Output Buffer Characteristics

Output AC Test Conditions

Symbol	Parameter	SSTL_18	Units
VOTR	Output Timing Measurement Reference Level	0.5 x VDDQ	V

Note: The VDDQ of the device under test is referenced.

Output DC Current Drive

Symbol	Parameter	SSTL_18	Units	Notes
IOH(DC)	Output Minimum Source DC Current	13.4	mA	1, 3, 4
IOL(DC)	Output Minimum Sink DC Current	-13.4	mA	2, 3, 4

Notes:

1. VDDQ = 1.7 V; VOUT = 1420 mV. (VOUT - VDDQ)/IOH must be less than 21 Ω for values of VOUT between VDDQ and VDDQ - 280 mV.
2. VDDQ = 1.7 V; VOUT = 280 mV. VOUT/IOL must be less than 21 Ω for values of VOUT between 0 V and 280 mV.
3. The dc value of VREF applied to the receiving device is set to VTT
4. The values of IOH(DC) and IOL(DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure VIH min plus a noise margin and VIL max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3 of JESD8-15A) along a 21 Ω load line to define a convenient driver current for measurement.

OCD Default Characteristics

Description	Parameter	Min.	Nom.	Max.	Units	Notes
Output Impedance		Normal 18 ohms See full strength default driver characteristics			ohms	1, 2
Output impedance step size for OCD calibration		0		1.5	ohms	6
Pull-up and pull-down mismatch		0		4	ohms	1, 2, 3
Output slew rate	SOUT	1.5		5	V/ns	1, 4, 5, 7, 8, 9

Notes:

1. Absolute Specifications (TOPER; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V). DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings.
2. Impedance measurement condition for output source dc current: VDDQ = 1.7 V; VOUT = 1420 mV; (VOUTVDDQ)/IOH must be less than 23.4 Ω for values of VOUT between VDDQ and VDDQ - 280 mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7 V; VOUT = 280 mV; VOUT/IOL must be less than 23.4 Ω for values of VOUT between 0 V and 280 mV.
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Slew rate measured from VIL(AC) to VIH(AC).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 Ω at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0 Ω value (no calibration) can only be achieved if the OCD impedance is 18 Ω +/-0.75 Ω under nominal conditions.
7. DRAM output slew rate specification applies to 667 MT/s speed bins.
8. Timing skew due to DRAM output slew rate mis-match between DQS / DQS# and associated DQ's is included in tDQSQ and tQHS specification.

Output Capacitance

Paramater	Symbol	-37C (DDR2-533C)		-3D (DDR2-667D)		Units
		Min	Max	Min	Max	
Input Capacitance (CK and CK#)	CCK	1.00	2.00	1.00	2.00	pF
Input Capacitance Delta (CK and CK#)	CDCK		0.25		0.25	pF
Input Capacitance (all other input-only pins)	CI	1.00	2.00	1.00	2.00	pF
Input Capacitance Delta (all other input-only pins)	CDI		0.25		0.25	pF
I/O Capacitance (DQ, DM, DQS, DQS#)	CIO	2.50	4.00	2.50	3.50	pF
I/O Capacitance Delta (DQ, DM, DQS, DQS#)	CDIO		0.50		0.50	pF

ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min.	Nom.	Max.	Units	Notes
Rtt effective impedance value for EMRS(A6=0, A2=1); 75 ohm	Rtt1(eff)	60	75	90	ohms	1
Rtt effective impedance value for EMRS(A6=1, A2=0); 150 ohm	Rtt2(eff)	120	150	180	ohms	1
Rtt effective impedance value for EMRS(A6=A2=1); 50 ohm	Rtt3(eff)	40	50	60	ohms	1
Deviation of VM with respect to VDDQ/2	Delta VM	-6		+6	%	2

Note:

1. Measurement Definition for Rtt(eff):
   Apply VIHac and VILac to test pin seperately, then measure current I(VIHac) and I(VILac) respectively

$$Rtt(eff) = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

2. Measurement Defintion for VM:
   Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1 \right) \times 100\%$$

ODT AC Electrical Characteristics and Operating Conditions

Symbol	Parameter/Condition	Min.	Max.	Units	Notes
tAOND	ODT turn-on delay	2	2	tCK	
tAON	ODT turn-on	tAC(Min)	tAC(Max)+0.7ns	ns	1
tAONPD	ODT turn-on (Power-Down Mode)	tAC(Min)+2ns	2tCK+tAC(Max)+1ns	ns	3
tAOFD	ODT turn-off delay	2.5	2.5	tCK	
tAOF	ODT turn-off	tAC(Min)	tAC(Max)+0.6ns	ns	2
tAOFPD	ODT turn-off (Power-Down Mode)	tAC(Min)+2ns	2.5tCK+tAC+1ns	ns	3
tANPD	ODT to Power-Down Mode Entry L:atency	3		tCK	4
tAXPD	ODT Power Down Exit Latency	8		tCK	4

Notes:

1. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.
2. ODT turn off time min is when the device starts to turn-off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.
3. For Standard Active Power-Down (with MR S A12 = “0”), the non power -down timings (tAOND, tAON, tAOFD and tAOF) apply.
4. tANPD an d tAXPD define the timing limit when either Power Down Mode Timings (tAONPD, tAOFPD) or Non-Power Down Mode timings (tAOND, tAOFD) have to be applied

IDD Specifications and Conditions

IDD Measurement Conditions

Symbol	Parameter/Condition
IDD0	Operating Current - One bank Active - Precharge: tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD1	Operating Current - One bank Active - Read - Precharge: IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
IDD2P	Precharge Power-Down Current: All banks idle; tCK = tCK(IDD); CKE is LOW, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD2Q	Precharge Standby Current: All banks idle; tCK = tCK(IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING
IDD2N	Precharge Quiet Standby Current: All banks idle; tCK = tCK(IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
IDD3Pf	Active Power-Down Current: All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING. MRS A12 bit is set to "0"(Fast Power-down Exit).
IDD3Ps	Active Power-Down Current: All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING. MRS A12 bit is set to "1"(Slow Power-down Exit).
IDD3N	Active Standby Current: All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD4R	Operating Current - Burst Read: All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W
IDD4W	Operating Current - Burst Write: All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD5B	Burst Auto-Refresh Current: tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD5D	Distributed Refresh Current: tCK = tCK(IDD); Refresh command frequency satisfying tREFI; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD6	Self-Refresh Current: CK and CK# at 0 V; CKE 0.2 V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.
IDD7	Operating Bank Interleave Read Current: All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1 x tCK(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;

Notes:

1. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. IDD values must be met with all combinations of EMRS bits 10 and 11.
2. For DDR2-667/800 testing, tCK in the Conditions should be interpreted as tCK(avg).
3. Definitions for IDD:
   a. LOW is defined as VIN ≤ VILAC(max).
   b. HIGH is defined as VIN ≥ VIHAC(min).
   c. STABLE = inputs stable at a HIGH or LOW level.
   d. FLOATING = inputs at VREF = VDDQ/2.
   e. SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.
4. Legend: A=Activate, RA=Read with Auto-Precharge, D=DESELECT.

IDD Specifications

Symbol	-37C DDR2-533C	-3D DDR2-667D	Units
IDD0	140	150	mA
IDD1	165	175	mA
IDD2P	25	30	mA
IDD2N	85	90	mA
IDD2Q	65	70	mA
IDD3Pf	45	45	mA
IDD3Ps	35	35	mA
IDD3N	100	105	mA
IDD4R	265	280	mA
IDD4W	265	275	mA
IDD5B	435	445	mA
IDD5D	90	90	mA
IDD6	12	12	mA
IDD7	445	485	mA

Notes:
1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric Test Condition.
3. IDD parameters are specified with ODT disabled.

AC Characteristics

(AC Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	-37C DDR2-533C		-3D DDR2-667D		-25E DDR2-800E		-25D DDR2-800D		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row Cycle Time	tRC	60		60		60		57.5		ns	
Auto Refresh Row Cycle Time	tRFC	127.5		127.5		127.5		127.5		ns	11
Row Active Time	tRAS	45	70K	45	70K	45	70K	45	70K	ns	21
Row Active to Column Address Delay	tRCD	15		15		15		12.5		ns	20
Row Active to Row Active Delay	tRRD	10		10		10		10		ns	
Four Activate Window	tFAW	50		50		45		45		ns	
Column Address to Column Address Delay	tCCD	2		2		2		2		tCK	
Row Precharge Time	tRP	15		15		15		12.5		ns	
Write Recovery Time	tWR	15		15		15		15		ns	
Auto precharge Write recovery + Precharge Time	tDAL	Min = tWR+tRP, Max = n/a								ns	12
Clock Cycle Time	tCK3 (CL=3)	5	8	5	8					ns	2
	tCK4 (CL=4)	3.75	8	3.75	8	3.75	8	3.75	8	ns	2
	tCK5 (CL=5)			3	8	3	8	2.5	8	ns	2
	tCK6 (CL=6)					2.5	8	2.5	8	ns	
Clock High Level Width	tCH	0.45	0.55	0.48	0.52	0.48	0.52	0.48	0.52	tCK	
Clock Low Level Width	tCL	0.45	0.55	0.48	0.52	0.48	0.52	0.48	0.52	tCK	
Cycle to cycle	tJITcc	250		250		200		200		ps	
Data-Out Edge to Clock Skew Edge	tAC	-0.5	0.45	-0.45	0.45	-0.4	0.4	-0.4	0.4	ns	
DQS-Out Edge to Clock Skew Edge	tDQSCK	-0.45	0.4	-0.4	0.4	-0.35	0.35	-0.35	0.35	ns	
DQS-Out Edge to Clock Skew Edge	tDQSQ		0.3		0.24		0.2		0.2	ns	
Data-Out Hold Time from DQS	tQH	Min = tHP(min)-tQHS, Max = n/a								ns	
Data Hold Skew Factor	tQHS		400		340		300		300	ps	
Clock Half Period	tHP	Min = tCH(min)/tCL(min), Max = n/a								ns	5

AC Characteristics

(AC Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	-37C DDR2-533C		-3D DDR2-667D		-25E DDR2-800E		-25D DDR2-800D		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input Setup Time (fast slew rate)	tIS	250		200		175		175		ps	15,17
Input Hold Time (fast slew rate)	tIH	375		275		250		250		ps	15,17
Input Pulse Width	tIPW	0.6		0.6		0.6		0.6		tCK	
Write DQS High Level Width	tDQSH	0.35		0.35		0.35		0.35		tCK	
Write DQS Low Level Width	tDQSL	0.35		0.35		0.35		0.35		tCK	
CLK to First Rising Edge of DQS-In	tDQSS	Min = -0.25tCK, Max = +0.25tCK								tCK	
Data-In Setup Time to DQS-In (DQ, DM)	tDS	100		100		50		50		ps	16,17, 18
Data-In Hold Time to DQS-In (DQ, DM)	tDH	225		175		125		125		ps	16,17, 18
DQS falling edge from CLK rising Setup Time	tDSS	0.2		0.2		0.2		0.2		tCK	
DQS falling edge from CLK rising Hold Time	tDSH	0.2		0.2		0.2		0.2		tCK	
DQ & DM Pulse Width	tDIPW	0.35		0.35		0.35		0.35		tCK	
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write DQS Preamble Setup Time	tWPRES	0		0		0		0		tCK	
Write DQS Preamble Hold Time	tWPREH	0.25		0.25		0.25		0.25		tCK	
Write DQS Preamble Time	tWPRE	0.35		0.35		0.35		0.35		tCK	
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	10
Internal Read to Precharge Command Delay	tRTP	7.5		7.5		7.5		7.5		ns	
Internal Write to Read Command Delay	tWTR	7.5		7.5		7.5		7.5		ns	13
Data-Out to High Impedance from CK/CK#	tHZ	Min = n/a, Max = tAC(max)								ns	7
DQS/DQS# Low Impedance from CK/CK#	tLZ(DQS)	Min = tAC(min), Max = tAC(max)								ns	7

AC Characteristics

(AC Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	-37C DDR2-533C		-3D DDR2-667D		-25E DDR2-800E		-25D DDR2-800D		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DQ to Low Impedance from CK/CK#	tLZ(DQ)	Min = 2 x tAC(min), Max = tAC(max)								ns	7
Mode Register Set Delay	tMRD	2		2		2		2		tCK	9
OCD Drive Mode Output Delay	tMOD	0	12	0	12	0	12	0	12	ns	
ODT Drive Mode Output Delay	tOIT	0	12	0	12	0	12	0	12	ns	
Exit Self refresh to Non-Read Command	tXSNR	Min = t_{RFC} + 10, Max = n/a								ns	19
Exit Self refresh to Read Command	tXSRD	200		200		200		200		t_{CK}	
Exit Precharge Power Down to any Non-Read Command	tXP	2		2		2		2		t_{CK}	14
Exit Active Power Down to Read Command	tXARD	2		2		2		2		t_{CK}	
Exit Active Power Down to Read Command (slow exit, low power)	tAXRDS	6-AL		7-AL		8-AL		8-AL		t_{CK}	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDELAY	Min = t_{IS}+t_{CK}+t_{IH}, Max = n/a								ns	
CKE minimum high and low pulse width	tCKE	3		3		3		3		t_{CK}	
Average Periodic Refresh Interval (-40°C ≤ T_C ≤ +85° C)	tREFI		7.8		7.8		7.8		7.8	µs	18, 23
Average Periodic Refresh Interval (+85°C < T_C ≤ +95° C)	tREFI		3.9		3.9		3.9		3.9	µs	18, 23
Average Periodic Refresh Interval (+95°C < T_C ≤ +105° C)	tREFI		3.9		3.9		3.9		3.9	µs	18, 23
Period Jitter	tJITPER	-125	125	-125	125	-100	100	-100	100	ps	22
Half Period Jitter	tJITDTY	-125	125	-125	125	-100	100	-100	100	ps	22
Cycle to Cycle Jitter	tJITCC	-250	250	-250	250	-200	200	-200	200	ps	22
Cumulative error, 2 cycles	tERR(2PER)	-175	175	-175	175	-150	150	-150	150	ps	22
Cumulative error, 3 cycles	tERR(3PER)	-225	225	-225	225	-175	175	-175	175	ps	22
Cumulative error, 4 cycles	tERR(4PER)	-250	250	-250	250	-200	200	-200	200	ps	22
Cumulative error, 5 cycles	tERR(5PER)	-250	250	-250	250	-200	200	-200	200	ps	22
Cumulative error, 6-10 cycles	tERR (6-10PER)	-350	350	-350	350	-300	300	-300	300	ps	22
Cumulative error, 11-50 cycles	tERR (11-50PER)	-450	450	-450	450	-450	450	-450	450	ps	22

Notes:

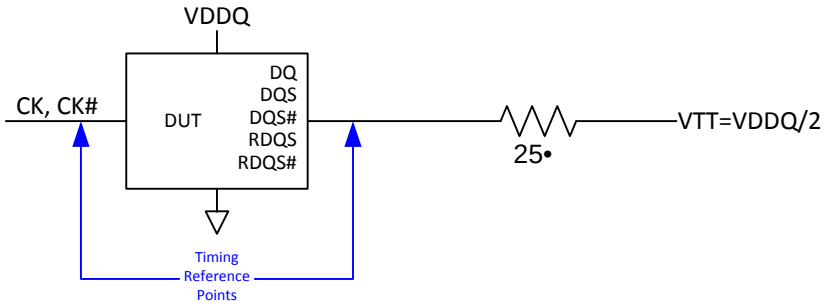
1. Input slew rate is 1 V/ns and AC timings are guaranteed for linear signal transitions.
2. The CK/CK# input reference level (for timing reference to CK/CK#) is the point at which CK and CK# cross the DQS/DQS# input reference level is the cross point when in differential strobe mode; the input reference level for signals other than CK/CK#, or DQS/DQS# is VREF.
3. Inputs are not recognized as valid until VREF stabilizes. During the period before VREF stabilizes, CKE = 0.2 x VDDQ is recognized as LOW.
4. The output timing reference voltage level is VTT.
5. The values tCL(min) and tCH(min) refer to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH.
6. For input frequency change during DRAM operation.
7. Transitions for tHZ and tLZ occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
8. These parameters guarantee device timing, but they are not necessarily tested on each device.
9. The specific requirement is that DQS and DQS# be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS. When programmed in differential strobe mode, DQS is always the logic complement of DQS except when both are in high-Z.
10. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
11. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device. (Note: tRFC depends on DRAM density)
12. For each of the terms, if not already an integer, round to the next highest integer. tCK refers to the application clock period. WR refers to the WR parameter stored in the MRS.
13. Parameter tWTR is at least two clocks independent of operation frequency.
14. User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MRS, A12 = “0”) a fast power-down exit timing tXARD can be used. In “low active power-down mode” (MRS, A12 = “1”) a slow power-down exit timing tXARDS has to be satisfied.
15. Timings are guaranteed with command / address input slew rate of 1.0 V/ns.
16. Timings are guaranteed with data / mask input slew rate of 1.0 V/ns.
17. Timings are guaranteed with CK/CK# differential slew rate 2.0 V/ns, and DQS/DQS# (and RDQS/RDQS#) differential slew rate 2.0 V/ns in differential strobe mode.
18. If refresh timing or tDS / tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
19. In all circumstances, tXSNR can be satisfied using tXSNR = tRFC + 10 ns.
20. The tRCD timing parameter is valid for both activate command to read or write command with and without Auto-Precharge. Therefore a separate parameter tRAP for activate command to read or write command with Auto-Precharge is not necessary anymore.
21. tRAS(max) is calculated from the maximum amount of time a DDR2 device can operate without a Refresh command which is equal to 9 x tREFI.
22. Definitions:
    a. tCK(avg): tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.
    b. tCH(avg): tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.
    c. tCL(avg): tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.
    d. tJITDTY: tJITDTY is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg)
    e. tJITPER: tJITPER is defined as the largest deviation of any single tCK from tCK(avg).
    f. tJITCC: tJITCC is defined as the difference in clock period between two consecutive clock cycles: tJITCC is not guaranteed through final production testing
    g. tERR: tERR is defined as the cumulative error across multiple consecutive cycles from tCK (avg).
23. Applicable to certain temperature grades. Specified OPER (Tc and Ta) must not be violated for each temperature grade.

Reference Loads, Slew Rates and Slew Rate Derating

1. Reference Load for Timing Measurements

Figure *AC Timing Reference Load* represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). This load circuit is also used for output slew rate measurements.

AC Timing Reference Load

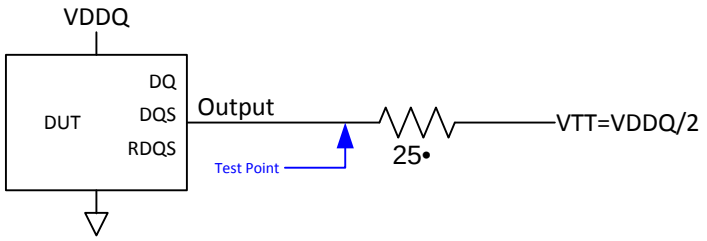


The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. DQS#) signal.

2. Slew Rate Measurements

a) Output Slew Rate

Output slew rate is characterized under the test conditions as shown in the figure below.



Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS – DQS#) output slew rate is measured between DQS – DQS# = - 500 mV and DQS – DQS# = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

b) Input Slew Rate

Input slew rate for single ended signals is measured from VREF(DC) to VIH(AC),min for rising edges and from VREF(DC) to VIL(AC),min for falling edges. For differential signals (e.g. CK – CK#) slew rate for rising edges is measured from CK – CK# = - 250 mV to CK - CK = + 500 mV (+ 250 mV to - 500 mV for falling edges). Test conditions are the same as for timing measurements.

ORDERING INFORMATION

Commercial Range: T_C = 0° to +85°C; T_A = 0°C to +70°C

Frequency	Speed Grade	CL-t_{RC}-t_{RP}	Order Part No.	Organization	Package
333 MHz	DDR2-667D	5-5-5	IS43DR16128-3DBL	128Mb x 16	84-ball FBGA, lead free

Industrial Range: T_C = -40° to +95°C; T_A = -40°C to +85°C

Frequency	Speed Grade	CL-t_{RC}-t_{RP}	Order Part No.	Organization	Package
333 MHz	DDR2-667D	5-5-5	IS43DR16128-3DBLI	128Mb x 16	84-ball FBGA, lead free
			IS43DR16128-3DBI	128Mb x 16	84-ball FBGA

Automotive, A1 Range: T_C = -40° to +95°C; T_A = -40°C to +85°C

Frequency	Speed Grade	CL-t_{RC}-t_{RP}	Order Part No.	Organization	Package
333 MHz	DDR2-667D	5-5-5	IS46DR16128-3DBLA1	128Mb x 16	84-ball FBGA, lead free

Automotive, A2 Range: T_C = -40° to +95°C; T_A = -40°C to +105°C

Frequency	Speed Grade	CL-t_{RC}-t_{RP}	Order Part No.	Organization	Package
333 MHz	DDR2-667D	5-5-5	IS46DR16128-3DBLA2	128Mb x 16	84-ball FBGA, lead free

84-ball FBGA: Fine Pitch Ball Grid Array Outline

