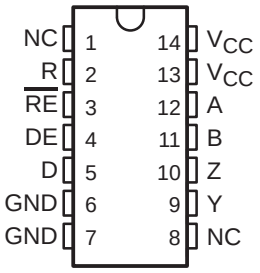
- **Designed for High-Speed Multipoint Data Transmission Over Long Cables**
- **Operate With Pulse Durations as Low as 30 ns**
- **Low Supply Current . . . 5 mA Max**
- **Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **3-State Outputs for Party-Line Buses**
- **Common-Mode Voltage Range of –7 V to 12 V**
- **Thermal Shutdown Protection Prevents Driver Damage From Bus Contention**
- **Positive and Negative Output Current Limiting**
- **Pin Compatible With the SN75ALS180**

description

The SN65LBC180 and SN75LBC180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that meet or exceed the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). Both devices are designed using TI's proprietary LinBiCMOS™ with the low power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

Both the SN65LBC180 and SN75LBC180 combine a differential line driver and receiver with 3-state outputs and operate from a single 5-V supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus whether disabled or powered off (V_{CC} = 0). These parts feature a wide common-mode voltage range making them suitable for point-to-point or multipoint data-bus applications.

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

Function Tables

DRIVER

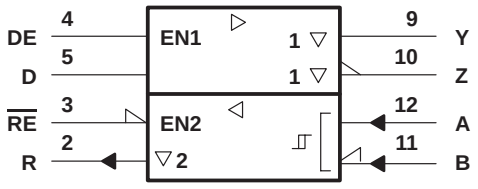
INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open circuit	L	H

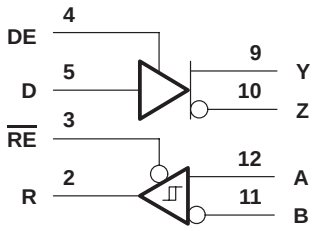
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



LinBiCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

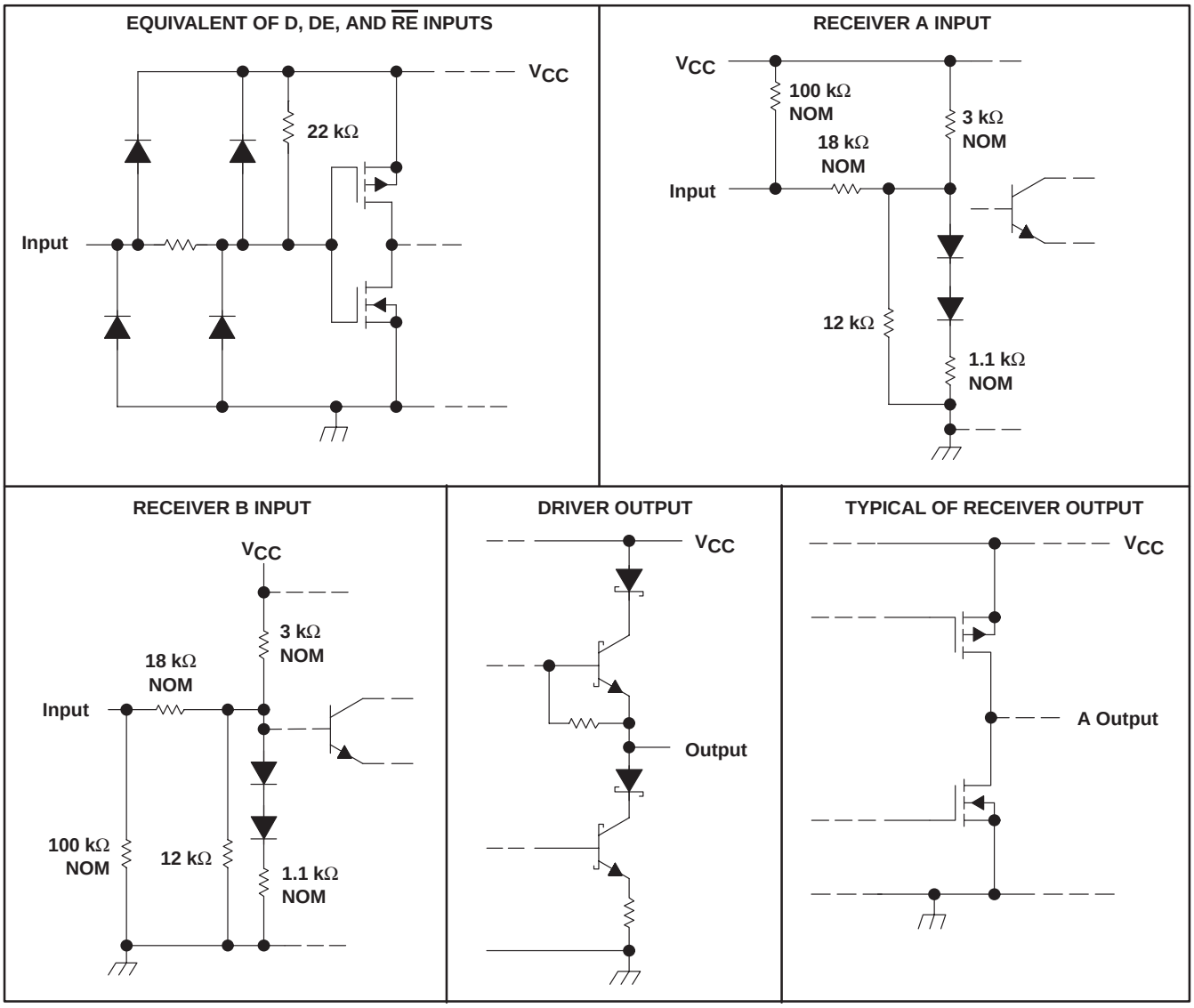
Copyright © 2000, Texas Instruments Incorporated

description (continued)

The devices also provide positive and negative output-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

The SN65LBC180 and SN75LBC180 are available in the 14-pin dual-in-line and small-outline packages. The SN75LBC180 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC180 is characterized over the industrial temperature range of –40°C to 85°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 7 V
Input voltage range, V_I (A, B)(see Note 1) . . . . . –10 V to 15 V
Voltage range at D, R, DE, $\overline{RE}$ (see Note 1) . . . . . –0.3 V to V_{CC} + 0.5 V
Continuous total power dissipation (see Note 2) . . . . . Internally limited
Total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65LBC180 . . . . . –40°C to 85°C
SN75LBC180 . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID}		–6‡		6	V
Voltage at any bus terminal (separately or common mode), V_O, V_I, or V_{IC}	A, B, Y, or Z	–7‡		12	V
High-level output current, I_{OH}	Y or Z			–60	mA
	R			–8	
Low-level output current, I_{OL}	Y or Z			60	mA
	R			8	
Operating free-air temperature, T_A	SN65LBC180	–40		85	°C
	SN75LBC180	0		70	

‡ The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.

DRIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
$\lvert V_{OD} \rvert$	Differential output voltage magnitude (see Note 3)	R_L = 54 Ω, See Figure 1	SN65LBC180	1.1	2.5	5	V
			SN75LBC180	1.5	2.5	5	
		R_L = 60 Ω, See Figure 2	SN65LBC180	1.1	2	5	
			SN75LBC180	1.5	2	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage (see Note 4)	See Figures 1 and 2				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω, See Figure 1		1	2.5	3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = –7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				–100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–100	µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V				±250	mA
I_{CC}	Supply current	Receiver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 3. The minimum V_{OD} specification of the SN65LBC180 may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

4. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 3	7	12	18	ns
$t_{t(OD)}$	Differential output transition time			5	10	20	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4			35	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5			35	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5			35	ns

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		–0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				45		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA		0.3	0.5	V
I_{OZ}	High-impedance-state output current	V_O = 0 V to V_{CC}				±20	µA
I_{IH}	High-level enable-input current	V_{IH} = 2.4 V				–50	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				–100	µA
I_I	Bus input current	V_I = 12 V, Other input at 0 V	V_{CC} = 5 V,		0.7	1	mA
		V_I = 12 V, Other input at 0 V	V_{CC} = 0 V,		0.8	1	
		V_I = –7 V, Other input at 0 V	V_{CC} = 5 V,		–0.5	–0.8	
		V_I = –7 V, Other input at 0 V	V_{CC} = 0 V,		–0.5	–0.8	
I_{CC}	Supply current	Driver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 6	11	22	33	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	33	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			3	6	ns
t_t	Transition time			5	8	ns
t_{PZH}	Output enable time to high level	See Figure 7			35	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level				35	ns
t_{PLZ}	Output disable time from low level				30	ns

PARAMETER MEASUREMENT INFORMATION

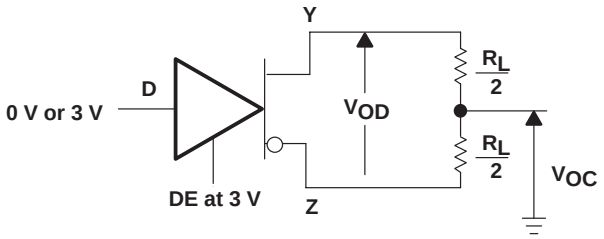


Figure 1. Differential and Common-Mode Output Voltages

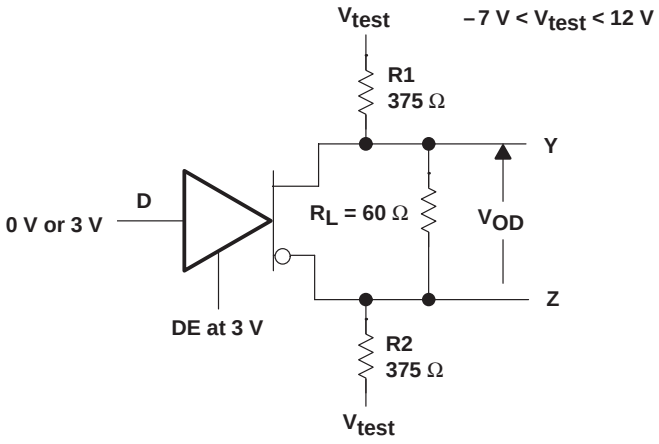
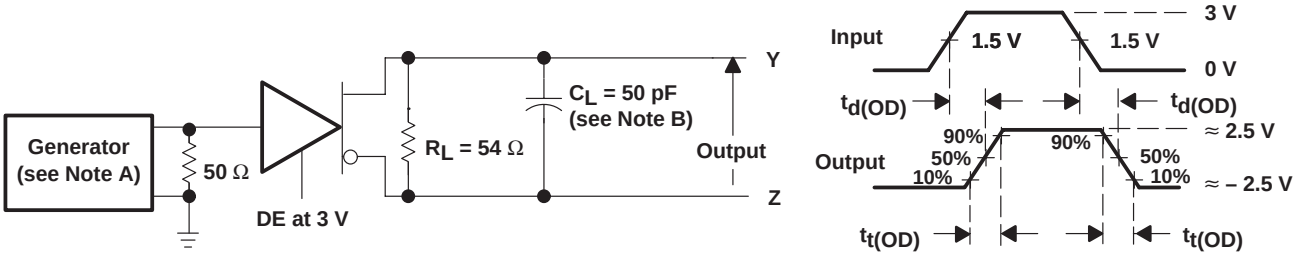


Figure 2. Driver V_{OD} Test Circuit



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

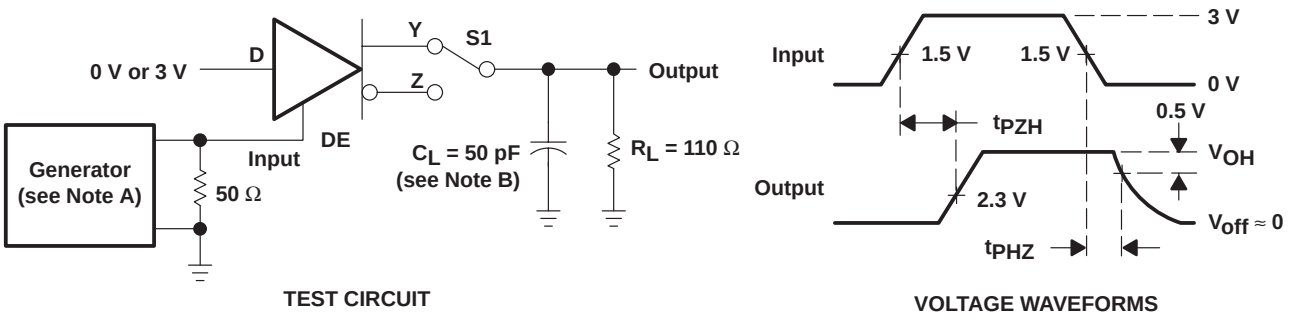


Figure 4. Driver Test Circuit and Enable and Disable Time Waveforms

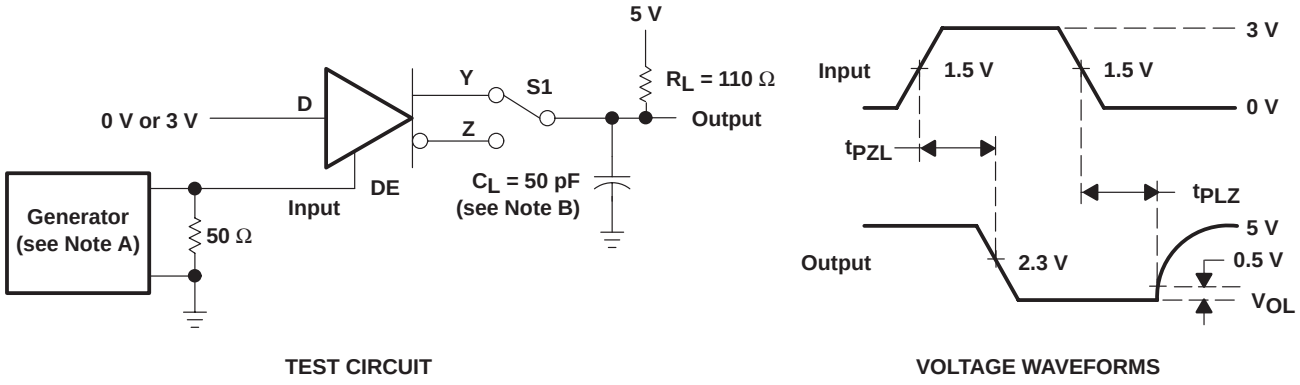
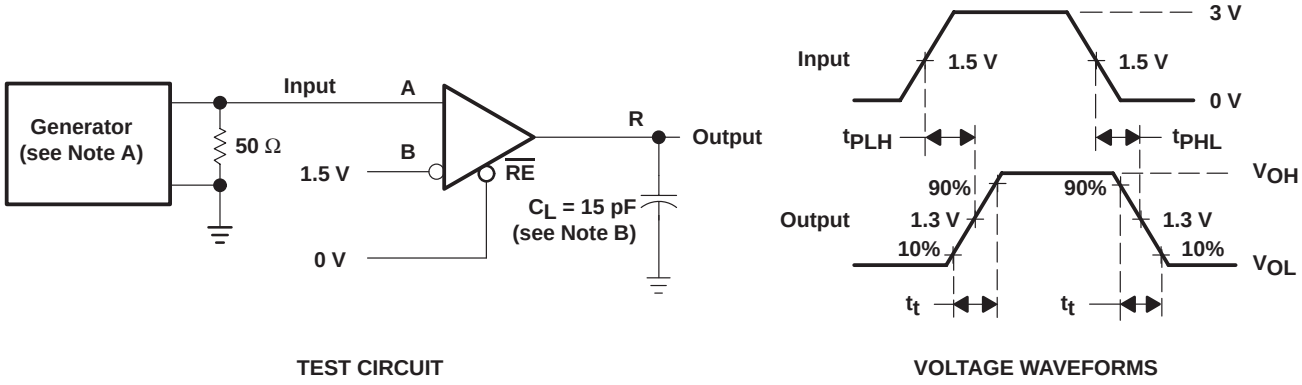


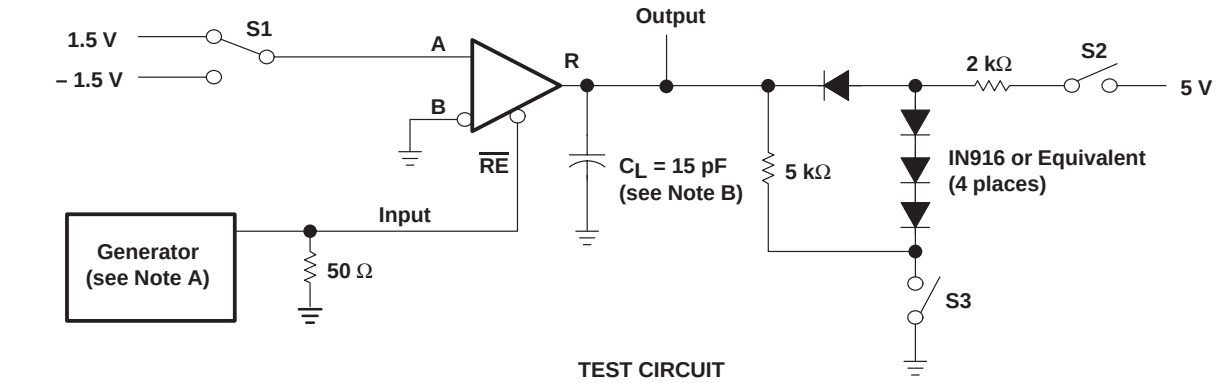
Figure 5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms



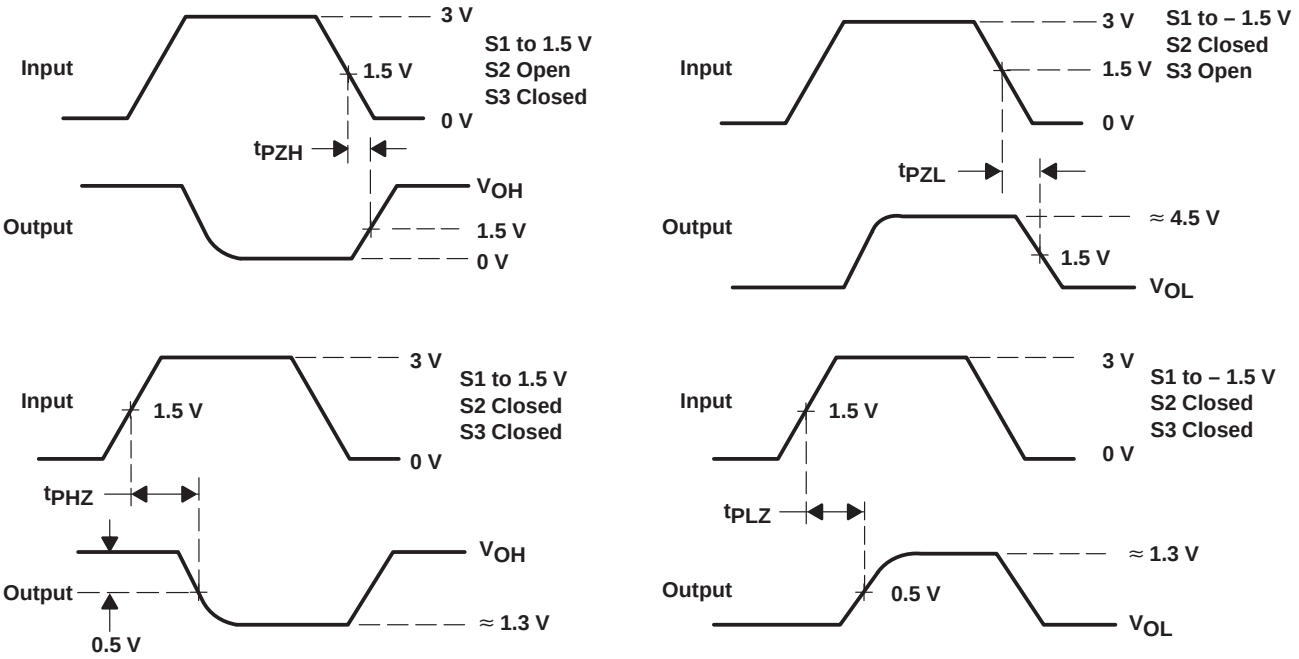
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Output Enable and Disable Times

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

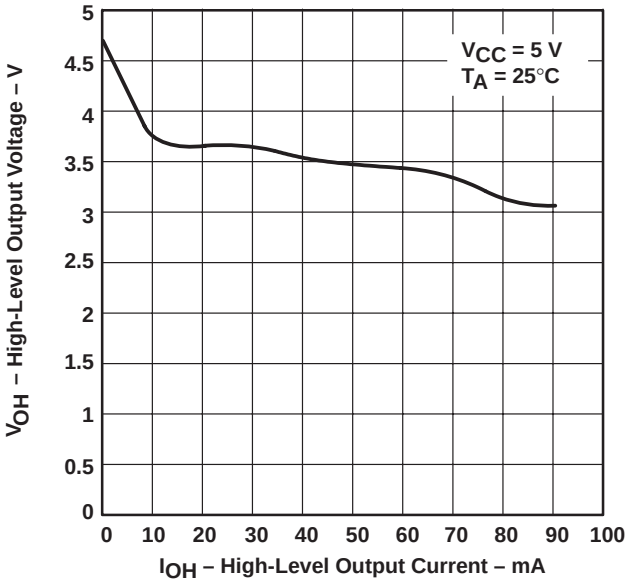


Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

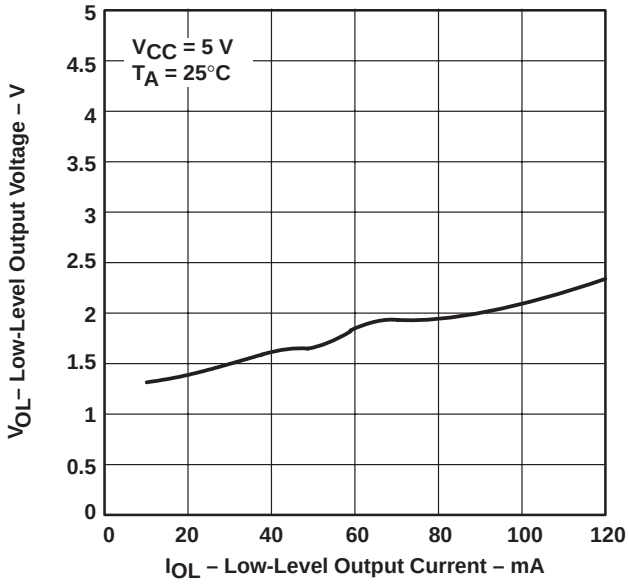


Figure 9

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

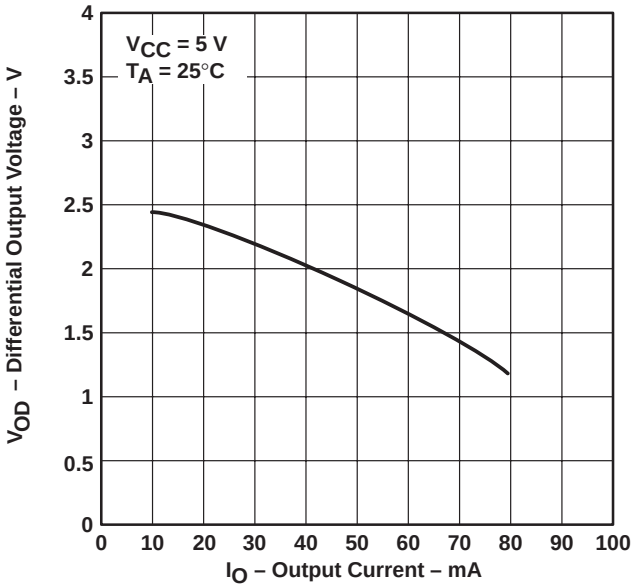


Figure 10

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

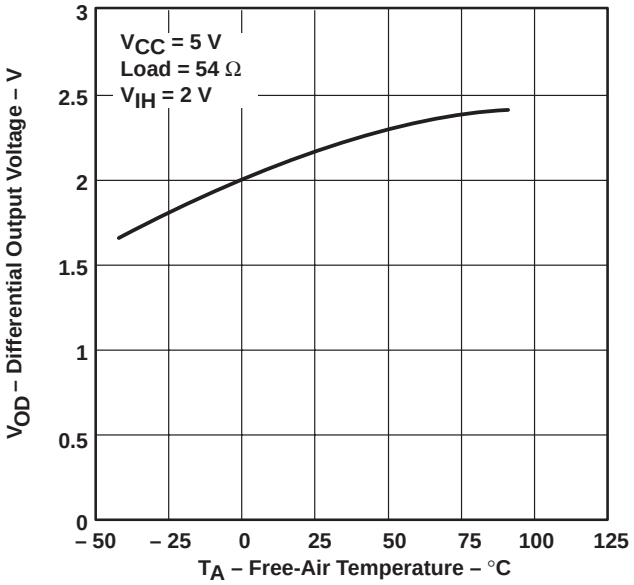


Figure 11

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL DELAY TIMES
vs
FREE-AIR TEMPERATURE

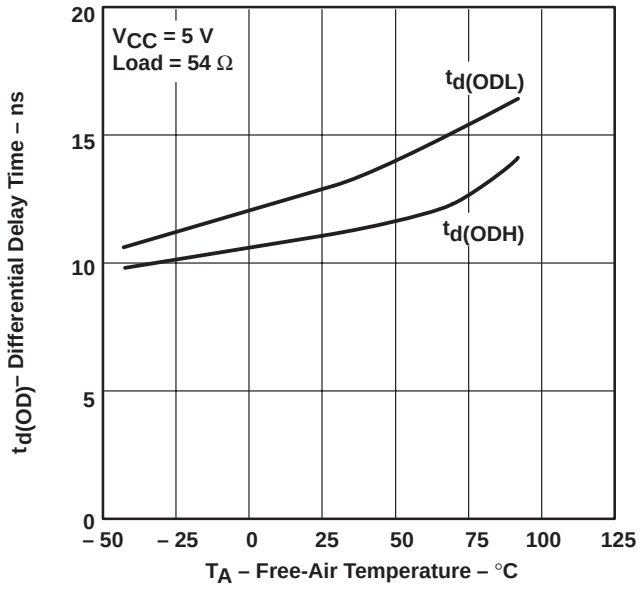


Figure 12

DRIVER
OUTPUT CURRENT
vs
SUPPLY VOLTAGE

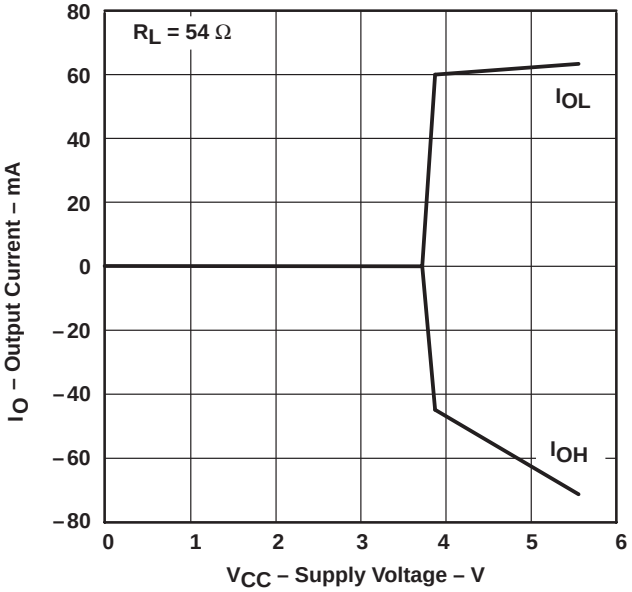


Figure 13

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

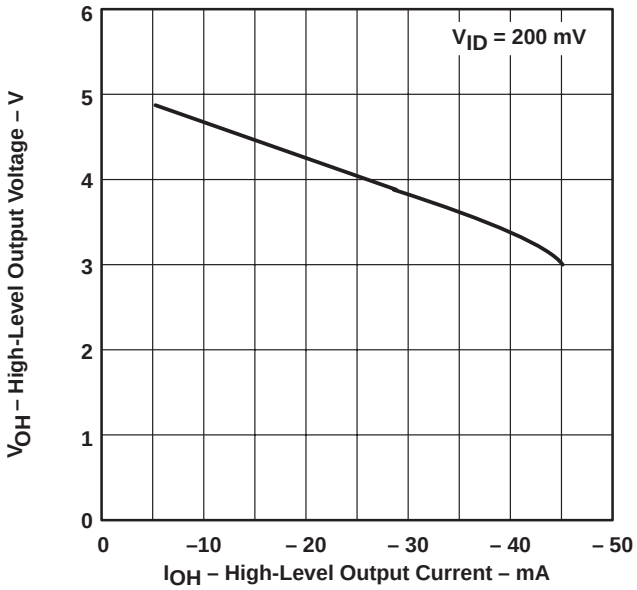


Figure 14

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

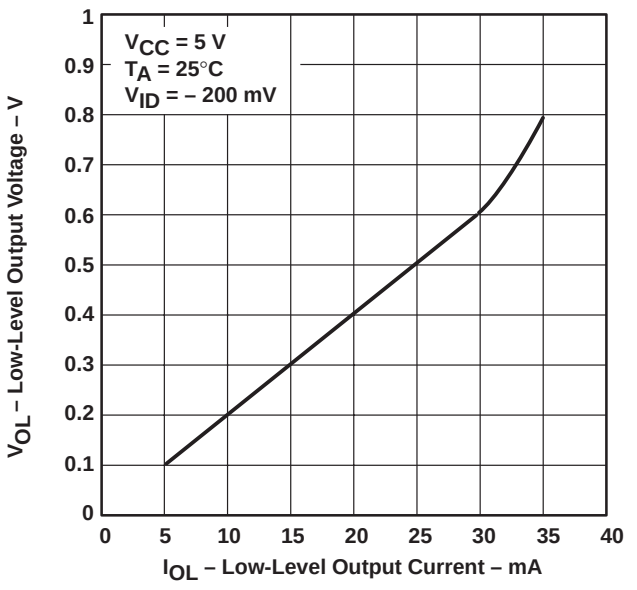


Figure 15

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

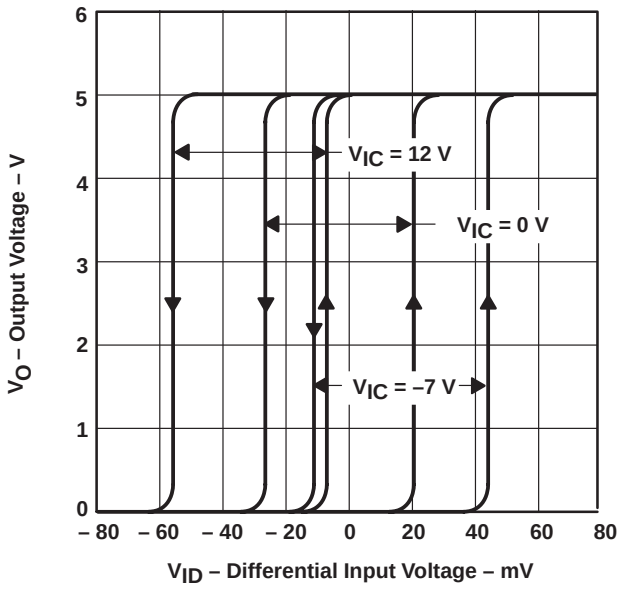


Figure 16

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

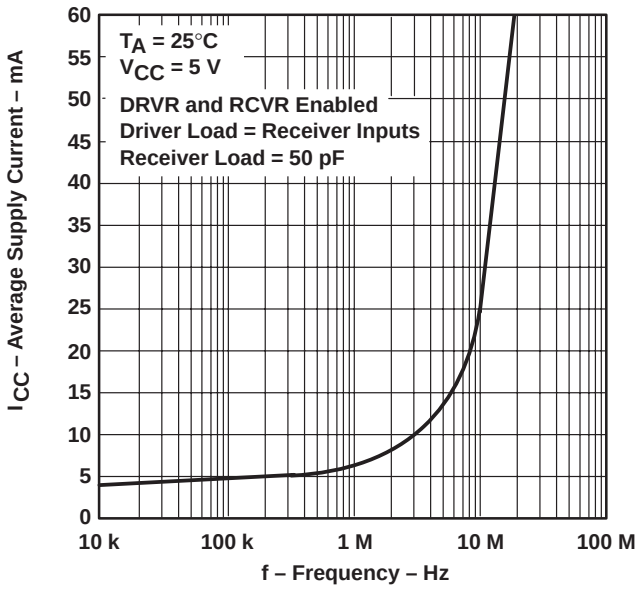


Figure 17

RECEIVER
BUS INPUT CURRENT
vs
INPUT VOLTAGE
(COMPLEMENTARY INPUT AT 0 V)

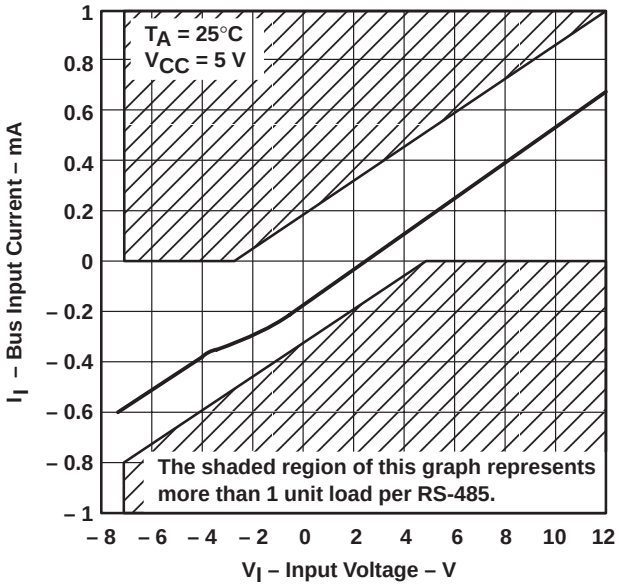


Figure 18

RECEIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

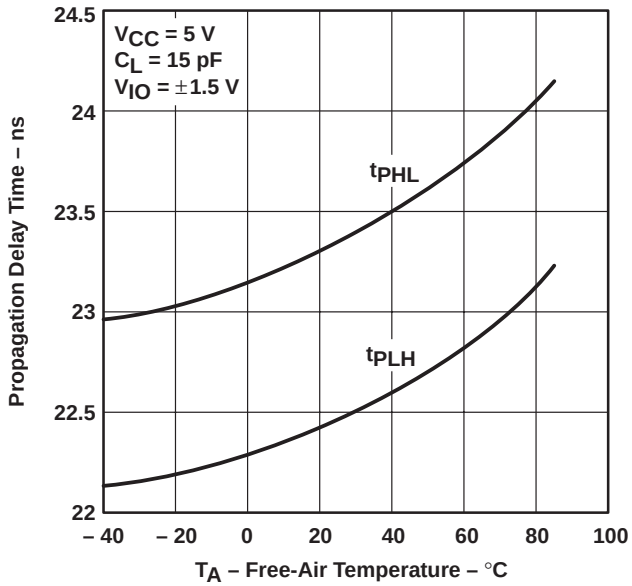
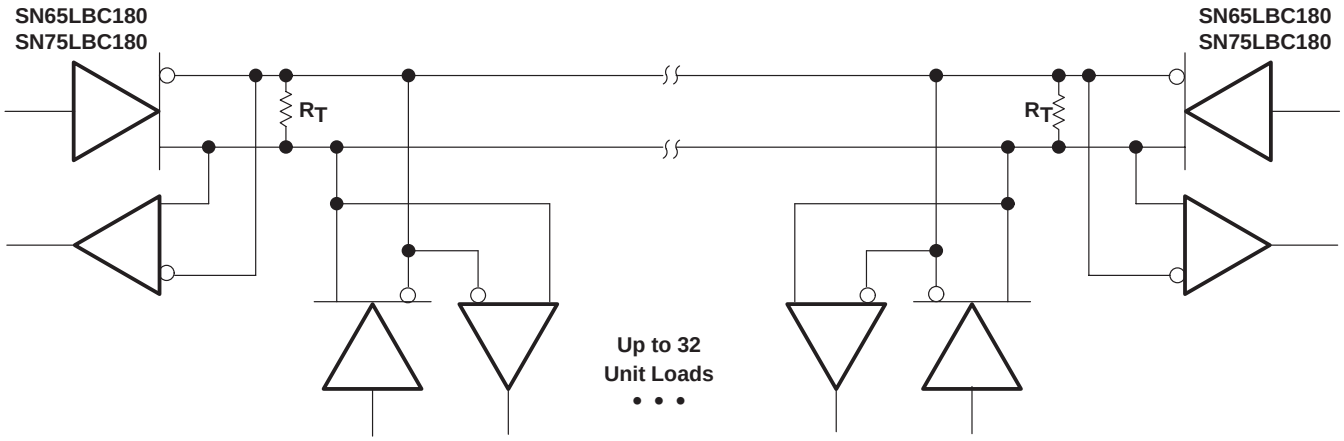


Figure 19

APPLICATION INFORMATION



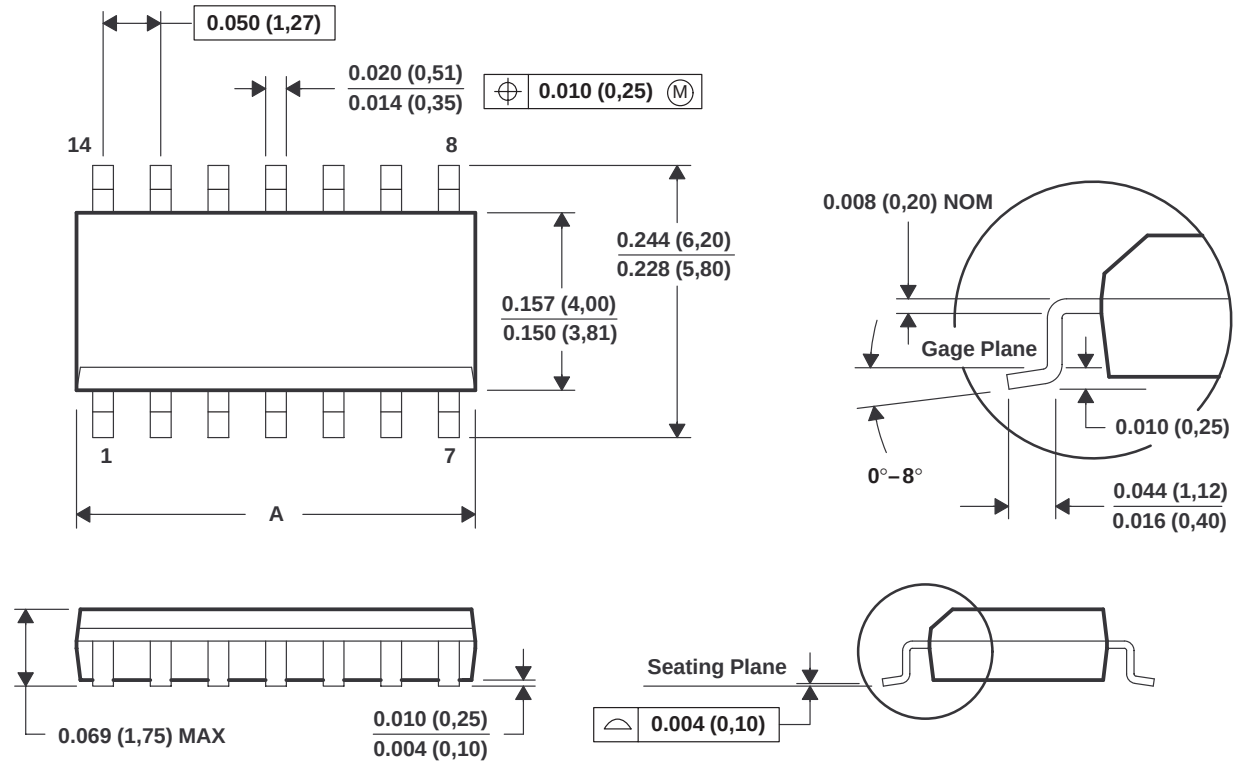
NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible. One SN75LBC180 typically represents less than one unit load.

Figure 20. Typical Application Circuit

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

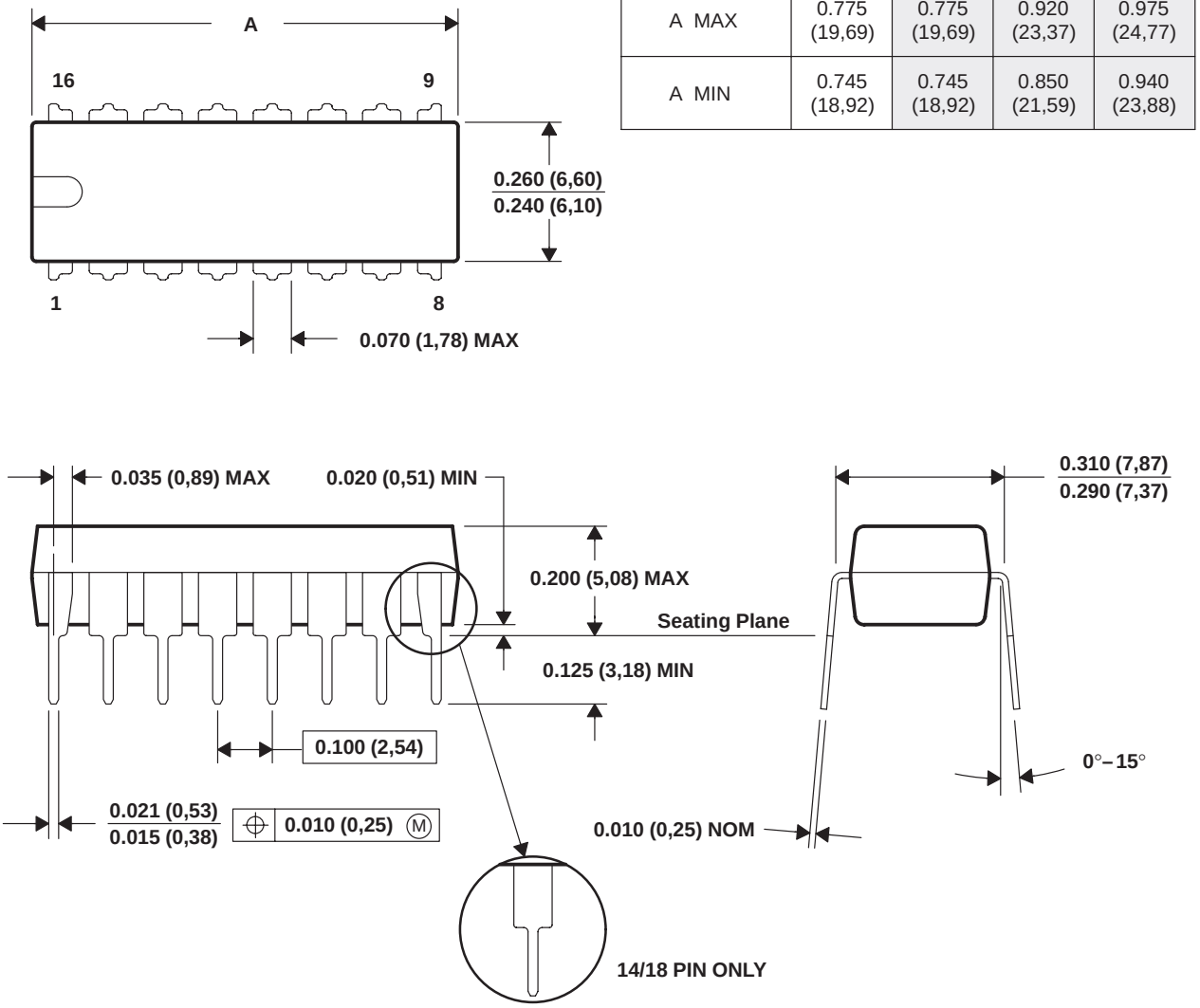
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

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