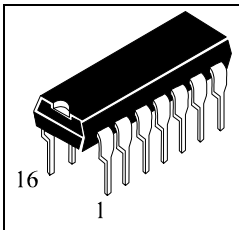
KK9151-3

PULSE DIALER

The KK9151-3 pulse dialer is a monolithic CMOS integrated circuit which converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended to replace mechanical telephone dialers and can operate directly from telephone lines. CMOS technology is used to produced this device, resulting in very low power requirements and high noise immunity. The KK9151-3 can be easily interfaced with a variety of telephones, requiring only a minimal number of external components.

- Direct telephone line operation
- 4 x 3 matrix keyboard interface
- Supply voltage range of 2.0 to 5.5 volts
- Inexpensive RC oscillator
- Low power standby mode for redialing
- 22-digit redial memory
- Redial with either * or # key
- Dialer reset for line power breaks > 200 ms
- Selectable make/break ratio
- High speed test capacity



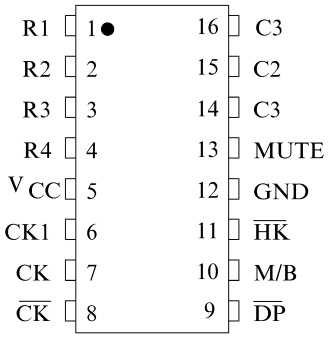
N SUFFIX
PLASTIC

ORDERING INFORMATION

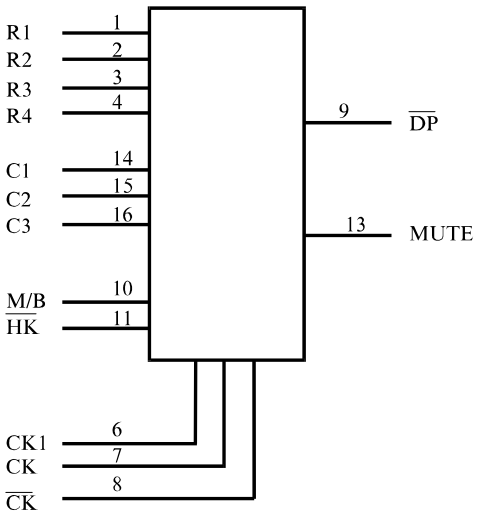
KK9151-3N Plastic

T_A = -20° to 70° C for package

PIN ASSIGNMENT



LOGIC DIAGRAM



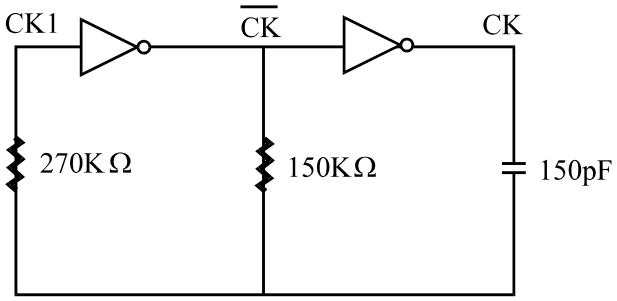
PIN 5 = V_{CC}
PIN 12 = GND

KEYBOARD ASSIGNMENT

	C1	C2	C3
R1	1	2	3
R2	4	5	6
R3	7	8	9
R4	*	0	#

(*,# : Redial)

PIN DESCRIPTION

PIN No.	NAME	DESCRIPTION
1 2 3 4 14 15 16	R1~R4 C1~C3	Key inputs. These inputs can be interfaced to either an XY matrix keyboard or a 2 of 7 type keyboard. The keypad inputs are normally held at high. When a key is depressed, scanning signals are presented at C1, C2, and C3 inputs; the dialer identifies the key by examining the R1~R4 inputs. Debouncing is provided to avoid false entry.
5 12	V_{CC} GND	Positive power supply input. Negative power supply input.
6 7 8	CK1,$\overline{CK}$, CK	Oscillator circuit input/output. The oscillator consists of two inverters, with oscillator frequency controlled by external RC components: R_{CK1}=270KΩ, R_{CK}=150KΩ, C_{CK}=150 pF  Oscillator Circuit
9	$\overline{DP}$	Dialing pulse output. This output consists of an N-channel open drain device. Normally this output will be in off state during make and on during break. Dialing pulse rate = 10pps and inter-digital pause = 800 ms when F_{OSC}=18KHz in normal mode.
10	M/B	Make/Break ratio select input. In normal mode, this input is used to select the Make/Break ratio: when input = V_{CC} , M/B ratio = 1/2. when input = GND, M/B ratio = 2/3. when connected to the clock output (pin 7), this input can trigger the IN9151-3 into test mode, generating high speed dialing.
11	$\overline{HK}$	Hook switch input. This input is used to detect whether the telephone is in the On-Hook or Off-Hook state: V_{CC}=on-hook GND=off-hook. (Resetting time = 200 ms minimum)
13	MUTE	Mute output. This output is an inverter normally at low state when there is no key entry. During outdialing it changes to high state and is used to mute the speech network.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.3 to +5.5	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.3 to V_{CC} +0.3	V
P_D	Power Dissipation in Still Air , Plastic DIP**	600	mW
Tstg	Storage Temperature	-55 to +150	°C
T_L	Lead Temperature, 1mm from case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
** Durating: -10 $^{mW}/_{°C}$ from 65°C to 70°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	5.5	V
V_{IN}	DC Input Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature	-10	+70	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND, V_{CC} = 2.0 V to5.5 V, T_A = -20 to +70°C)

Symbol	Parameter	Test Conditions	Guaranteed Limits		Unit
			Min	Max	
I_{MR}	Maximum Memory Retention Current	V_{CC}=1.0 V, HK=V_{CC} ,all outputs unloaded		1	µA
I_{CC}	Maximum Supply Operating Current	oscillator running, all outputs unloaded		200	µA
I_{SB}	Maximum Standby Current	all outputs unload HK=V_{CC}		4	µA
I_{OL}	Minimum Output Sink Current (Mute, DP)	V_{CC}=2.0V, V_{OUT}=0.5V, f=18KHz	2		mA
I_{OH}	Minimum Output Drive Current (Mute)	V_{CC}=2.0V, V_{OUT}=V_{CC}-1V, f=18KHz	1		mA
V_{IL}	Min High-Level Input Voltage		0.8V_{CC}	V_{CC}	V_{CC}
V_{IL}	Max Low-Level Input Voltage		GND	0.2V_{CC}	
I_{IN}	Max. Input Leakage Current	V_{CC}=5.5V		±1.0	µA

AC ELECTRICAL CHARACTERISTICS (F_{OSC} = 18 KHz, V_{CC}=2.0 to 5.5 V, T_A=-20 to +70°C)

Symbol	Parameter	Test Conditions	Guaranteed Limit			Unit
			Min.	Typ.	Max	
M/B	Make/Break Ratio	M/B=V_{CC}		1/2		
		M/B=GND		2/3		
DR	Dial Pulse Rate	F_{OSC}=18KHz		10		pps
		F_{OSC}=36KHz		20		
T_M	Maximum Make Time (Figure 3)	10pps	1/2		33	ms
		10pps	2/3		40	
		20pps	1/2		16.6	
		20pps	2/3		20	
T_B	Maximum Break Time (Figure 3)	10pps	1/2		66	
		10pps	2/3		60	
		20pps	1/2		33	
		20pps	2/3		30	
T_{IDP}	Maximum Inter-digital Pause Time (Figure 3)	10pps	1/2		800	
		10pps	2/3		800	
		20pps	1/2		400	
		20pps	2/3		400	
T_{PDP}	Maximum Pre-digital Pause (Figure 3)	10pps	1/2		800	
		10pps	2/3		800	
		20pps	1/2		400	
		20pps	2/3		400	
T_{MDP}	Maximum Mute Delay Time (Figure 3)	10pps	1/2		33	
		10pps	2/3		40	
		20pps	1/2		16.6	
		20pps	2/3		20	
T_{KD}	Minimum Key Debounce Time	V_{IN}=GND or V_{CC}	30			

Operation Procedures

Symbol Definitions:

D_P: pulse digit (0 through 9)
ZiZiZi: conversation
0-0↑: off-hook.
0-0↓: on-hook.
* or # : Redial

Recommended Operations:

Normal Dialing:
0-0↑; D_P ... D_P; ZiZiZi; 0-0↓
Dial pulse begins as soon as first key is entered.
Debounced and detected on chip.
Redialing:
0-0↑; * or # key
(* or # key can be accepted as first key entry after Off-Hook.)

Functional Description

1) N-channel open drain output - DP (Figure 1).
2) Clock oscillator
The clock oscillator consists of two inverters, with the frequency of oscillation controlled by external components connected to pins 6,7, and 8. The circuit is sufficiently versatile to allow the use of a variety of external component configurations. The oscillator circuit is shown in figure 2.

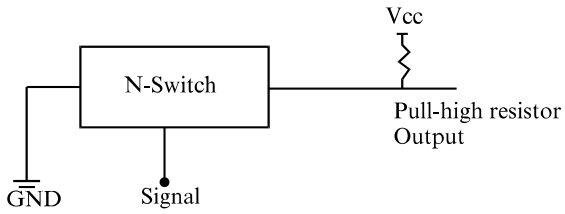


Figure 1

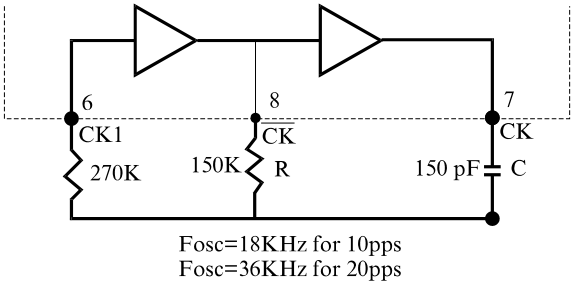
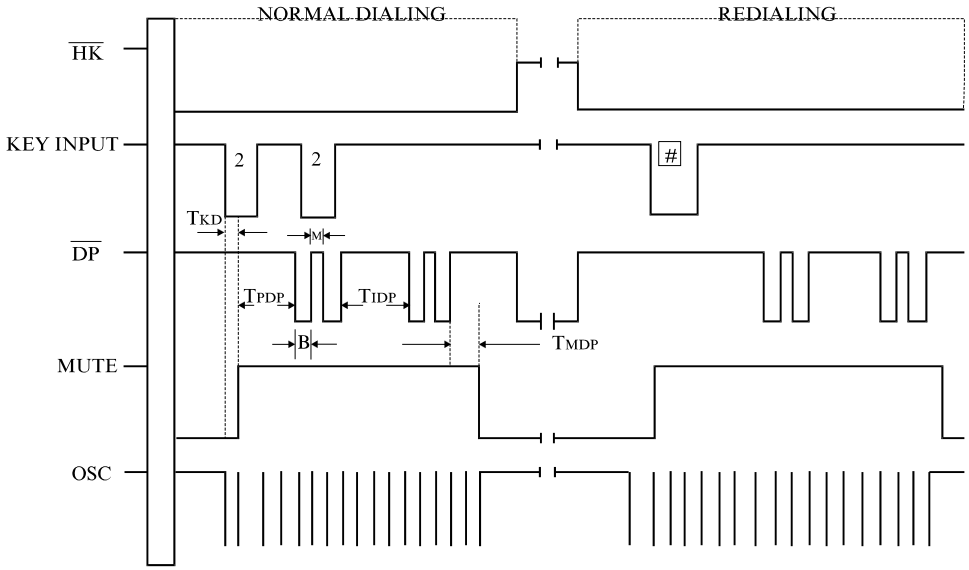
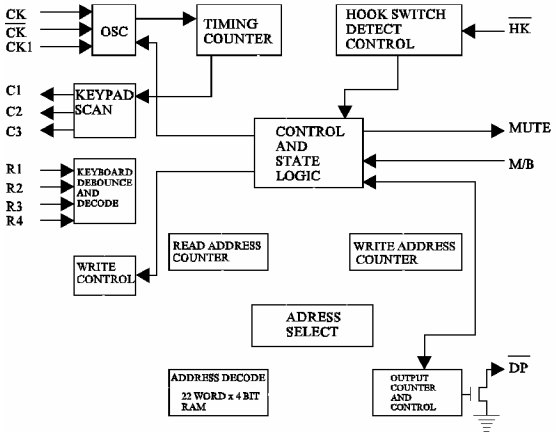


Figure 2

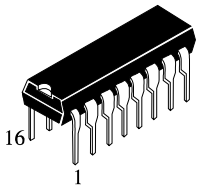
SWITCHING WAVEFORMS

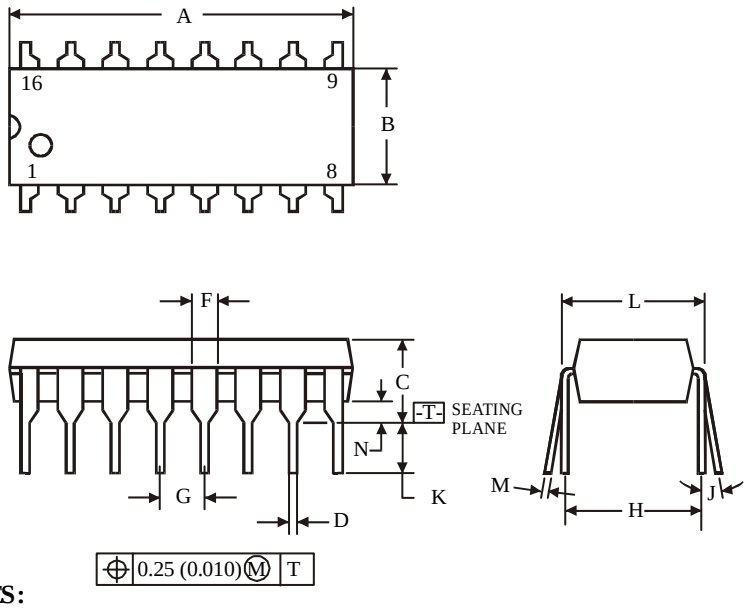


EXPANDED LOGIC DIAGRAM



N SUFFIX PLASTIC DIP
(MS - 001BB)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.