

BLM7G1822S-80AB; BLM7G1822S-80ABG

LDMOS 2-stage power MMIC

Rev. 2 — 1 July 2015

Product data sheet

1. Product profile

1.1 General description

The BLM7G1822S-80AB(G) is a dual section, asymmetric, 2-stage power MMIC using NXP's state of the art GEN7 LDMOS technology. This multiband device is perfectly suited as small cell final stage in Doherty configuration, or as general purpose driver in the 1805 MHz to 2170 MHz frequency range. Available in gull wing or straight lead outline.

Table 1. Performance

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$. Test signal: 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF; specified in a class-AB production circuit.

Test signal	f	I_{Dq1} [1]	I_{Dq2} [1]	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
single carrier W-CDMA								
carrier section	2167.5	40	120	28	4	30	24	-39.5
peaking section	2167.5	80	240	28	8	28.3	24	-36

[1] I_{Dq1} represents driver stage; I_{Dq2} represents final stage.

1.2 Features and benefits

- Designed for broadband operation (frequency 1805 MHz to 2170 MHz)
- High section-to-section isolation enabling multiple combinations
- High Doherty efficiency thanks to 2 : 1 asymmetry
- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

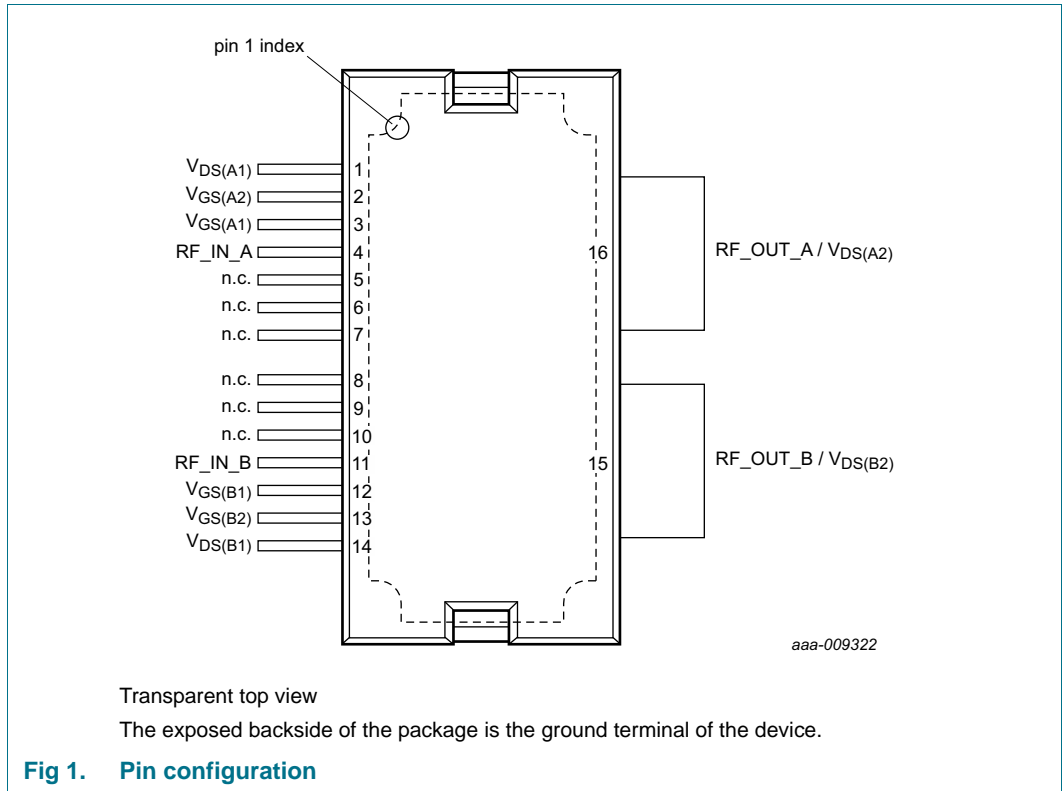
1.3 Applications

- RF power MMIC for W-CDMA base stations in the 1805 MHz to 2170 MHz frequency range. Possible circuit topologies are the following as also depicted in [Section 8.1](#):
 - ◆ Asymmetric final stage in Doherty configuration
 - ◆ Asymmetric driver for high power Doherty amplifier



2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of carrier section, driver stage (A1)
$V_{GS(A2)}$	2	gate-source voltage of carrier section, final stage (A2)
$V_{GS(A1)}$	3	gate-source voltage of carrier section, driver stage (A1)
RF_IN_A	4	RF input carrier section (A)
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
RF_IN_B	11	RF input peaking section (B)
$V_{GS(B1)}$	12	gate-source voltage of peaking section, driver stage (B1)
$V_{GS(B2)}$	13	gate-source voltage of peaking section, final stage (B2)
$V_{DS(B1)}$	14	drain-source voltage of peaking section, driver stage (B1)

Table 2. Pin description ...continued

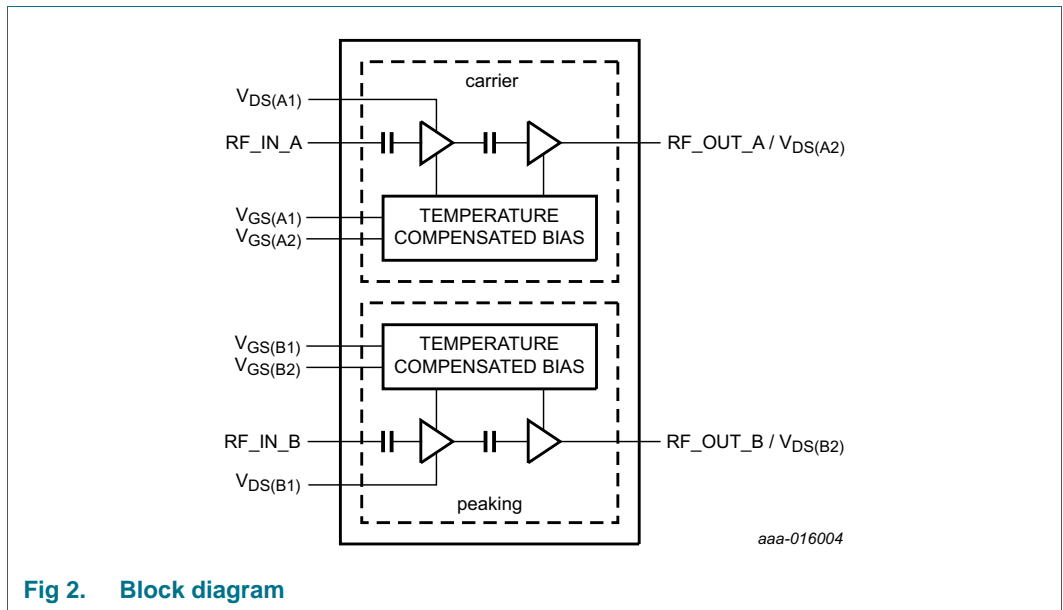
Symbol	Pin	Description
RF_OUT_B/ $V_{DS(B2)}$	15	RF output peaking section (B) / drain-source voltage of peaking section, final stage (B2)
RF_OUT_A/ $V_{DS(A2)}$	16	RF output carrier section (A) / drain-source voltage of carrier section, final stage (A2)
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLM7G1822S-80AB	HSOP16F	plastic, heatsink small outline package; 16 leads (flat)	SOT1211-2
BLM7G1822S-80ABG	HSOP16	plastic, heatsink small outline package; 16 leads	SOT1212-2

4. Block diagram



5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
Carrier section				
R _{th(j-c)}	thermal resistance from junction to case	final stage; T _{case} = 90 °C; P _L = 1.26 W [1]	2.4	K/W
		driver stage; T _{case} = 90 °C; P _L = 1.26 W [1]	7.6	K/W
Peaking section				
R _{th(j-c)}	thermal resistance from junction to case	final stage; T _{case} = 90 °C; P _L = 2.52 W [1]	1.5	K/W
		driver stage; T _{case} = 90 °C; P _L = 2.52 W [1]	5.5	K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics

T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier section						
Final stage						
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.302 mA	65	-	-	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 120 mA	1.6	2	2.45	V
		V _{DS} = 28 V; I _D = 120 mA [1]	1.9	2.6	3.3	V
ΔI _{Dq} /ΔT	quiescent drain current variation with temperature	T _{case} = -40 °C to +85 °C [1]	-	1.5	-	%
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	1.4	μA
I _{DSX}	drain cut-off current	V _{GS} = 5.55 V; V _{DS} = 10 V	-	5.4	-	A
I _{GSS}	gate leakage current	V _{GS} = 1.0 V; V _{DS} = 0 V	-	-	140	nA
Driver stage						
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.058 mA	65	-	-	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 40 mA	1.7	2.1	2.55	V
		V _{DS} = 28 V; I _D = 40 mA [2]	1.9	2.6	3.2	V
ΔI _{Dq} /ΔT	quiescent drain current variation with temperature	T _{case} = -40 °C to +85 °C [2]	-	1.5	-	%
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	1.4	μA
I _{DSX}	drain cut-off current	V _{GS} = 5.55 V; V _{DS} = 10 V	-	1.05	-	A
I _{GSS}	gate leakage current	V _{GS} = 1.0 V; V _{DS} = 0 V	-	-	140	nA
Peaking section						
Final stage						
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.604 mA	65	-	-	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 240 mA	1.6	2.15	2.6	V
		V _{DS} = 28 V; I _D = 240 mA [3]	2	3	3.8	V
ΔI _{Dq} /ΔT	quiescent drain current variation with temperature	T _{case} = -40 °C to +85 °C [3]	-	2	-	%
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	1.4	μA
I _{DSX}	drain cut-off current	V _{GS} = 5.55 V; V _{DS} = 10 V	-	11	-	A
I _{GSS}	gate leakage current	V _{GS} = 1.0 V; V _{DS} = 0 V	-	-	140	nA

Table 6. DC characteristics ...continued
T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver stage						
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.116 mA	65	-	-	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 80 mA	1.7	2.15	2.55	V
		V _{DS} = 28 V; I _D = 80 mA [4]	2	2.7	3.3	V
ΔI _{Dq} /ΔT	quiescent drain current variation with temperature	T _{case} = -40 °C to +85 °C [4]	-	2	-	%
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	1.4	μA
I _{DSX}	drain cut-off current	V _{GS} = 5.55 V; V _{DS} = 10 V	-	1.9	-	A
I _{GSS}	gate leakage current	V _{GS} = 1.0 V; V _{DS} = 0 V	-	-	140	nA

- [1] In production circuit with 825 Ω gate feed resistor.
- [2] In production circuit with 850 Ω gate feed resistor.
- [3] In production circuit with 1205 Ω gate feed resistor.
- [4] In production circuit with 460 Ω gate feed resistor.

Table 7. RF Characteristics

Typical RF performance at f = 2167.5 MHz; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 40 mA (carrier section, driver stage); I_{Dq2} = 120 mA (carrier section, final stage); P_{L(AV)} = 4 W (carrier section); I_{Dq1} = 80 mA (peaking section, driver stage); I_{Dq2} = 240 mA (peaking section, final stage); P_{L(AV)} = 8 W (peaking section) unless otherwise specified, measured in an NXP straight lead production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier section						
Test signal: single carrier W-CDMA [1]						
G _p	power gain		29.5	31	32.5	dB
η _D	drain efficiency		21	24	-	%
RL _{in}	input return loss		-	-13.5	-10	dB
ACPR _{5M}	adjacent channel power ratio (5 MHz)		-	-39.5	-36.5	dBc
PAR _O	output peak-to-average ratio		7	7.8	-	dB
Peaking section						
Test signal: single carrier W-CDMA [1]						
G _p	power gain		26.8	28.3	29.8	dB
η _D	drain efficiency		20	24	-	%
RL _{in}	input return loss		-	-20	-10	dB
ACPR _{5M}	adjacent channel power ratio (5 MHz)		-	-36	-31	dBc
PAR _O	output peak-to-average ratio		5.2	7	-	dB
Test signal: CW [2]						
Δφ _{s21}	phase response difference	normalized; between sections	-15	-	+15	deg
Δ S ₂₁ ²	insertion power gain difference	normalized; between sections	-0.6	-	+0.6	dB

- [1] 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF.
- [2] f = 2170 MHz.

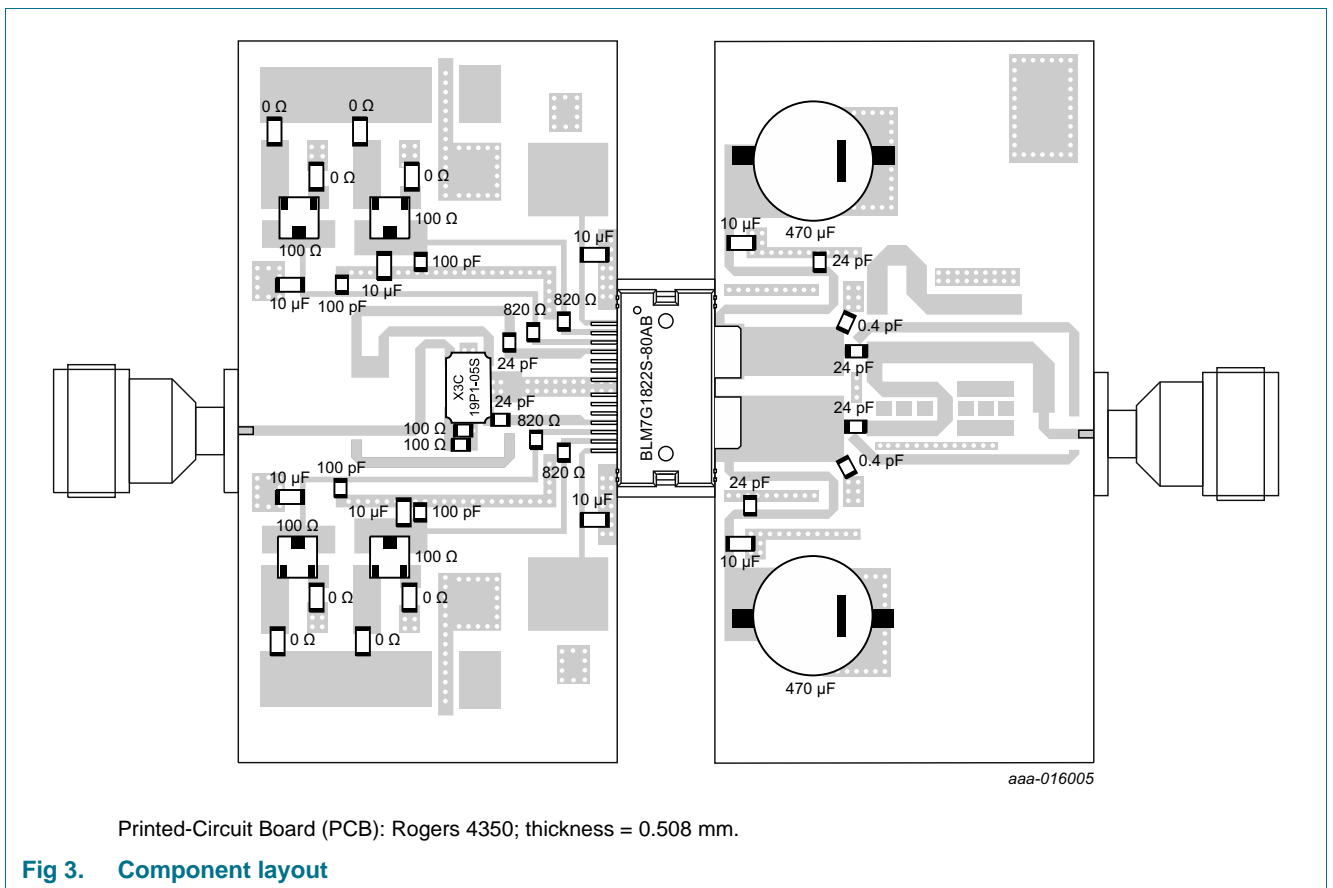
8. Application information

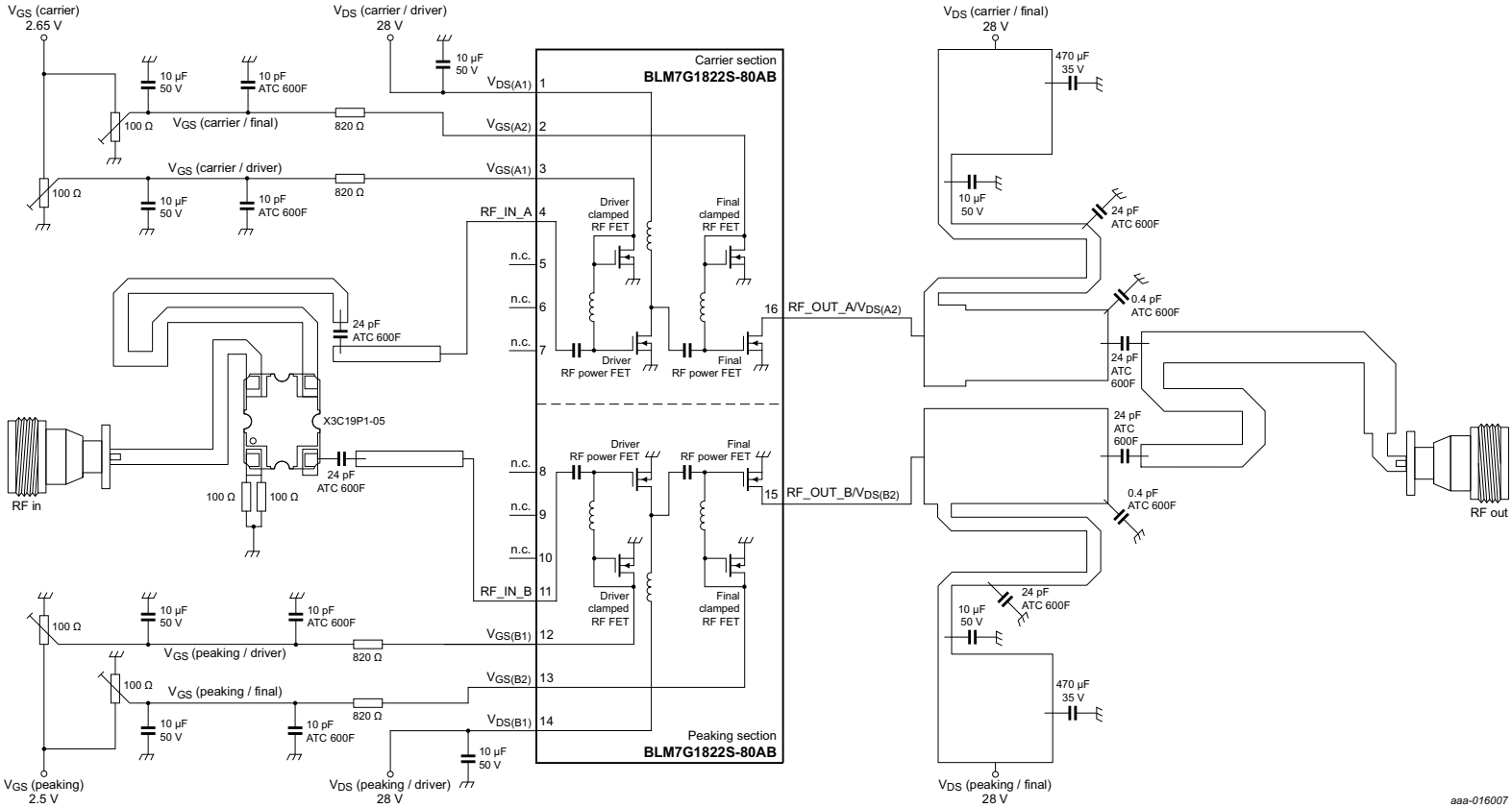
Table 8. Doherty typical performance

Test signal: 1-tone CW; RF performance at $T_{case} = 25\text{ °C}$; $V_{DS} = 28\text{ V}$; $I_{Dq1} = 40\text{ mA}$ (carrier section, driver stage); $I_{Dq2} = 90\text{ mA}$ (carrier section, final stage); $I_{Dq1} = 20\text{ mA}$ (peaking section, driver stage); $V_{GS} = 0.9\text{ V}$ (peaking section, final stage); unless otherwise specified, measured in an NXP, $f = 1805\text{ MHz}$ to 1880 MHz , Doherty application circuit (see [Figure 3](#) and [Figure 4](#)).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	$f = 1842.5\text{ MHz}$; 1-tone pulsed CW (10 % duty cycle)	-	89	-	W
η_D	drain efficiency	at $P_{L(3dB)}$; $f = 1842.5\text{ MHz}$; 1-tone pulsed CW (10 % duty cycle)	-	52.5	-	%
G_p	power gain	$P_{L(AV)} = 14.12\text{ W}$; $f = 1842.5\text{ MHz}$	-	26.3	-	dB
B_{video}	video bandwidth	$P_{L(AV)} = 6.3\text{ W}$; $f = 1842.5\text{ MHz}$; 2-tone CW	-	70	-	MHz
G_{flat}	gain flatness	$P_{L(AV)} = 14.12\text{ W}$	-	0.5	-	dB
K	Rollett stability factor	$T_{case} = -40\text{ °C}$; $f = 0.1\text{ GHz}$ to 3 GHz	[1]	> 1	-	

[1] For carrier and peaking sections (S-parameters measured with load-pull jig).





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Fig 4. Electrical schematic

8.1 Possible circuit topologies

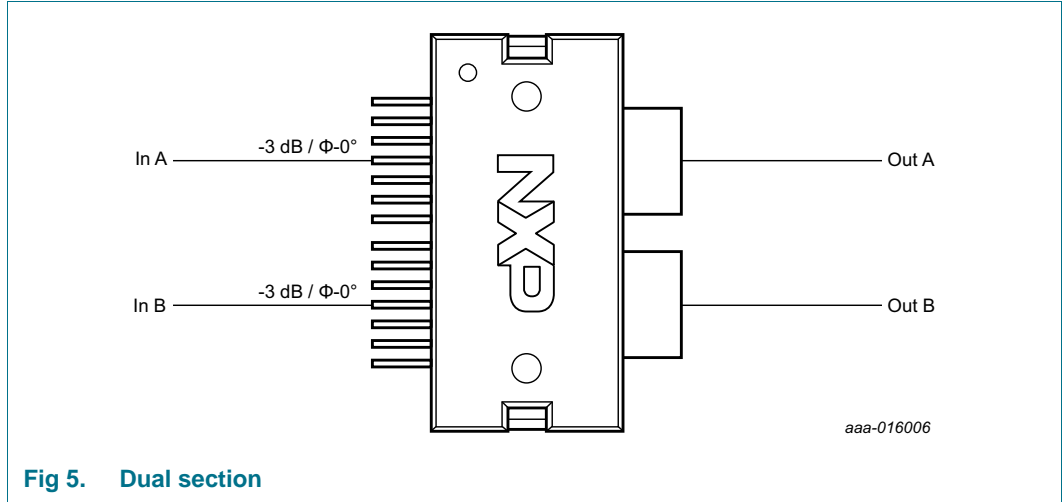


Fig 5. Dual section

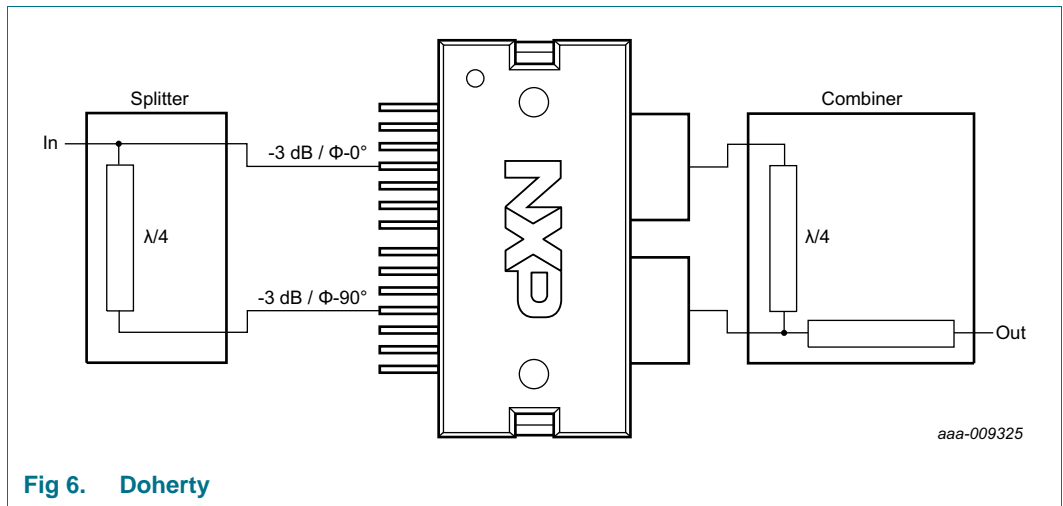


Fig 6. Doherty

8.2 Ruggedness in class-AB operation

The BLM7G1822S-80AB and BLM7G1822S-80ABG are capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $f = 2140$ MHz; $V_{DS} = 32$ V; $I_{Dq1} = 40$ mA (carrier section, driver stage); $I_{Dq2} = 120$ mA (carrier section, final stage); $I_{Dq1} = 80$ mA (peaking section, driver stage); $I_{Dq2} = 180$ mA (peaking section, final stage); $P_i = 16$ dBm (carrier section); $P_i = 22$ dBm (peaking section). P_i is measured at CW and corresponding to $P_{L(3dB)}$ under $Z_S = 50 \Omega$ load.

8.3 Impedance information

Table 9. Typical impedance

Measured load-pull data at 3 dB gain compression point; test signal: pulsed CW; $T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$; $Z_S = 50\text{ }\Omega$; $I_{Dq1} = 40\text{ mA}$ (carrier section, driver stage); $I_{Dq2} = 110\text{ mA}$ (carrier section, final stage); $I_{Dq1} = 80\text{ mA}$ (peaking section, driver stage); $I_{Dq2} = 200\text{ mA}$ (peaking section, final stage). Typical values unless otherwise specified.

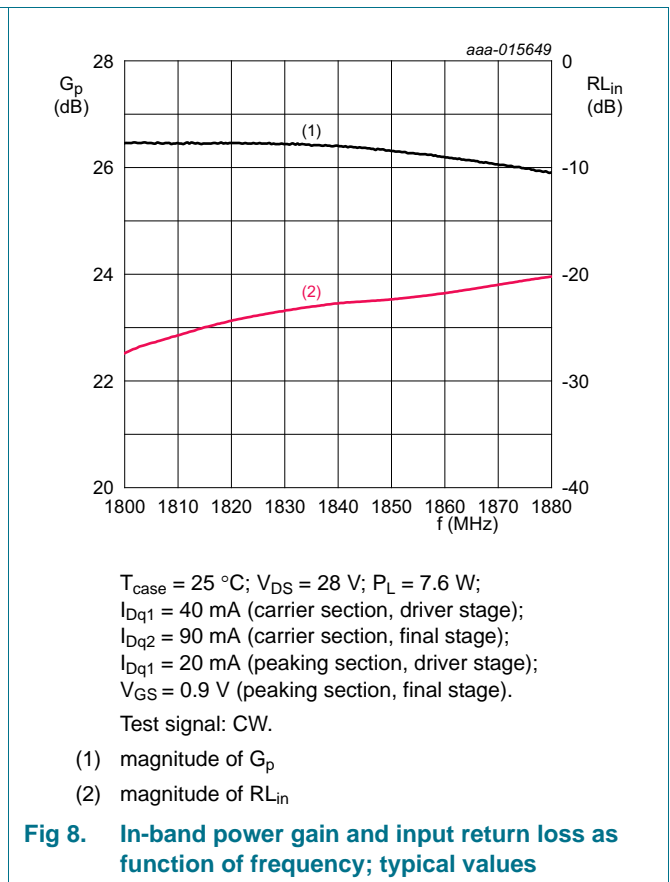
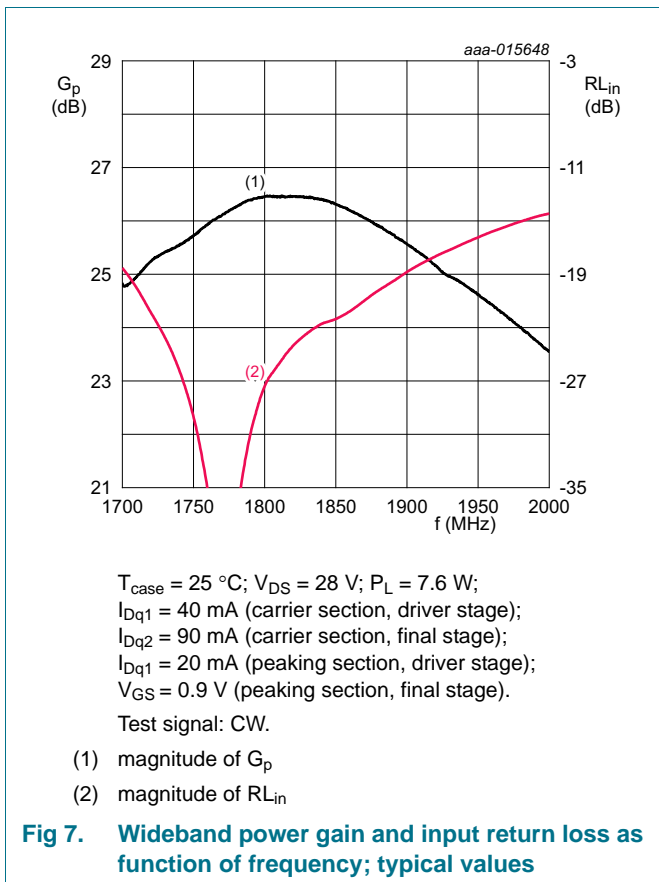
f	tuned for maximum output power					tuned for maximum power added efficiency				
	Z _L	G _{p(max)}	P _L	η_{add}	AM-PM conversion	Z _L	G _{p(max)}	P _L	η_{add}	AM-PM conversion
(MHz)	(Ω)	(dB)	(W)	(%)	(deg)	(Ω)	(dB)	(W)	(%)	(deg)
Carrier section										
BLM7G1822S-80AB										
1805	7.7 – j10.6	32.2	45.8	51	0.3	16.7 – j4.2	33.5	43.9	58.8	–4.9
1842.5	7.8 – j10.6	32.3	45.8	51.8	0.9	16.2 – j5.6	33.4	44	58.5	–3
1880	7.7 – j10.6	32.3	45.8	52.1	1.4	12.2 – j4.6	33.4	44.5	58.4	–2.8
1930	6.7 – j10.8	32	45.7	48.8	0.3	11.6 – j3.4	33.5	44.1	57.7	–4.3
1960	7.8 – j10.6	32.6	45.7	51.4	1.6	9.9 – j4.4	33.6	44.6	57.6	–2.3
1990	6.3 – j9.5	32.5	45.7	49.1	0.5	8.6 – j4.3	33.6	44.6	57	–3.1
2110	6.3 – j9.5	33	45.8	51.4	–4	7.3 – j4.8	33.8	44.6	56.4	–4.4
2140	6.3 – j9.5	33	45.7	51.8	–5.9	7.3 – j4.8	33.8	44.5	56.2	–5.4
2170	6.8 – j10.8	32.8	45.6	50.1	–7.5	7.0 – j6.3	33.6	44.9	56.5	–7
BLM7G1822S-80ABG										
1805	8.0 – j13.4	31.8	45.8	50.3	–1.7	14.8 – j8.7	33	44.6	58.1	–5.5
1842.5	8.0 – j13.4	31.9	45.8	49.2	–1	16.3 – j4.3	33.3	44.7	57.5	–7.4
1880	8.0 – j13.4	32.1	45.8	50	–0.3	12.7 – j7.1	33.2	44.5	57.3	–4.3
1930	8.0 – j13.4	32.1	45.8	50.3	–0.6	12.8 – j7.3	33.2	44.4	56.3	–3.4
1960	8.0 – j13.4	32.4	45.7	49.9	–0.4	11.1 – j6.8	33.5	44.5	56.1	–3.6
1990	7.7 – j15.2	32.2	45.7	47	–0.7	9.0 – j7.7	33.4	44.8	55.9	–3.4
2110	8.1 – j13.4	33	45.8	52.1	–6.1	7.6 – j8.0	33.6	44.7	56.1	–6.7
2140	6.5 – j12.8	32.7	45.7	50.8	–8.9	7.6 – j8.0	33.5	44.5	55.7	–7.7
2170	7.0 – j14.1	32.4	45.6	49.1	–10	8.6 – j9.0	33.3	44.8	55.8	–7.8
Peaking section										
BLM7G1822S-80AB										
1810	2.6 – j5.9	29.2	48.6	49.6	–2.7	5.4 – j5.1	30.3	47.4	56.4	–5.6
1840	2.7 – j5.8	29.9	48.5	49.3	–3.8	4.9 – j4.8	30.9	47.5	56.3	–6.2
1880	2.6 – j5.8	29.6	48.5	48.5	–2.4	4.8 – j4.3	30.6	47.4	55.3	–5
1930	2.6 – j5.8	29.9	48.4	47.9	–1.1	4.3 – j4.2	30.8	47.4	54.3	–2.9
1960	2.6 – j5.8	29.9	48.4	48	–1	4.2 – j4.2	30.8	47.5	54.3	–2.2
1990	2.6 – j5.7	29.6	48.3	47.5	–2.1	3.6 – j4.0	30.4	47.4	53.8	–3.9
2110	2.6 – j5.8	29.8	48.3	48.3	–3.6	3.1 – j4.1	30.2	47.4	52.6	–4.7
2140	2.6 – j5.8	29.8	48.3	48.6	–4.1	3.1 – j4.7	30.3	47.6	51.9	–3.9
2170	2.6 – j5.8	29.5	48.2	46	–5.4	2.6 – j4.7	30.1	47.5	51.2	–6.4

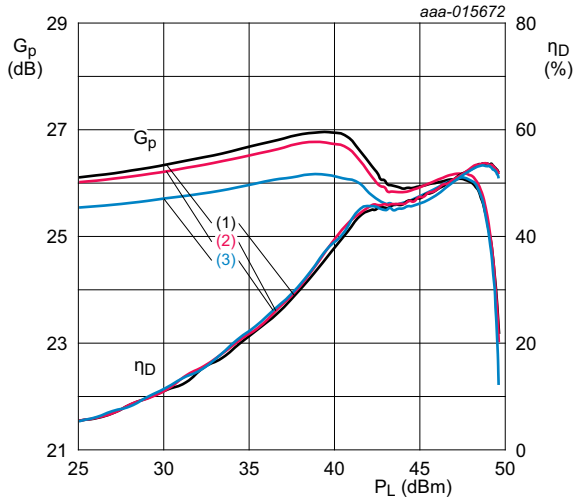
Table 9. Typical impedance ...continued

Measured load-pull data at 3 dB gain compression point; test signal: pulsed CW; $T_{case} = 25\text{ °C}$; $V_{DS} = 28\text{ V}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\%$; $Z_S = 50\text{ }\Omega$; $I_{Dq1} = 40\text{ mA}$ (carrier section, driver stage); $I_{Dq2} = 110\text{ mA}$ (carrier section, final stage); $I_{Dq1} = 80\text{ mA}$ (peaking section, driver stage); $I_{Dq2} = 200\text{ mA}$ (peaking section, final stage). Typical values unless otherwise specified.

f	tuned for maximum output power					tuned for maximum power added efficiency				
	Z _L	G _{p(max)}	P _L	η_{add}	AM-PM conversion	Z _L	G _{p(max)}	P _L	η_{add}	AM-PM conversion
(MHz)	(Ω)	(dB)	(W)	(%)	(deg)	(Ω)	(dB)	(W)	(%)	(deg)
BLM7G1822S-80ABG										
1810	3.0 – j8.9	29.3	48.4	50.6	-1.7	5.3 – j7.6	30.3	47.5	57.5	-5.3
1840	2.7 – j8.7	29.1	48.3	48.4	-4.4	5.0 – j7.5	30.2	47.5	56.9	-7.5
1880	3.0 – j8.8	29.4	48.4	50.5	-2.3	4.7 – j7.1	30.3	47.4	56.4	-5.1
1930	2.7 – j9.0	29.6	48.4	48.7	-2.7	4.4 – j7.0	30.6	47.4	56.1	-5.5
1960	2.7 – j9.0	29.6	48.4	48.7	-2.7	4.0 – j6.8	30.6	47.4	55.9	-5.3
1990	2.7 – j8.9	29.7	48.4	48	-2	3.8 – j7.1	30.6	47.5	55	-3.7
2110	2.7 – j9.5	29.9	48.5	49.5	-3.4	2.8 – j7.6	30.6	47.6	54.9	-4.2
2140	2.6 – j9.5	29.9	48.3	49.1	-4	2.6 – j7.9	30.5	47.6	53.7	-3.2
2170	2.4 – j9.7	29.7	48.3	47.4	-5.5	2.6 – j8.2	30.5	47.7	53	-4.6

8.4 Graphs



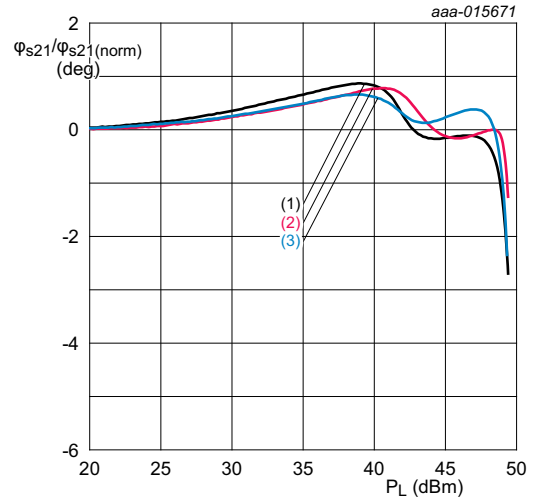


$T_{case} = 25\text{ }^\circ\text{C}$; $V_{DS} = 28\text{ V}$;
 $I_{Dq1} = 40\text{ mA}$ (carrier section, driver stage);
 $I_{Dq2} = 90\text{ mA}$ (carrier section, final stage);
 $I_{Dq1} = 20\text{ mA}$ (peaking section, driver stage);
 $V_{GS} = 0.9\text{ V}$ (peaking section, final stage).

Test signal: pulsed CW ($t_p = 200\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$).

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1842.5\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

Fig 9. Power gain and drain efficiency as function of output power; typical values

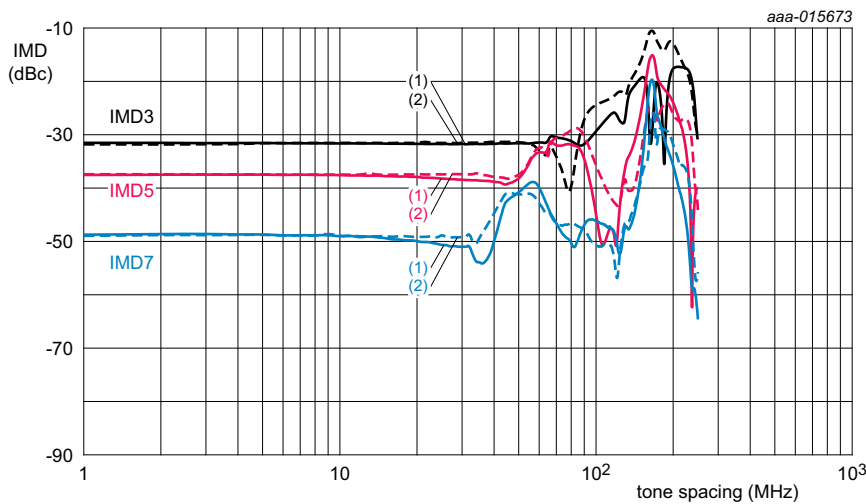


$T_{case} = 25\text{ }^\circ\text{C}$; $V_{DS} = 28\text{ V}$;
 $I_{Dq1} = 40\text{ mA}$ (carrier section, driver stage);
 $I_{Dq2} = 90\text{ mA}$ (carrier section, final stage);
 $I_{Dq1} = 20\text{ mA}$ (peaking section, driver stage);
 $V_{GS} = 0.9\text{ V}$ (peaking section, final stage).

Test signal: pulsed CW ($t_p = 200\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$).

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1842.5\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

Fig 10. Normalized phase response as a function of output power; typical values

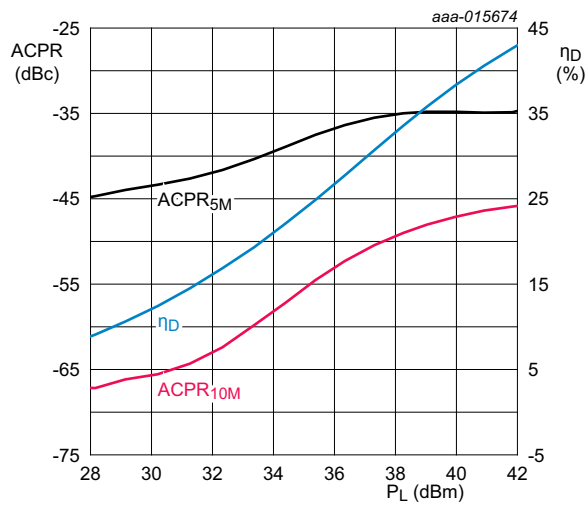


$T_{case} = 25\text{ }^\circ\text{C}$; $V_{DS} = 28\text{ V}$; $I_{Dq1} = 40\text{ mA}$ (carrier section, driver stage); $I_{Dq2} = 90\text{ mA}$ (carrier section, final stage);
 $I_{Dq1} = 20\text{ mA}$ (peaking section, driver stage); $V_{GS} = 0.9\text{ V}$ (peaking section, final stage).

Test signal: 2-tone CW ($f_c = 1842.5\text{ MHz}$).

- (1) IMD low
- (2) IMD high

Fig 11. Intermodulation distortion as a function of tone spacing; typical values



$T_{case} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 28\text{ V}$; $I_{Dq1} = 40\text{ mA}$ (carrier section, driver stage); $I_{Dq2} = 90\text{ mA}$ (carrier section, final stage);
 $I_{Dq1} = 20\text{ mA}$ (peaking section, driver stage); $V_{GS} = 0.9\text{ V}$ (peaking section, final stage).
 Test signal: 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF; $f = 1842.5\text{ MHz}$.

Fig 12. Adjacent channel power ratio and drain efficiency as function of output power; typical values

9. Package outline

HSOP16F: plastic, heatsink small outline package; 16 leads(flat)

SOT1211-2

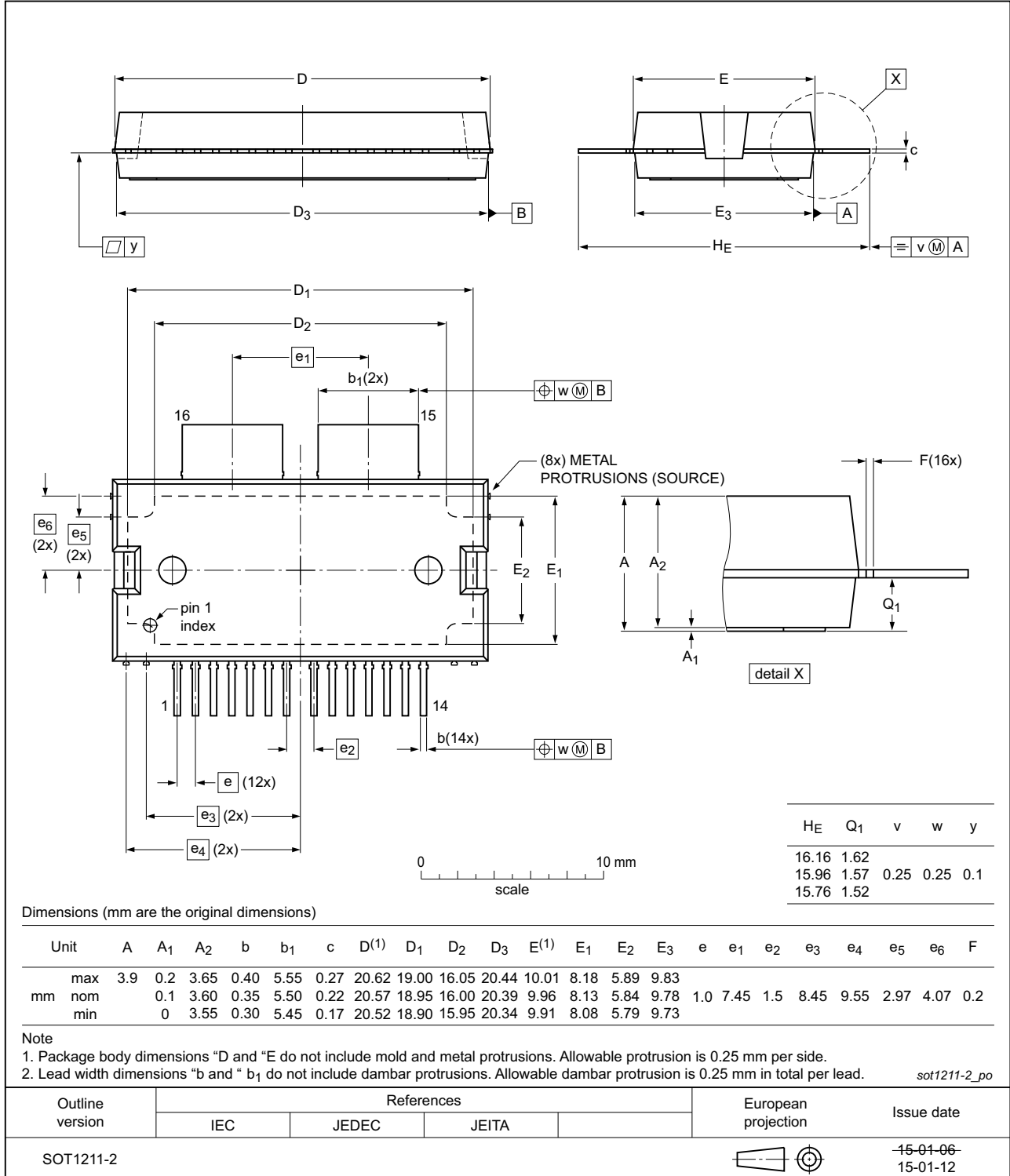


Fig 13. Package outline SOT1211-2 (HSOP16F)

HSOP16: plastic, heatsink small outline package; 16 leads

SOT1212-2

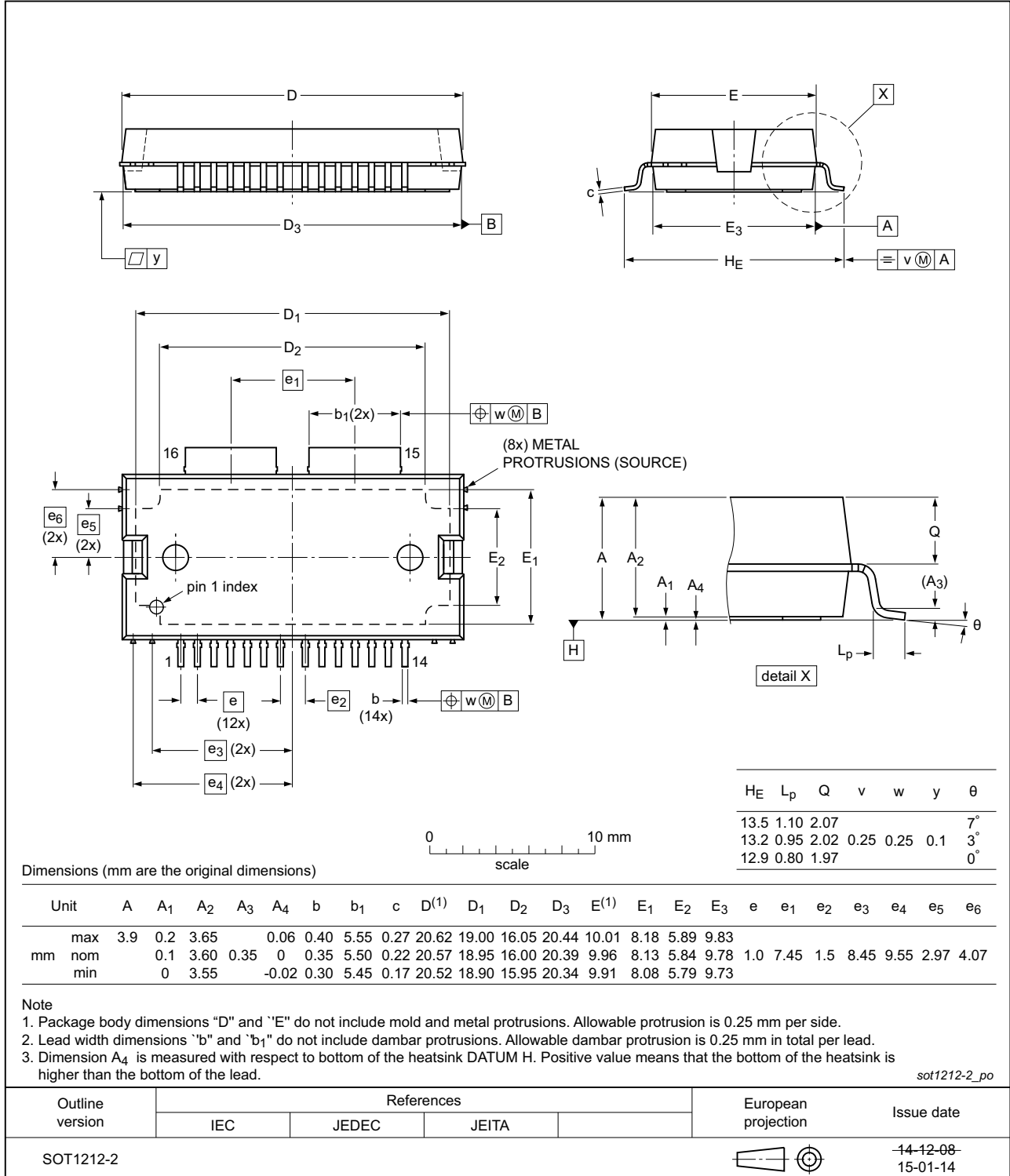


Fig 14. Package outline SOT1212-2 (HSOP16)

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
AM	Amplitude Modulation
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GEN7	Seventh Generation
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
PM	Phase Modulation
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM7G1822S-80AB_S-80ABG v.2	20150701	Product data sheet	-	BLM7G1822S-80AB_S-80ABG v.1
Modifications:		<ul style="list-style-type: none"> • Table 3 on page 3: the package version of the BLM7G1822S-80AB has been changed to SOT1211-2 • Table 3 on page 3: the package version of the BLM7G1822S-80ABG has been changed to SOT1212-2 • Figure 13 on page 13: the figure now shows the SOT1211-2 package outline • Figure 14 on page 14: the figure now shows the SOT1212-2 package outline 		
BLM7G1822S-80AB_S-80ABG v.1	20141128	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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