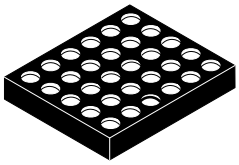
ONA10IV

16 Watt Digital Input Class-D Audio Amplifier with Speaker Sense Digital Output

ON Semiconductor®

www.onsemi.com



WLCSP30
CASE 567VB

Description

The ONA10IV is a digital input, mono Class−D audio amplifier with real time, integrated current and voltage sensing of the loudspeaker it's driving. This sense data is transmitted to the host through a separate digital output.

The ONA10IV can be directly connected to a 2−cell (2S) or 3−cell (3S) battery and offers a fast automatic gain control (AGC) for brownout protection that can react within 10 μs.

Up to eight devices can share the digital audio interfaces through I^2C control. A separate bus (MAGC) is used to synchronize gain across multiple ONA10IV instantiations during a brownout protection event.

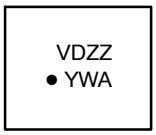
Key Features

- Filter−less, Mono Class−D Amplifier
  - 16 W into 4 Ω / 14 V Supply (1% THD+N)
  - 13.8 W into 4 Ω / 12 V Supply (1% THD+N)
  - 500 μV "Click and Pop" Suppression
  - 42 μV_{RMS} Noise Floor (A−Weighted)
  - No Boost Capacitors Required
- Speaker Voltage & Current Sense
  - Up to 20 kHz Bandwidth
  - 81 / 71 dBA Dynamic Range (Voltage / Current)
  - 0.5% V/I Gain Error Variation
- Digital Audio / Sense Configurations
  - 16 kHz to 96 kHz Audio Sampling Rates
  - 16−, 24−, and 32−Bit I^2S Data
  - 16−, 24−, and 32−Bit TDM Data (up to 8 Slots)
  - Selectable PCM or PDM Format
- I^2C Fast Mode (up to 1 MHz) Control
- EMI Reduction Controls
- Over Current and Thermal Protection
- PVDD Power Supply: 5.5 V to 14 V
- DVDD Power Supply: 1.62 V to 1.98 V
- 30−Bump WLCSP
  - 2.31 mm x 2.89 mm, 0.4mm pitch
- This is a Pb−Free Device

Applications

- Laptops, Smart Speakers, Portable Speakers, and Other IoT Devices

MARKING DIAGRAM



VD = Specific Device Code
ZZ = Wafer Lot
YW = Date Code
A = Assembly Location

ORDERING INFORMATION

Device	Package	Shipping†
NCA−ONA10IVUCX	WLCSP30 (Pb−Free)	3000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Capabilities

- *Filter−less Class D Amplifier:* Capable of operating off of direct 2−cell (2S) or 3−cell (3S) battery connection or a regulated supply from 5.5 V to 14 V.
- *Current and Voltage Speaker Sensing:* Able to sense up to 20 kHz with low gain error variation.
- *TDM / I2S Digital Audio Input:* Programmable interface that can support 16 kHz to 96 kHz sample rates with up to eight 16− to 32−bit input slots. Ability to select CKI active edge as well as FRCK polarity, delay, and pulse mode.
- *PDM Digital Audio Input/Output:* Ability to bypass embedded digital filters and drive/sense the speaker using pulse density modulation (PDM) interface.
- *TDM / I2S Digital Sense Path Output:* Can provide die temperature, current and voltage speaker sense data in up to 8 slots.
- *Volume Control:* Ability to adjust volume in 0.375 dB steps and automatically ramp on start up or shut down using 4 different rates.
- *Amplifier Gain:* Independently adjustable for PCM or PDM mode.
- *EMI Reduction Controls:* 4 selectable edge rates and 8 spread spectrum modes to accommodate EMI reduction per system needs.
- *Brownout Protection:* Fast reaction of less than 10 μs with ability to customize attack threshold for a 2−cell or 3−cell battery. Maximum attenuation as well as attack, hold, and release timing programming available to adjust the dynamic response to a brownout event.
- *MAGC Synchronous Gain Adjustments:* Dedicated bus to synchronize multiple chip instantiations to within 0.5 dB.
- *Fatal Protections:* Includes output over−current, supply under−voltage, clock error, and chip over−temperature protections that are always on when the amplifier is active. The ONA10IV can recover from each fatal protection automatically without host intervention.
- *Interrupt Flags:* Indicate when a fatal protection, brownout protection, or thermal foldback is active.
- *Thermal Foldback:* Ability to customize the chip's thermal response to elevated die temperature using four programmable thresholds. Attack, hold, and release timing customization also available.
- *Power Reduction Options:* Ability to disable features like IV sensing, brownout protection, and thermal foldback to reduce power consumption.

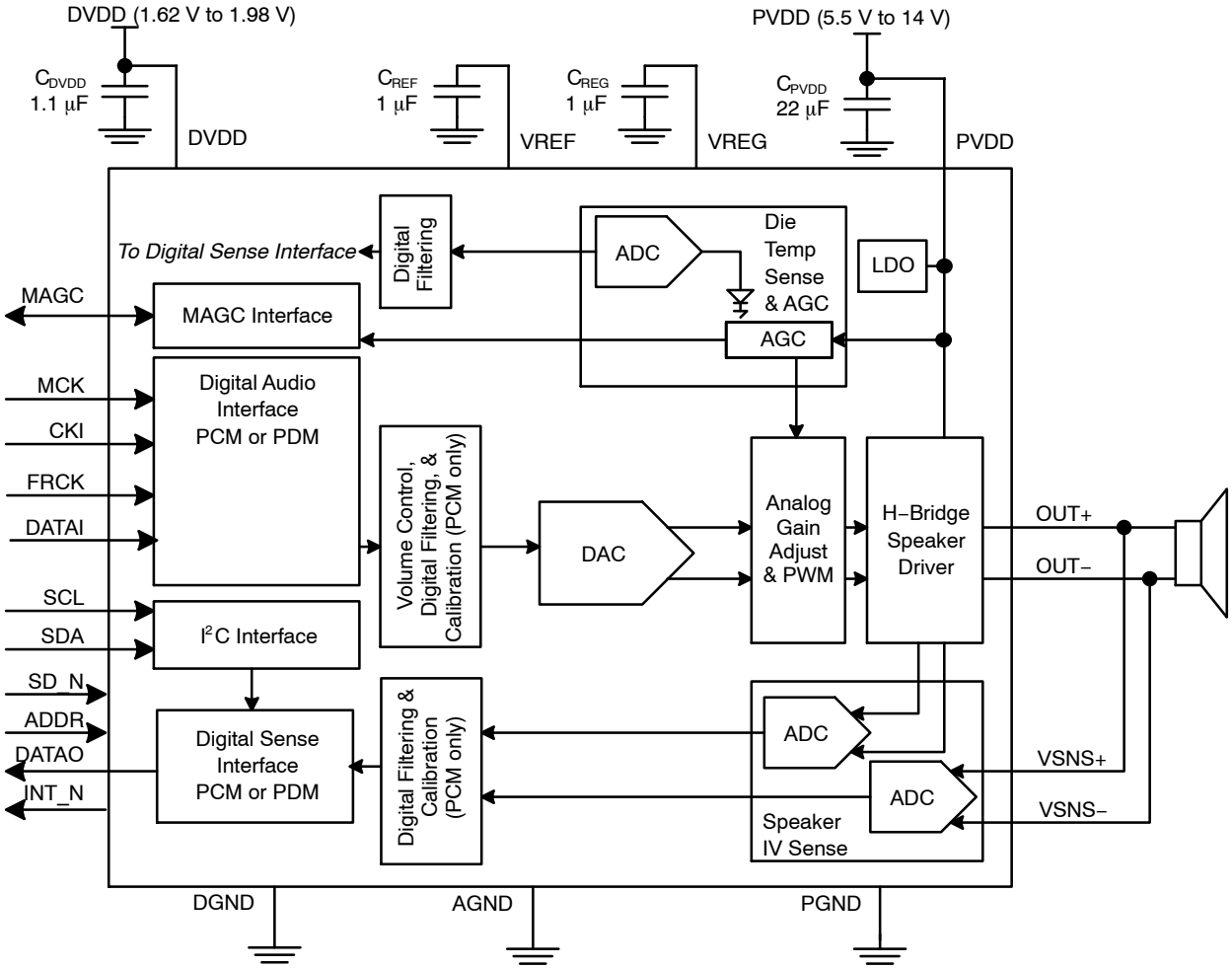


Figure 1. Functional Diagram

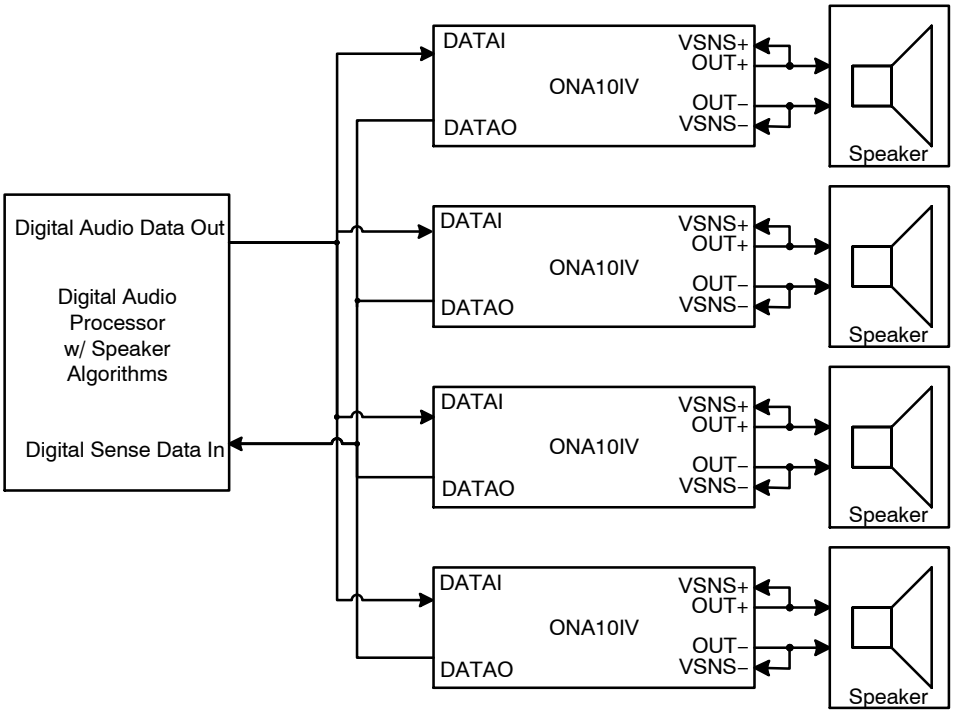


Figure 2. System Diagram

PIN CONFIGURATION

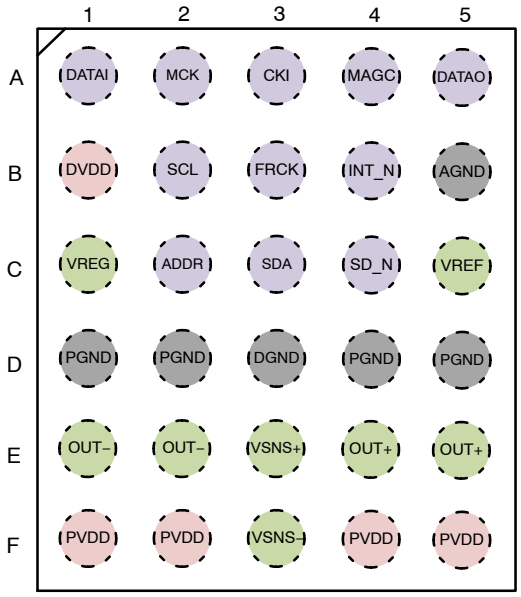


Figure 3. Top Through View (Balls Down)

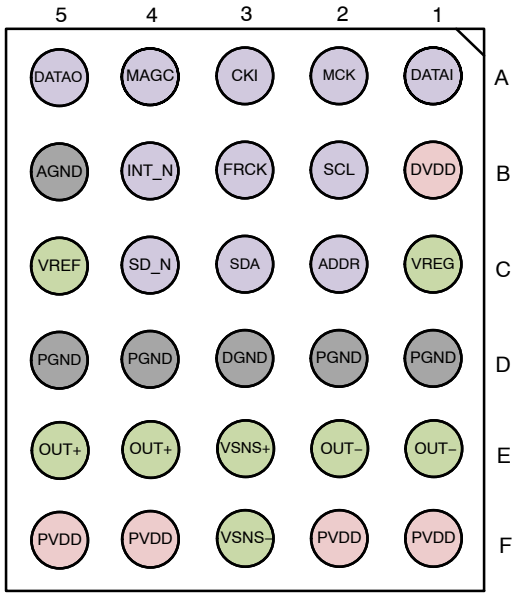


Figure 4. Bottom View (Balls Up)

PIN DESCRIPTION

Pin No.	Name	Type	Description
A1	DATAI	Data Input	DAI – Serial Digital Audio Data (either I^2S or PDM)
A2	MCK	Clock Input	DAI – Master Clock
A3	CKI	Clock Input	DAI – Bit Clock (PCM Mode) / PDM Clock (PDM Mode) Input
A4	MAGC	Control Bidirectional	Multi−speaker automatic gain control (MAGC) to synchronize multiple ONA10IV instantiations
A5	DATAO	Data Output	PDM or Serial PCM Speaker Sense Data Output
B1	DVDD	Power	Digital Power Supply
B2	SCL	Clock Input	I^2C – Clock Signal
B3	FRCK	Clock Input	DAI – Frame Clock (PCM Mode)
B4	INT_N	Control Output	Interrupt Request Signal
B5	AGND	Ground	Analog Ground
C1	VREG	Analog Output	Internal LDO Regulator Output
C2	ADDR	Control Input	Hardware selection of I^2C address to allow multiple ONA10IV instantiations.
C3	SDA	Data Bidirectional	I^2C – Data Signal
C4	SD_N	Control Input	Shutdown (Active Low)
C5	VREF	Analog Output	Internally Generated Reference
D1, D2, D4, D5	PGND	Ground	High Power Ground
D3	DGND	Ground	Digital Ground
E1,E2	OUT−	Analog Output	Inverting Class D Amplifier Output
E3	VSNS+	Analog Input	Positive Analog Input for Voltage Sense
E4, E5	OUT+	Analog Output	Non−inverting Class D Amplifier Output
F1,F2,F4,F5	PVDD	Power	Output Driver Power Supply
F3	VSNS−	Analog Input	Negative Analog Input for Voltage Sense

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
PV_{DD}	Voltage on PVDD Pin		−0.3	17.0	V
DV_{DD}	Voltage on DVDD Pin		−0.3	2.2	V
V_{OUT}	Voltage on OUT− and OUT+ Pins (Output Disabled)		−0.3	PV_{DD} + 0.3	V
	Voltage on INT_N, DATAO, and MAGC Pins (Output Disabled)		−0.3	6.0	
V_{IN}	Voltage on VSNS− and VSNS+ Pins		−0.3	PV_{DD} + 0.3	
V_{CNTRL}	Control Input Voltage	SCL, SDA, ADDR, CKI, DATAI, MCK, FRCK, MAGC, SD_N	−0.3	6.0	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RATINGS

Symbol	Parameter		Min	Typ	Max	Unit
T_J	Junction Temperature		–	–	150	°C
T_{STG}	Storage Temperature Range		−65	–	150	°C
T_L	Lead Temperature (Soldering, 10 s)		–	–	300	°C
θ_{JA}	Thermal Resistance, JEDEC Standard, Still Air	4−layer Board	–	55 (Note 1)	–	°C/W
		4−layer Board w/ vias	–	33 (Note 2)	–	
P_D	Maximum continuous on−chip power dissipation (T_A = 25°C) for multi−layer board		–	3.0	–	W

1. More layers can provide a lower θ_{JA}.
2. JEDEC standard board utilizes a via for each ball.

ESD PROTECTION

Symbol	Parameter	Condition	Min	Unit
ESD	Human Body Model (HBM)	ANSI/ESDA/ JEDEC JS−001−2012	2	kV
	Charged Device Model (CDM)	According to “EIA/JESD22−C101 Level III”	500	V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min (Note 3)	Typ	Max	Unit
T_A	Operating Temperature Range	−40	–	85	°C
DV_{DD}	Digital Supply Voltage Range	1.62	–	1.98	V
PV_{DD}	Power Supply Voltage Range (2S− Battery Configuration)	5.5	–	9.0	V
	Power Supply Voltage Range (3S− Battery Configuration)	7.5	–	14.0	V
C_{REF}	Reference Capacitor	0.85	–	–	μF
C_{REG}	Regulator Capacitor	0.85	–	–	μF
C_{PVDD}	PV_{DD} Capacitor (s)	20	–	–	μF
C_{DVDD}	DV_{DD} Capacitor (s)	0.85	–	–	μF
R_{PD_DATAO}	Pull down resistor; Only 1 required per DATAO bus	–	–	10	kΩ
Z_L	Load Inductance	–	10	–	μH
	Load Resistance	4	–	–	Ω

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Minimum passive component values include temperature, tolerance, and aging.

ELECTRICAL CHARACTERISTICS (PV_{DD} = 12 V, DVDD = 1.8 V, f_S = FRCK = 48 kHz, 24−bit digital audio data, Z_L = ∞, T_A = 25°C, SD_N = H, Default I^2C registers, and audio measurement bandwidth = 20 Hz to 20 kHz (AES17) unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPEAKER DRIVER PATH							
P_O	Maximum Continuous Output Power	THD+N ≤ 10%, f = 1 kHz	Z_L = 4 Ω + 10 μH PV_{DD} = 12 V	−	16.0	−	W
		THD+N ≤ 1%, f = 1 kHz	Z_L = 4 Ω + 10 μH PV_{DD} = 12 V	−	13.8	−	
			Z_L = 8 Ω + 10 μH PV_{DD} = 14 V	−	10.9	−	
			Z_L = 8 Ω + 10 μH PV_{DD} = 12 V	−	8.1	−	
			Z_L = 8 Ω + 10 μH PV_{DD} = 10.8 V	−	6.5	−	
			Z_L = 8 Ω + 10 μH PV_{DD} = 7.2 V	−	2.9	−	
R_{ON}	On Resistance of Output Stage	I_O = 500 mA High Side + Low Side Resistance		−	435	−	mΩ
η	Efficiency	f = 1 kHz, PV_{DD} = 14 V	P_{OUT} = 14 W, Z_L = 4 Ω + 10 μH	−	84	−	%
			P_{OUT} = = 10 W, Z_L = 8 Ω + 10 μH	−	90	−	
PSRR	PV_{DD} Power Supply Rejection Ratio	PV_{DD} = 5.5 V to 14V , Digitally Silent Input		−	74	−	dB
		f_{RIPPLE} = 217 Hz, Square Wave on PVDD 10 μs Rise/Fall Time PV_{DD} = 12 V w/ 200 mV Drop Digitally Silent Input		−	74	−	
		f_{RIPPLE} = 10 kHz, V_{RIPPLE} = 200 mV_{PP} Digitally Silent Input		−	74	−	
		f_{RIPPLE} = 20 kHz, V_{RIPPLE} = 200 mV_{PP} Digitally Silent Input		−	70	−	
K_{CP}	Click−And−Pop Level (Note 10)	Digitally Silent Input Peak Output Voltage A−weighted, T_A = 25°C Z_L = 4 Ω + 10 μH	Into Shutdown	−	±0.5	−	mV
			Out of Shutdown	−	±0.5	−	
V_{OS}	Differential Output Offset Voltage	T_A = 25°C, Digitally Silent Input Z_L =4 Ω + 10 μH		−	±0.5	±1.5	mV
e_N	Output Noise	Digitally Silent Input, 16 dB Gain Z_L = 4 Ω + 10 μH	A−weighted	−	42	−	$μV_{RMS}$
			Un−weighted	−	57	−	
DR	Dynamic Range	16 dB Gain, −60 dBFS Input Z_L = 4 Ω + 10 μH, A−weighted Relative to 1% THD+N Driver Path Output Power		−	105	−	dB
THD+N	Total Harmonic Distortion Plus Noise	f = 1 kHz	P_{OUT} = 4 W, Z_L = 8 Ω + 10 μH	−	0.012	−	%
			P_{OUT} = 8 W, Z_L = 4 Ω + 10 μH	−	0.015	−	
		f = Up to 8 kHz	P_{OUT} = 4 W, Z_L = 8 Ω + 10 μH	−	0.080	−	
			P_{OUT} = 8 W, Z_L = 4 Ω + 10 μH	−	0.090	−	

ELECTRICAL CHARACTERISTICS (PV_{DD} = 12 V, DVDD = 1.8 V, f_S = FRCK = 48 kHz, 24−bit digital audio data, Z_L = ∞, T_A = 25°C, SD_N = H, Default I^2C registers, and audio measurement bandwidth = 20 Hz to 20 kHz (AES17) unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPEAKER DRIVER PATH						
A_V	Amplifier Gain	Selected through AGC response or I^2C programming. Z_L = 8 Ω + 10 μH or Z_L = 4 Ω + 10 μH	15.4	16.0	16.6	dB
			11.4	12.0	12.6	
			8.3	9.0	9.6	
			5.2	6.0	6.7	
			2.1	3.0	3.9	
DAC_{MAP}	Typical DAC Mapping	0 dBFS PCM Input	–	4.22	–	dBV
		0 dBFS PDM Input 85.35% Ones Density Maximum	−9.68	−0.13	7.23	
DAC Digital Filter Characteristics (f_s = 16, 22.05, 44.1, or 48kHz) (Note 5)						
f_{PB}	Passband	−0.1 dB Cutoff	–	0.43* f_s	–	Hz
		−3 dB Cutoff	–	0.504* f_s	–	Hz
		−6 dB Cutoff	–	0.524* f_s	–	Hz
δ_P	Passband Ripple		–	0.052	–	dB
f_{SB}	Stopband		–	0.62* f_s	–	Hz
α_S	Stopband Attenuation	$f > f_{SB}$	–	58	–	dB
t_g	Group Delay		–	8.25	–	S
DAC Digital Filter Characteristics (f_s = 32 or 96 kHz) (Note 5)						
f_{PB}	Passband	−0.1 dB Cutoff	–	0.43* f_s	–	Hz
		−3 dB Cutoff	–	0.485* f_s	–	Hz
		−6 dB Cutoff	–	0.494* f_s	–	Hz
δ_P	Passband Ripple		–	0.054	–	dB
f_{SB}	Stopband		–	0.54* f_s	–	Hz
α_S	Stopband Attenuation	$f > f_{SB}$	–	58	–	dB
t_g	Group Delay		–	8.25	–	S
Driver References (Note 5)						
$f_{SW(AMP)}$	Class−D Switching Frequency	MCK = 12.2880 MHz	–	646.7	–	kHz
		MCK = 11.2986 MHz	–	519.2	–	
α_D	Digital Volume Control (Note 4)	Programmable in 0.375 dB steps from MUTE to 0 dB	−95.25	–	0	dB
SPEAKER SENSE PATH						
ΔG_{ERRVI}	Gain Error Variation, Voltage Over Current (Note 10)	T_A = 0°C to 60°C, −40 dBFS Input at 40 Hz	–	±0.50	–	%
Current Sense						
I_{IN}	Current Sense Range		–	–	3.50	A_P
BW_I	Converter Bandwidth	HPF Enabled	0.014	–	20	kHz
DR_I	Dynamic Range	−60 dBFS Input 16 dB Gain, A−weighted Relative to 1% THD+N Driver Path Output Power	–	71	–	dB
Voltage Sense						
V_{IN}	Voltage Sense Range		–	–	14	V_P
BW_V	Converter Bandwidth	HPF Enabled	0.014	–	20	kHz

ELECTRICAL CHARACTERISTICS (PV_{DD} = 12 V, DVDD = 1.8 V, f_S = FRCK = 48 kHz, 24−bit digital audio data, Z_L = ∞, T_A = 25°C, SD_N = H, Default I^2C registers, and audio measurement bandwidth = 20 Hz to 20 kHz (AES17) unless otherwise noted) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPEAKER SENSE PATH							
Voltage Sense							
DR_V	Dynamic Range	−60 dBFS Input 16 dB Gain, A−weighted Relative to 1% THD+N Driver Path Output Power		–	81	–	dB
POWER SUPPLY							
V_{REG}	Regulator Voltage	I_{REG} = 100 μA, Standby Bit Set		–	5.00	–	V
I_{PVDD}	Supply Current, PV_{DD}	Digital Silence	PV_{DD} = 14 V	–	13.8	–	mA
			PV_{DD} = 12 V	–	13.5	–	
			PV_{DD} = 10.8 V	–	13.2	–	mA
			PV_{DD} = 7.2 V	–	12.6	–	mA
I_{DVDD}	Supply Current, DV_{DD}	Digital Silence		–	1.5	2.0	mA
I_{SB_PVDD}	Standby Current, PV_{DD}	STBY bit set in I^2C register or CKI static (Note 6)	PV_{DD} = 12 V	–	2.9	–	mA
			PV_{DD} = 7.2 V	–	2.9	–	
I_{SB_DVDD}	Standby Current, DV_{DD}	STBY bit set in I^2C register or CKI static (Note 6)		–	0.3	–	mA
I_{DRV_PVDD}	Driver Path Only Supply Current, PV_{DD}	Digital Silence, IVSNS_PD bit active.		–	9.9	–	mA
I_{DRV_DVDD}	Driver Path Only Supply Current, DV_{DD}	Digital Silence, IVSNS_PD bit active.		–	1.0	–	mA
I_{SD}	Shutdown Current	SD_N = L	PV_{DD} = 12 V	–	2.0	–	μA
			DV_{DD} = 1.8 V	–	0.3	2.0	
ENVIRONMENT SENSE & PROTECTION CHARACTERISTICS							
Chip Protection Thresholds							
V_{LMT}	Under−Voltage Limit, PV_{DD}	Threshold		2.5	–	4.5	V
		Hysteresis		–	0.2	–	
	Under−Voltage Limit, DV_{DD}	Threshold		0.5	–	1.5	
		Hysteresis		–	0.5	–	
I_{LMT}	Output Current Limit	Shutdown Threshold		3.6	5.0	–	A
T_{LMT}	Thermal Limit	Shutdown Threshold		–	145	–	°C
		Recovery Threshold		–	115	–	
Automatic Gain Control (AGC) for Brownout Protection							
V_{ATH}	Attack Threshold Range	Programmable through I^2C	2S Battery Configuration (48 mV Steps)	6.511	–	7.999	V
			3S Battery Configuration (72 mV Steps)	9.763	–	11.995	
ACC_P	Absolute Accuracy	2S Battery Configuration		–	±70	–	mV
		3S Battery Configuration		–	±104	–	
t_A	Attack Time (Gain Decrease)	Programmable through I^2C in 35 μs steps		5	–	530	μs/dB
t_H	Hold Time	Programmable through I^2C in 35 ms steps		10	–	Infinite	ms
t_R	Release Time (Gain Increase)	Programmable through I^2C in 70 ms steps		5	–	1055	ms/dB

ELECTRICAL CHARACTERISTICS (PV_{DD} = 12 V, DVDD = 1.8 V, f_S = FRCK = 48 kHz, 24−bit digital audio data, Z_L = ∞, T_A = 25°C, SD_N = H, Default I^2C registers, and audio measurement bandwidth = 20 Hz to 20 kHz (AES17) unless otherwise noted) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ENVIRONMENT SENSE & PROTECTION CHARACTERISTICS							
Automatic Gain Control (AGC) for Brownout Protection							
t_L	AGC Attenuation Latency	Attack Time set to 5 μs. Measured from PVDD to initial response on OUT±		–	–	10	μs
Δ_{AGC}	Maximum AGC Attenuation	Gain setting is 16 dB or 12 dB (Note 7)		−2	–	−9	dB
Δ_{AGC}	AGC Attenuation Step Size			–	0.5	–	dB
t_{D2D}	MAGC Device−to−Device Latency			–	1	–	Sample
A_{D2D}	MAGC Device−to−Device Gain Delta			–	0.5	–	dB
Die Temperature Sense							
BW_T	Converter Bandwidth			–	500	–	Sps
T_{IN}	Temperature Sense Range			−40	–	150	°C
DIGITAL INTERFACE (Includes SCL, SDA, CKI, FRCK, MCK, SD_N, MAGC, ADDR, DATAI, DATAO, and INT_N)							
I/O Characteristics							
V_{IH}	Input High Voltage			0.7 x DV_{DD}	–	DV_{DD}	V
V_{IL}	Input Low Voltage			−0.5	–	0.3 x DV_{DD}	V
V_{HYST}	Input Hysteresis	SCL, SDA, and ADDR		–	0.20	–	V
		All other inputs (Note 8)		–	0.40	–	
I_{IH}	Input High Leakage	Input Voltage = V_{IH} to DV_{DD}		−1	–	1	μA
I_{IL}	Input Low Leakage	Input Voltage = V_{IL} to DGND		−1	–	1	μA
I_{OFF}	Off Leakage	DV_{DD} = 0 V	Any I/O from 0 V to 2.2 V	−10	–	10	μA
			SCL, SDA, and ADDR from 0 V to 5.5 V	−10	–	10	μA
I_{OZ}	Disable Leakage	DATAO & MAGC Pins, Across all DV_{DD} V_{IN} on pin from 0 V to 2.2 V.		−5	–	5	μA
C_{IN}	Input Capacitance				5	–	pF
V_{OH}	Output High Voltage	All Outputs; I_{OH} = 4 mA		1.2	–	–	V
		For MAGC/DATAO, 50% Drive; I_{OH} = 2 mA		1.2	–	–	
V_{OL}	Output Low Voltage	For MAGC/DATAO	I_{OL} = 4 mA	0	–	0.2 x DV_{DD}	V
			50% Drive; I_{OL} = 2 mA	0	–	0.2 x DV_{DD}	
		For SDA, SCL, & INT_N; I_{OL}= 3 mA		0	–	0.4	
I_{OL}	Output Low Current	For SDA, SCL, & INT_N; V_{OL} = 0.4 V		3	–	–	mA
Shutdown and Standby Timing							
t_{WU}	Wake−Up Time	SD_N = L → H to I^2C Communication		10	–	–	μs
		Shutdown condition removed (OUT+/− active) through I^2C. MCK is present		–	–	17.0	ms
		Standby condition removed (OUT+/− active) through I^2C.		–	–	11.0	ms

ELECTRICAL CHARACTERISTICS (PV_{DD} = 12 V, DVDD = 1.8 V, f_S = FRCK = 48 kHz, 24−bit digital audio data, Z_L = ∞, T_A = 25°C, SD_N = H, Default I^2C registers, and audio measurement bandwidth = 20 Hz to 20 kHz (AES17) unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INTERFACE (Includes SCL, SDA, CKI, FRCK, MCK, SD_N, MAGC, ADDR, DATAI, DATAO, and INT_N)						
Shutdown and Standby Timing						
t_{SD}	Shutdown/Standby Time	Time required after volume ramp down. MCK must be present during this period.	5.0	5.1	–	ms
Global Timing Requirements (Regardless of Mode or Interface)						
f_{FRCK}	FRCK Input Frequency Range		16	–	96	kHz
f_{MCK}	MCK Input Frequency Range	f_S = 16, 24, 32, 48, or 96 kHz	–	12.2880	–	MHz
		f_S = 44.1 kHz	–	11.2896	–	
$t_{jit, MCK}$	MCK Jitter	Allowable RMS jitter with minimal performance degradation.	–	–	0.1	ns
t_{SETUP}	FRCK or DATAI to CKI Setup Time		10	–	–	ns
t_{HOLD}	FRCK or DATAI to CKI Hold Time		0	–	–	ns
PCM Mode – I^2S						
f_{CKI}	CKI Frequency Range	CKI must be 32, 48, and 64x of FRCK.	0.512	–	6.144	MHz
PCM Mode – TDM (Used for DATAI & DATAO)						
	Number of Slots Supported		2	–	8	Slots
f_{CKI}	CKI Frequency Range		0.512	–	12.288	MHz
PDM Mode (Used for DATAI & DATAO)						
f_{CKI}	Clock Frequency		–	3.072	–	MHz
t_{PDM_SETUP}	DATAI to CKI Setup Time		10	–	–	ns
t_{PDM_HOLD}	DATAI to CKI Hold Time		0	–	–	ns
t_{PDM_VALID}	Time from CKI Transition to DATAO Remaining Valid	C_{LOAD} = 15 pF	–	17	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. This value is programmable through I^2C.
5. These specs are intended as reference and are guaranteed by design.
6. CKI is static based upon it not meeting the criteria as outlined in the Clock Requirements section.
7. Absolute minimum gain setting is 3 dB.
8. Does not include MCK
9. In the recommended implementation, VDDEXT is DVDD.
10. Validated by characterization.

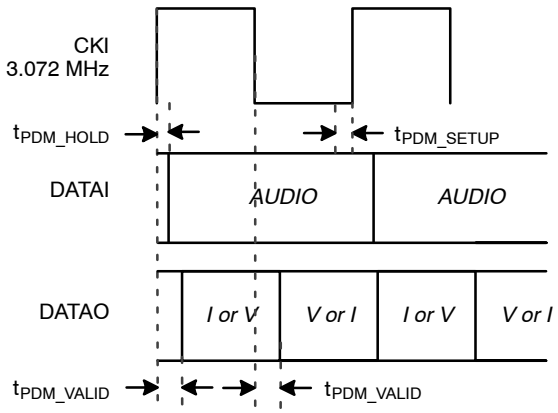
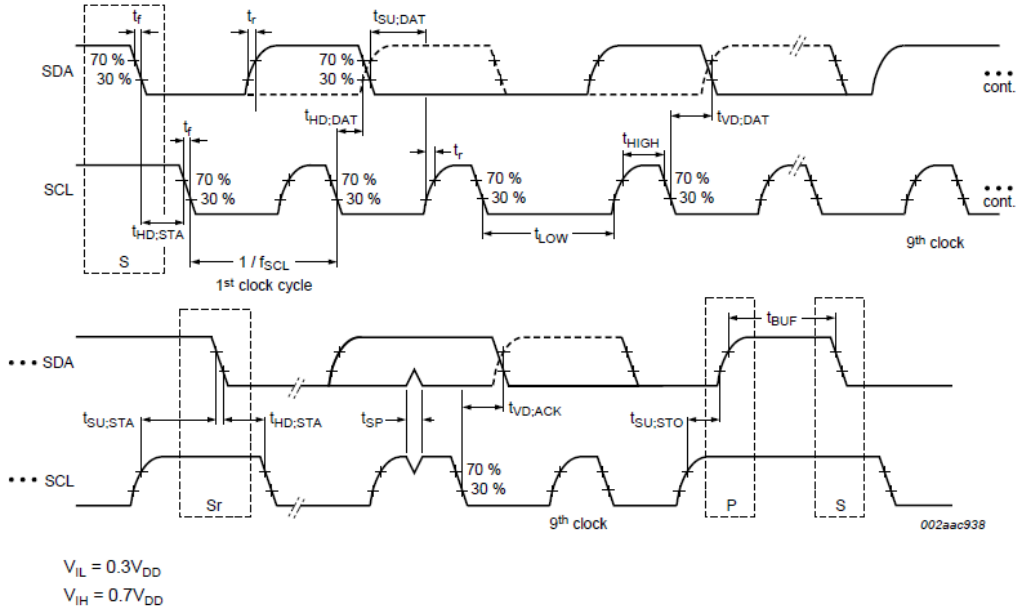


Figure 5. PDM Timing Parameters

FAST MODE I²C SPECIFICATION

Symbol	Parameter	Fast Mode		
		Min	Max	Unit
f_{SCL}	SCL Clock Frequency	0	1000	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.26	–	μs
t_{LOW}	Low Period of SCL Clock	0.5	–	μs
t_{HIGH}	High Period of SCL Clock	0.26	–	μs
$t_{SU;STA}$	Set−up Time for Repeated START Condition	0.26	–	μs
$t_{HD;DAT}$	Data Hold Time	0	–	μs
$t_{SU;DAT}$	Data Set−up Time	50	–	μs
t_r	Rise Time of SDA and SCL Signals	–	120	ns
t_f	Fall Time of SDA and SCL Signals	20* (V_{DDEXT} / 5.5 V) (Note 11)	120	ns
$t_{SU;STO}$	Set−up Time for STOP Condition	0.26	–	μs
t_{BUF}	Bus−Free Time between STOP and START Conditions	0.5	–	μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns
C_b	Capacitive Load for each Bus Line	–	550	pF
$t_{VD−DAT}$	Data Valid Time for Data from SCL LOW to SDA HIGH or LOW Output	0	0.45	μs
$t_{VD−ACK}$	Data Valid Time for acknowledge from SCL LOW to SDA HIGH or LOW Output	0	0.45	μs
V_{nL}	Noise Margin at the LOW Level	0.1* V_{DDEXT} (Note 11)	–	V
V_{nH}	Noise Margin at the HIGH Level	0.2* V_{DDEXT} (Note 11)	–	V

11. In the recommended implementation, VDDEXT is DVDD.
12. Validated by characterization.



$V_{IL} = 0.3V_{DD}$
$V_{IH} = 0.7V_{DD}$

Figure 6. Definition of Timing for Full−Speed Mode Devices on the I²C Bus

Table 1. I2C SLAVE ADDRESS

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	See Table 5 in I²C Slave Address Selection							R/W

TYPICAL PERFORMANCE CHARACTERISTICS

(Unless otherwise noted: Z_L = 8 Ω + 10 μH, f = 1 kHz, Audio measurement bandwidth 20 Hz to 20 KHz (AES17), PV_{DD} = 12 V, T_A = 25°C, Typical external component values)

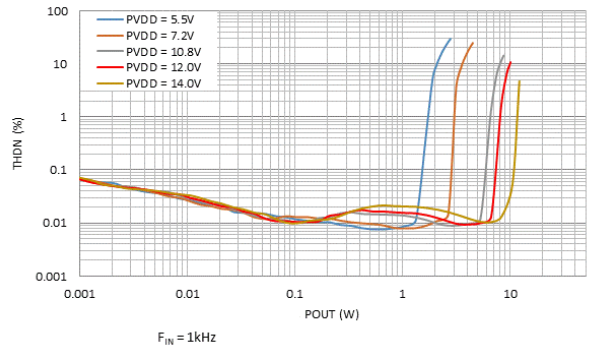


Figure 7. THD+N vs. Output Power

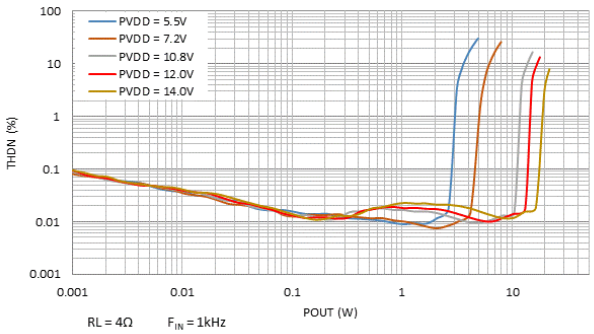


Figure 8. THD+N vs. Output Power

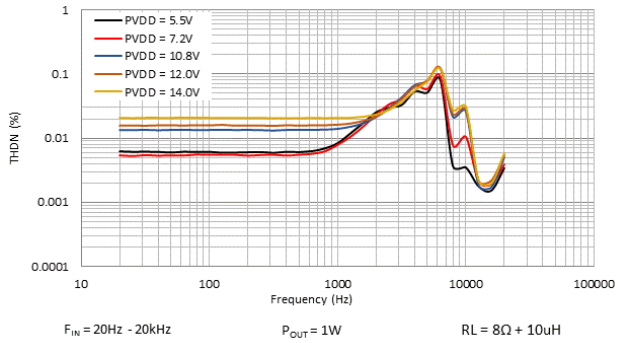


Figure 9. THD+N vs. Frequency

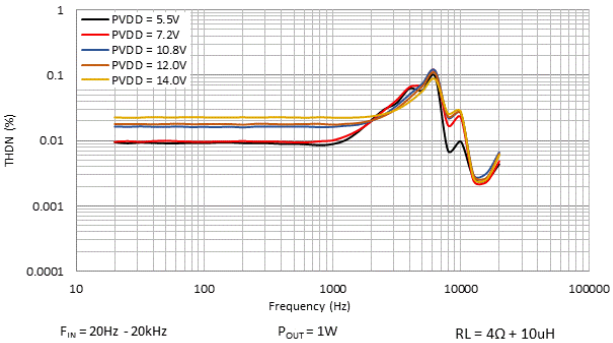


Figure 10. THD+N vs. Frequency

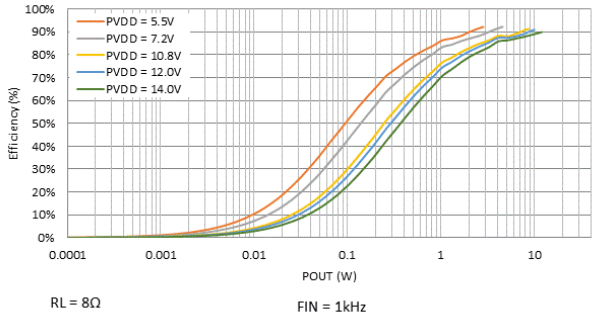


Figure 11. Efficiency vs. Output Power

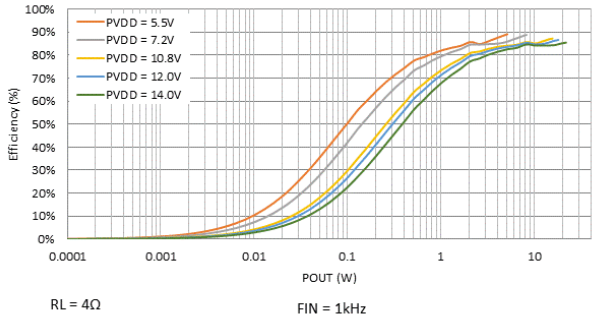


Figure 12. Efficiency vs Output Power

TYPICAL PERFORMANCE CHARACTERISTICS

(Unless otherwise noted: Z_L = 8 Ω + 10 μH, f = 1 kHz, Audio measurement bandwidth 20 Hz to 20 KHz (AES17), PV_{DD} = 12 V, T_A = 25°C, Typical external component values) (continued)

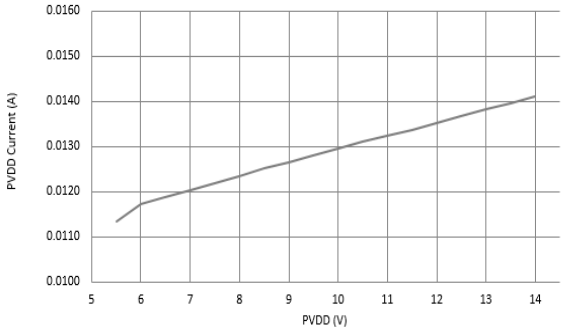


Figure 13. P_{VDD} Idle Current vs. P_{VDD}

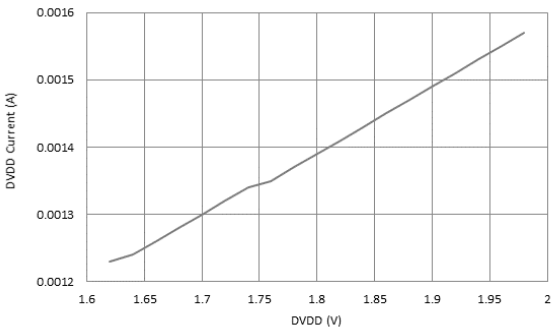


Figure 14. D_{VDD} Idle Current vs. D_{VDD}

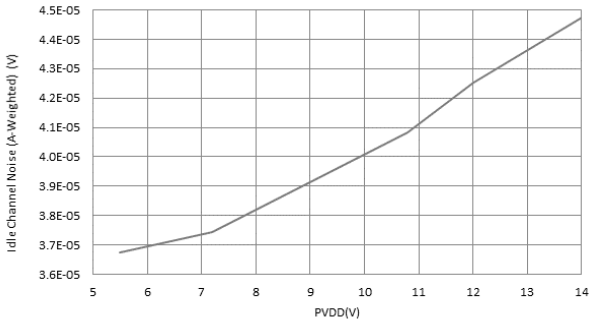


Figure 15. Idle Channel Noise (A−Weighed) vs. PVDD

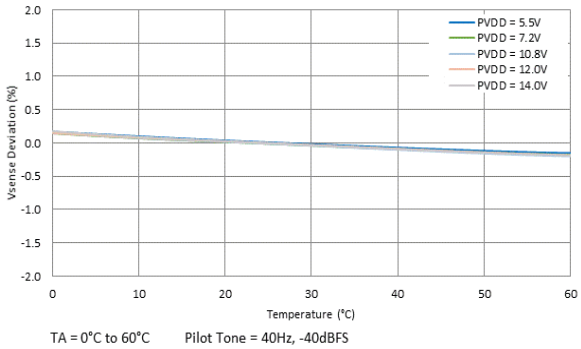


Figure 16. Vsense Gain Deviation vs. Temperature

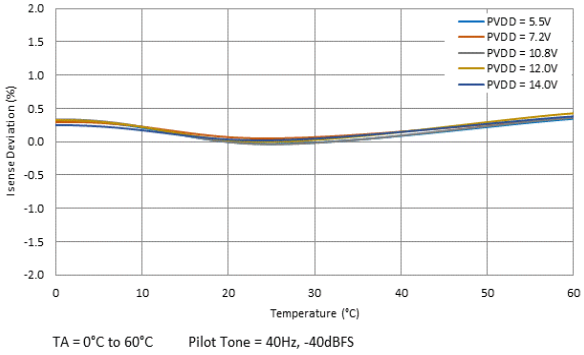


Figure 17. Isense Gain Deviation vs. Temperature

THEORY OF OPERATION

The ONA10IV is an audio endpoint, meaning that it includes the converters and amplifiers that translate the digital audio input into an analog audio output across the speaker and then senses that analog signal, amplifies, converts it to digital, and communicates what it senses to the host. This driver/sensor loop allows the host to optimize the audio speaker system.

While the theory of operation does not vary, there are multiple interface formats and device configurations that the ONA10IV can support. The remainder of this section describes the operating requirements and configurations. The list below summarizes the interface options available to the host:

Pulse Code Modulated (PCM)

- Formats: I^2S, Left−Justified, and TDM
- Sampling (f_{FRCK}): 16 kHz to 96 kHz
- Slot Width: 16−, 24, or 32 bits
- f_{CKI}: 512 kHz to 6.144 (I^2S)/12.288 MHz (TDM)
- f_{MCK}: 12.288 MHz or 11.2896 MHz (can be phase asynchronous to CKI/FRCK)
- TDM configuration can be adjusted so long as*:*
  - *f_{CKI} = # of slots * slot width * sampling frequency*
- The digital formats are all clocked using MCK, CKI and FRCK. The digital input clocking is also applicable to the following interfaces:
  - Digital Audio Input (DATAI Pin)
  - Digital Sense Output (DATAO Pin)
  - MAGC Bidirectional Bus (MAGC Pin)

Pulse Density Modulated (PDM)

- f_{CKI}: 3.072 MHz
- f_{MCK}: 12.288 MHz
- This modulation scheme is simpler and only clocked with CKI. The MAGC signal does not support PDM output and, if the MAGC feature is utilized, a FRCK is still required.

Power Supplies

The ONA10IV uses two power supplies, DV_{DD} (1.8 V regulated supply) and PV_{DD}, (can be a regulated supply between 5.5 V to 14 V or a stacked cell battery (2S, 5.5 V to 9 V or 3S, 7.5 V to 13.5 V)) and generates a third, V_{REG} (5 V internally regulated supply).

DV_{DD} [1.62 V to 1.98 V]

DV_{DD} is intended to match the I/O supply of the host such that no translators are required in the board design. It provides power to the digital interface and device controls. If DV_{DD} is 0 V, the chip cannot be communicated with, the I^2C registers are in reset, the PV_{DD} supply current is below I_{SD} (max.), and the I/O leakage current is less than I_{OFF_DVDD} (max.).

PV_{DD} [5.50 V to 14.00 V]

PV_{DD} provides a high voltage rail that supplies the H−Bridge of the amplifier to drive the speaker. It is also used to generate the V_{REG} supply.

If PV_{DD} is below V_{LIM} (shutdown) and not in shutdown, the chip enables only circuitry associated with detecting PV_{DD}. DV_{DD} supply current is I_{DVDD} (typ.), and the speaker interface pins (OUT+, OUT−, VSNS+, VSNS−) each have leakage less than I_{OFF_PVDD} (max.).

V_{REG} [~5.00 V]

V_{REG} is an internally generated supply that provides power to most of the analog circuitry. It is 0 V when the part is in shutdown (SD_N or SD_N bit low), PV_{DD} is below V_{LIM} (shutdown), or DV_{DD} is below V_{LIM} (shutdown).

POWER/ENABLE SEQUENCING

The following power sequence is required on power−up:

1. PV_{DD} is the first power supply applied to the device.
2. With SD_N low and PV_{DD} above V_{LIM} (recovery), DV_{DD} is applied with SCL and SDA always above V_{IH}.*
3. Wait until DV_{DD} is above V_{LIM} (recovery).
4. Remove chip from a hard shutdown by driving the SD_N pin high.
5. I^2C communication is available after 10 μs.
6. Remove chip from a soft shutdown by writing a 1 to the SD_N bit in register 0x01: PWR_CTRL.
7. With MCK applied any time prior to this point, wait t_{WU} before transmitting digital audio.

*In the above sequence, SD_N does not have to be an independent signal − it can be tied to DV_{DD}.

Power States

The ONA10IV has three power states when DV_{DD} is present: SHUTDOWN, STANDBY, and ACTIVE. These are described below.

SHUTDOWN Power State
("Hard": SD_N < V_{IL} or "Soft": SD_N bit is 0)

The SHUTDOWN power state provides the lowest possible supply current, I_{SD}. In shutdown, all non−I^2C digital I/Os and the speaker interface pins are all below their I_{OZ} (max) specifications. SHUTDOWN can be accessed through a "soft" shutdown (SD_N bit is 0) or a "hard" shutdown (SD_N < V_{IL}).

In "Hard" shutdown, the I^2C registers are reset and I^2C is not operational. The minimum time for SD_N to be low is indicated by "Soft" shutdown will not reset the registers and allow I^2C communication, but will have slightly higher leakage current on D_{VDD} (adds 5 − 10 μA at higher temperatures).

STANDBY Power State

A STANDBY power state can be entered through I²C (from the PWR_CTRL register), if CKI is not toggling, or after a timeout period from an AGC or error state. If STANDBY is entered into from a timeout period, the part can recover by entering RESET or exiting the automatic mode that triggered the timeout period (i.e. – disable AGC_TIMEOUT or ARCV setting). This mode is not as low−power as shutdown, but disables the DAC, mutes the amplifier, and disables all sense circuitry.

Table 2. POWER STATE CONDITIONS AND AVAILABLE OPERATIONS

Power State	Error State	Condition to Enter State	Available Operation
RESET	N/A	DVDD < V_{LIM}	None
		SD_N Input < V_{IL}	
		Writing 1 to RST bit	
SHUTDOWN	N/A	SD_N Input < V_{IL}	I2C Communication when SD_N Input > V_{IH}
		SD_N bit is 0	
	Under−Voltage (VERR)	PVDD < V_{LIM} (Note, I_{PVDD} > I_{SD})	
STANDBY	N/A	STBY bit is 1	I2C Communication Only
		Exceeding ARVC attempts or AGC_TIMEOUT Time	
ACTIVE	None	N/A	All
	AGC Active	PVDD < BATT_ATH Register Setting	Speaker Drive Gain Limited by AGC_MAX_ATT
	Thermal Foldback Active	$T_J \geq$ T_ATH Register Setting	Maximum Volume Limited
	Over−Temperature Error (TERR)	$T_J \geq T_{LIM}$	I2C Communication Only
	Over−Current Error (IERR)	$I_{OUT\pm} > I_{LIM}$	I2C Communication Only

The following sections describe operation in the *"ACTIVE Power State"…*

DIGITAL AUDIO INPUT

The digital audio input can be configured for a single−bit Pulse Density Modulation (PDM) stream or in a Pulse Code Modulation (PCM) format such as: I2S, Left Justified (LJ), or Time Divided Multiplexing (TDM). Examples of these digital audio formats are shown in the diagrams in Figure 18 (I2S) and Figure 19 (TDM).

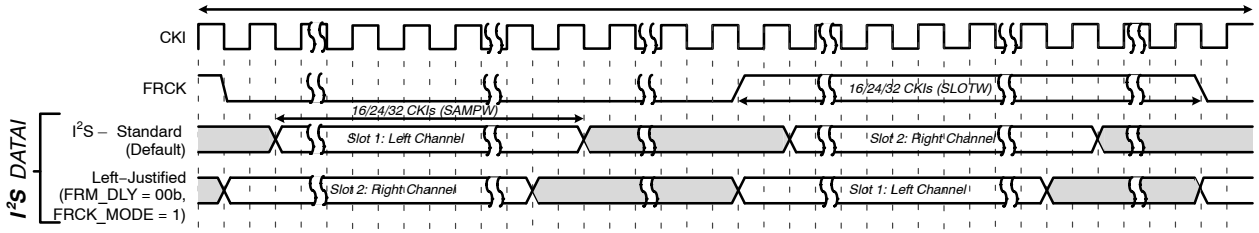


Figure 18. I²S Digital Audio Input (I²S and LJ Formats Shown)

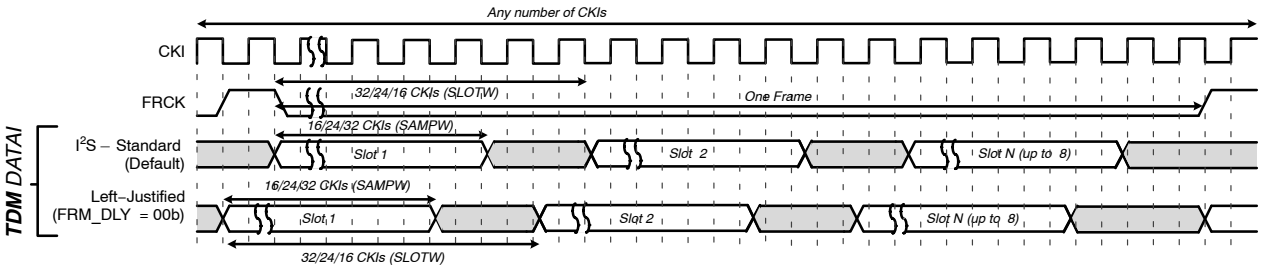


Figure 19. TDM Digital Audio Input (I²S and LJ Formats Shown)

PDM Digital Audio Operation

In PDM mode, audio data on the DATAI pin is clocked in by CKI. Pulse Density Modulation (PDM) is a common output of ADCs and, in essence, is the audio signal oversampled by f_{CKI}. An example of this format is shown below:

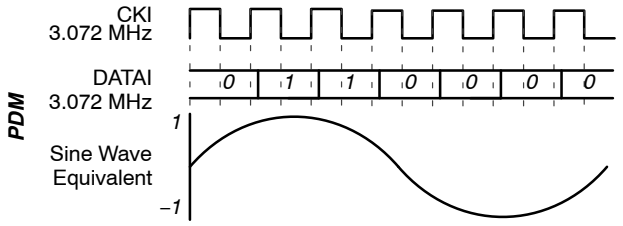


Figure 20. PDM Digital Audio Input

The PDM data that is received on DATAI is mapped into the DAC. This mapping is configurable via I2C in the register under PDM_DAC_MAP. Additionally, a separate amplifier gain for PDM mode can be set in the same register under PDM_AMP_GAIN. When switching into PDM mode this value will be used rather than the PCM_AMP_GAIN setting. A time of t_{SW_MOD}, is required to switch between the PCM and PDM interfaces. It is expected that the host will manage any sequencing required between digital audio formats to avoid undesirable audible effects.

PCM Digital Audio Operation

Audio data on the DATAI pin is clocked in by CKI with the most significant bit appearing first. Audio samples are two's complement Pulse Code Modulation (PCM) and are 16 bits, 24 bits, or 32 bits in width as defined by the SAMPW register bits. SLOTW defines the number of CKI periods between each sample. For example, sample width may be 24 bits (SAMPW = 01b), while slot width may be 32 bits (SLOTW = 10b). After every 24 bit sample, there are an additional 8 bits (that are ignored by the DAC) before the next sample begins. Sample length must be equal to or less than slot width.

Sample rate, f_S, is equal to the FRCK frequency. In addition, one data "frame" is equal to one FRCK period.

PCM audio data is internally buffered and fed to the DAC at the end of the audio frame. This is done to keep separate amplifiers in phase with each other in multi−slot systems. The slot that the ONA10IV responds to can be selected using the A_SLOT setting in the register.

I2S Digital Audio Interface

For I^2S or left justified data (DAI = 00b), each frame contains 2 separate slots of audio – left channel and right channel. In each frame, the left channel is always transmitted first, and the right channel is always second. FRCK's duty cycle is always 50%.

Figure 18 shows the I^2S digital audio interface with two different formats on DATAI: I^2S (traditional) and left−justified. For "left justified", FRCK is high during left channel audio data and low during right slot audio data (FRCK_MODE = 1). Audio samples are left justified so that the first data bit appears at the first CKI period after a FRCK edge (FRM_DLY = 00b). Data is valid on the rising edges of CKI (BEDGE_DAI = 1). If the audio sample width is 24 bits (SAMPW = 01b), but the data slot width is 32 bits (SLOTW = 10b) the 8 bits after the audio sample are ignored and one FRCK period is 64 CKI periods. The chip will respond to left or right channel audio data based on the A_SLOT setting in the register.

For "I^2S" formatted I^2S digital audio, it is similar to left justified except that the frame is delayed by one CKI (FRM_DLY = 01) and FRCK is low for left slot audio data and high for right slot audio data (FRM_POL = 0). Note that the frame still begins with left channel audio data. If the frame were to begin with right channel audio data, left and right audio would be out of phase with each other by $^1/_2$ fS. In this example, audio sample width is 16 bits wide (SAMPW = 00b) but the slot width is still 32 bits (SLOTW = 10b) and FRCK period is still 64 CKI periods. Only right channel audio data is used (A_SLOT = 0000b).

TDM Digital Audio Interface

One TDM "frame" can contain 2, 4, or 8 separate slots of audio. In each frame, slot 1 is transmitted first; slot 2 is transmitted second, and so on. FRCK signals the beginning of a frame with a single pulse that is 1 CKI period wide. This can also be changed in I^2C through the FRCK_MODE settings.

PCM audio data is internally buffered and fed to the DAC at the end of the audio frame. This is done to keep separate amplifiers in phase with each other in multi−slot systems. The data slot that the ONA10IV receives can be selected using the A_SLOT register.

Clock Requirements

The ONA10IV requires a master clock that is 12.288 MHz or 11.2896 MHz (depending on if the sample rate is 44.1 kHz).

The bit (CKI) and frame (FRCK) clock need to match what has been programmed in the FS register (0x06) such that the following equation is valid:

$$f_S = f_{FRCK} = \frac{f_{CKI}}{N_{Channels} \cdot Slot_{Width}} \quad \text{(eq. 1)}$$

In addition, FRCK frequency must always be within recommended operating conditions. If FRCK fails to meet these criteria, a clock error is detected (CERR) and the class−D amplifier will shutdown (see Interrupts & Fault Recovery section).

Volume Control

Volume can be ramped anytime the driving path is enabled or the volume setting changed. This minimizes pop if audio data is nonzero. If AVOLUP is set to 1 and the driving path is enabled, then the volume is ramped from mute up to MAX_VOL in VOL_RAMP. If the thermal fold back limit is reached before the volume reaches the MAX_VOL setting, the startup ramp releases control of MAX_VOL. If AVOLUP = 0, the volume is immediately set to MAX_VOL upon enable.

If AVOLDN is set to 1 and the driving path is disabled, the volume is ramped from its present value down to mute in VOL_RAMP. During the ramp, the detection of a thermal error is allowed to accelerate the downward ramp, but it is not allowed to increase the volume. If AVOLDN = 0, volume is immediately set to mute upon disable.

Further, if the maximum volume setting is changed, then the volume will also be ramped up or down as necessary.

Shutdown conditions caused by PVDD < VLIM or class−D amplifier over−current are immediate and unaffected by the VOL_RAMP setting.

Interrupts & Fault Recovery

The ONA10IV contains multiple fault flags that will drive the INT_N pin low when the status of the flag changes to alert the host and prevent a system failure. The flags are contained in the register and can be cleared by writing a “1” in the flagged bit. The following faults are detected and flagged:

- Under−Voltage Limit (VERR_I)
- Over Output current Limit (IERR_I)
- Over−Temperature Limit (TERR_I)
- Absent or Insufficient Clocks (CERR_I)

Additionally, there are interrupts to communicate that Automatic gain correction (AGC_I) or thermal foldback(TFB_I) is active.

Where the interrupt flag is sent to indicate a change in an error state, the error status register always shows the active status of the error.

If PV_{DD} falls below V_{LIM} (shutdown), the device goes into an under−voltage error state that is similar to shutdown. The device remains off until PV_{DD} rises above V_{LIM} (recovery). I^2C registers are reset to default values.

If the output current of the class−D amplifier exceeds I_{LIM} (shutdown), OUT+ and OUT− are high impedance and the IERR bit is set to 1. The I^2C port remains active and I^2C register values are preserved. If ARCV = 1, the class−D amplifier attempts to restart every 1 s until the fault condition is removed. If ARCV = 0, the class−D amplifier remains off until SD_N or MRCV are toggled to successfully restart the amplifier without an over−current event.

If the junction temperature meets or exceeds T_{LIM} (shutdown), OUT+ and OUT− are disabled, and the TERR bit is set to 1. The I^2C port remains active and I^2C register values are preserved. If ARCV = 1, the class−D amplifier will restart after the die temperature meets or falls below T_{LIM} (recovery). If the MAX_ARCV is limited, then every 1 s period is counted as a recovery attempt. If ARCV = 0, the class−D amplifier remains off and the TERR status bit is set to 1 until SD_N or MRCV are toggled to successfully restart the amplifier without an over−temperature event. See the “Thermal Foldback” section for more detail.

If a clock error is detected (see the Clock Requirements section), OUT+ and OUT− are high impedance, and the CERR bit is set to 1. The I^2C port remains active and I^2C register values are preserved. If ARCV = 1, the class−D amplifier will turn on when all clocks are valid. If ARCV = 0, the class−D amplifier will remain off until SD_N or MRCV are toggled to successfully restart the amplifier without a clock error event.

During a CERR, the DATAO and MAGC buses will maintain their last driving state.

Low EMI

The class−D amplifier’s low EMI design allows the OUT+ and OUT− pins to be connected directly to a speaker without an output filter.

Edge Rate Control minimizes EMI generated by the high−current switching waveform of the Class−D amplifier output. One of the main contributors to EMI generated by Class−D amplifiers is the high−frequency energy produced by rapid (large dV/dt) transitions at the edges of the switching waveform. ERC suppresses the high−frequency component of the switching waveform by extending the rise and fall times of the output FET transitions at all power levels. Rise and fall rates are set to a default of 3.5 V/ns and can be reprogrammed through I^2C.

Spread spectrum switching can also be adjusted through I^2C.

Thermal Foldback

Compared to thermal protection (Figure 22; described in Interrupts & Fault Recovery), the thermal foldback feature (Figure 21) is a pre−emptive attempt to avoid the over−temperature fault (TERR). The following describes the sequence that it conducts to limit the volume. All configurations are set in the 0x15: SENSE_CNTRL register.

1. Unless thermal foldback is disabled (TFB_PD = 1), at any time the die temperature reaches the attack threshold (set in register bits, T_ATH) the thermal foldback sequence initiates. The thermal foldback attacks at a rate of T_ATTACK to a target output attenuation of −12 dB from the current MAX_VOL setting and is applied to all signal amplitudes. The reduction in gain does not track with temperature, but reduces gain until the temperature has reached a recovery threshold that is 10°C below the attach threshold (T_ATH) or has reached the maximum attenuation.
2. While in foldback, any time the die temperature has gone below the recovery threshold then the chip waits a hold time (T_HOLD) until it begins ramping the volume (using the settings in volume control register, VOL_CTRL).
3. If the ONA10IV remains in foldback at maximum attenuation (−12 dB from MAX_VOL) without reaching the recovery threshold for an extended period of time, the TFB_PD bit can be set to 1 to remove the foldback and rely on thermal protection only.
4. When the die temperature is below the temperature attack threshold, the thermal foldback feature has no effect on the signal path.

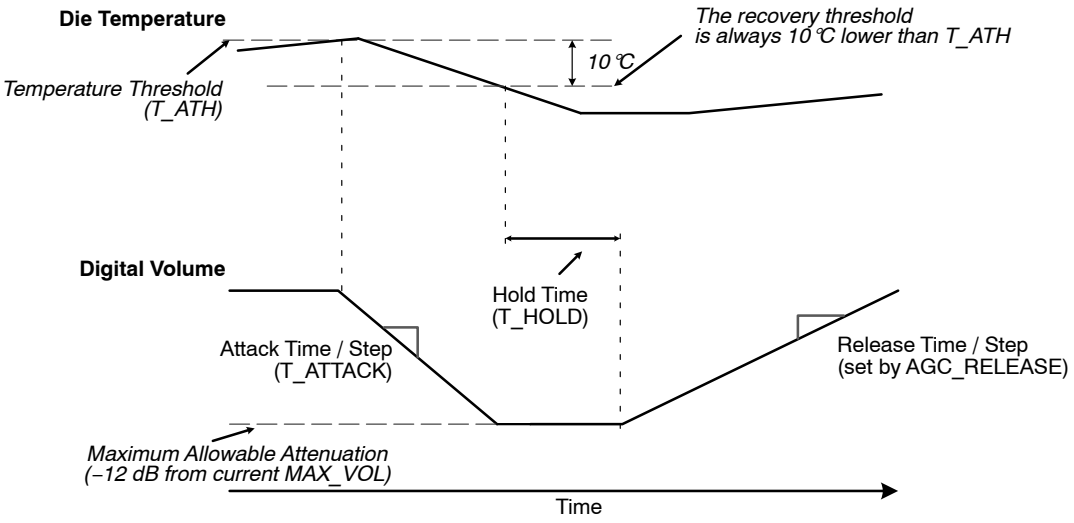


Figure 21. Thermal Foldback: Die Temperature Changes vs. Time

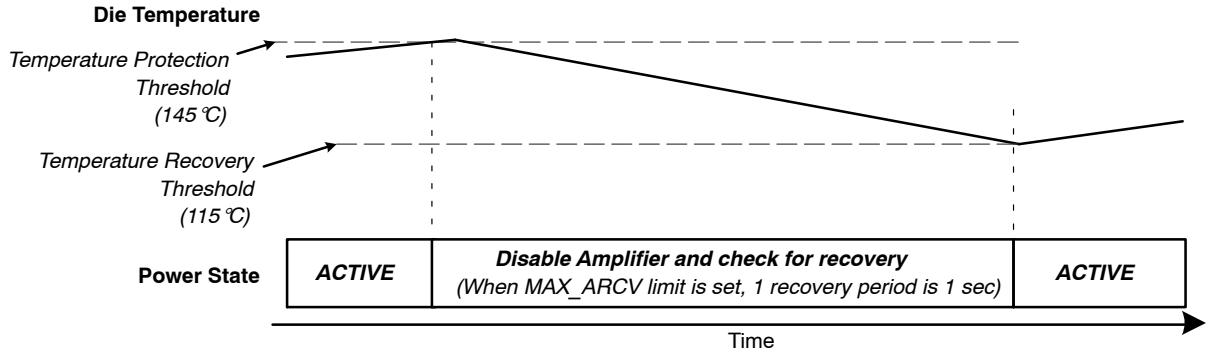


Figure 22. Thermal Protection: Die Temperature Changes vs. Time

Automatic Gain Control (AGC) for Brownout Protection

The AGC eases low−PV_{DD} current demands by reducing the maximum volume when PV_{DD} voltage drops below an "attack" threshold. The AGC attack threshold can be set by the AGC_CTRL register. The following is an example AGC sequence that would automatically control the system gain

1. At any time the battery (PV_{DD}) crosses below the attack threshold (BATT_ATH), the AGC sequence initiates. The AGC attacks (AGC_ATTACK) to the target output attenuation (AGC_MAX_ATT) that is applied to all signal amplitudes. The latency from PV_{DD} dropping below BATT_ATH to the output changing is 10 μs (maximum). The reduction in gain does not track the battery, but attacks until PV_{DD} has gone above the attack threshold (BATT_ATH).
   The timing values are set in and registers.
2. At any time the battery has gone above the attack threshold (BATT_ATH), the chip waits a hold time (AGC_HOLD) until it begins its release timing (AGC_RELEASE) from the automatic gain control.
3. If the ONA10IV remains at AGC_MAX_ATT for a programmable timeout period, AGC_TIMEOUT, then the device will go into standby. The AGC error status will be maintained. To exit, the part can be reset (through a hard or soft shutdown) or the AGC_TIMEOUT can be disabled to begin searching for a recovery of PVDD.
4. When PV_{DD} is above the AGC attack threshold, the AGC has no effect on the signal path.

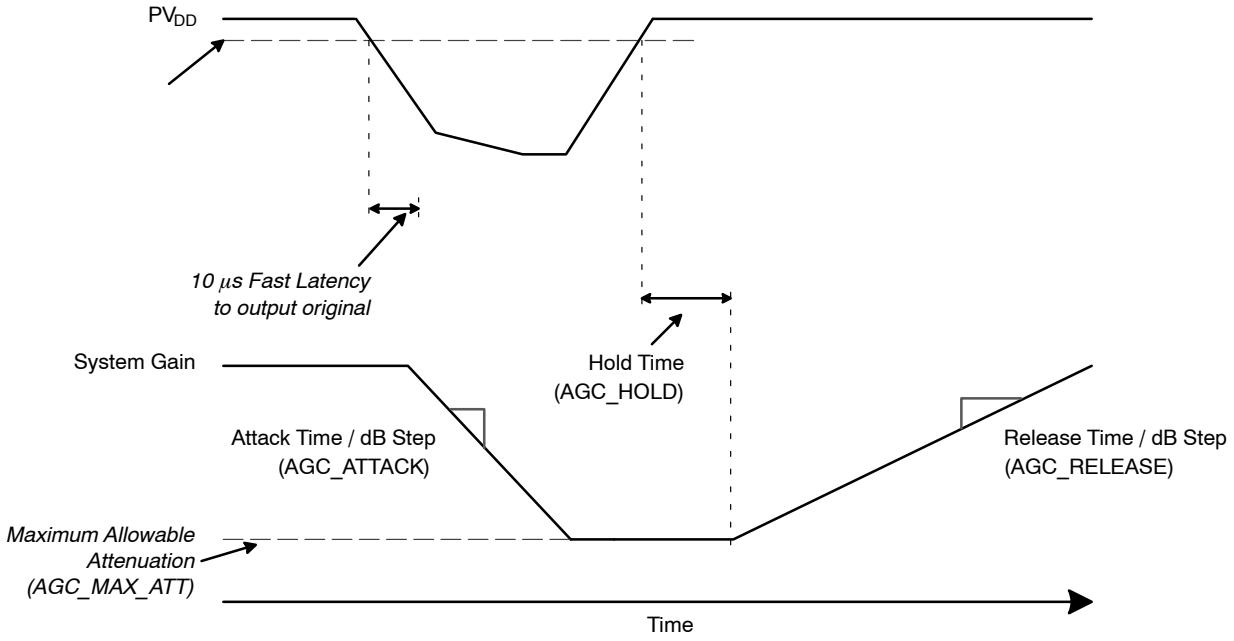


Figure 23. AGC Changes vs. Time

Multi−amplifier Automatic Gain Control (MAGC) Bus

In order to maintain a balanced multi−speaker / multi−amplifier system, it is necessary to have a means of synchronizing and matching the gain of each instantiation of ONA10IV (up to 8) quickly (within t_{D2D}; typically one sample), accurately (within $A_{D2D;}$ typically 0.5 dB), and despite its current environment.

To do this, each ONA10IV is programmed through I^2C to transmit on a particular slot (up to 8) on the MAGC bus. Additionally, it can be programmed to listen to as many of the other slots as desired. When the chip detects an AGC event, it transmits the current gain setting within its slot onto the MAGC bus and then releases the bus into high impedance immediately after transmission (as shown in Figure 24). All other ONA10IVs synchronize their amplifier gain to the lowest setting on the MAGC bus (whether transmitted (measured on−chip) or received). The MAGC setting does not affect the active operation of AGC, only the amplifier gain setting.

If any ONA10IV on the host exceeds the AGC_TIMEOUT period and goes into STANDBY, it sends a 0x1F code to other instantiations to go into STANDBY. Entering STANDBY through a MAGC command will not set an interrupt flag. Only the instance of ONA10IV that flagged the AGC, we have set an interrupt flag.

If MAGC is enabled (via MAGC_EN register bit) and AGC is disabled (AGC_PD), the ONA10IV will still react to what it receives on the MAGC bus.

If a more rapid response is required, then the gain data can be sent out on multiple slots for systems with 4 or less instantiations of the ONA10IV.

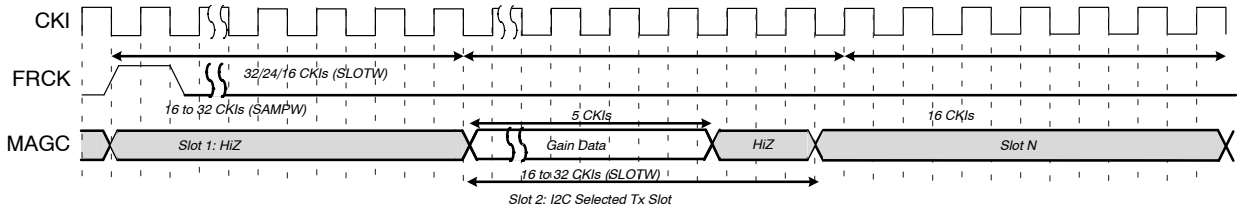


Figure 24. MAGC Gain Transmission

Speaker Sense

The ONA10IV includes two analog−to−digital converters that aid in allowing the host to drive the speakers at the maximum possible volume. Speaker impedances vary considerable over frequency and knowing what the speaker voltage and current allows the host to optimize the audio system without damaging the speaker. Based on the I2C settings in the register, the output can be sent out in a PDM format or in a PCM format within a selected slot determined by register.

For PCM, the results of these ADCs are sent out in 2 μs complement out of the DATAO output. Example timing diagram of the PCM format is shown in the Digital Sense Interface section. A summary of the code is found below:

Table 3. SPEAKER SENSE

	MSB	Speaker Sense Encoding														LSB	Unit
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Voltage Sense	$-(2^4)$	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	Volts
Current Sense	$-(2^2)$	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	Amps

Die Temperature Sense

While speaker protection is provided by the current and voltage sense paths, the environmental conditions of the chip (and system) are measured by another ADC used for monitoring the die temperature. These values can be read through I^2C or streaming concurrently (through TDM) on DATAO in PCM mode. A summary of the code is found below:

Table 4. TEMPERATURE SENSE

	MSB	Speaker Sense Encoding									LSB	Unit
	10	9	8	7	6	5	4	3	2	1	0	
Temperature Sense	$-(2^8)$	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	°C

Digital Sense Interface (DATAO)

The DATAO output is used communicate the output of the sense ADCs to the host. It can be configured for either PDM Mode (as shown in Figure 25) or as a TDM interface (as shown in Figure 26) in the register. In TDM mode, the data is sent out from MSB to LSB. In PDM mode, data can be sent on both edges of the clock if both current and voltage sense paths are enabled. Or, if one path is enabled, both edges will transmit the enabled sense path data. Temperature cannot be sent out through DATAO in PDM mode

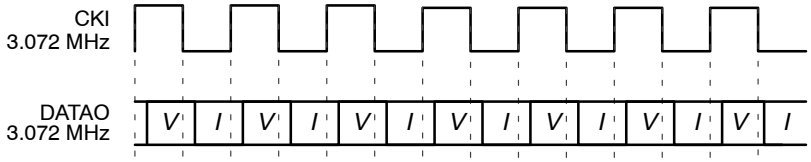


Figure 25. Digital Sense Interface with PDM

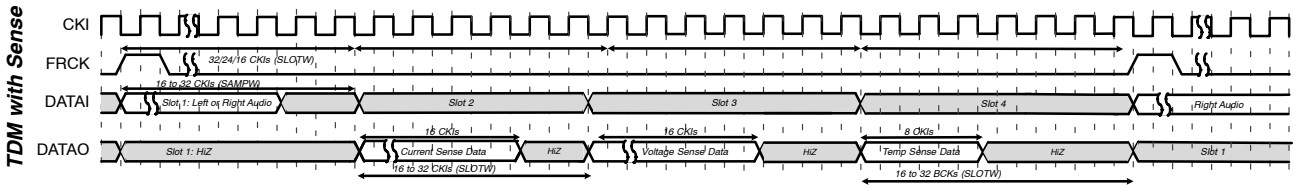


Figure 26. Digital Sense Interface with TDM

I²C Interface

The ONA10IV includes a full I2C slave controller. The I2C slave fully complies with the I2C specification version 6 requirements. This block is designed for Fast Mode traffic with up to 1 MHz SCL operation.

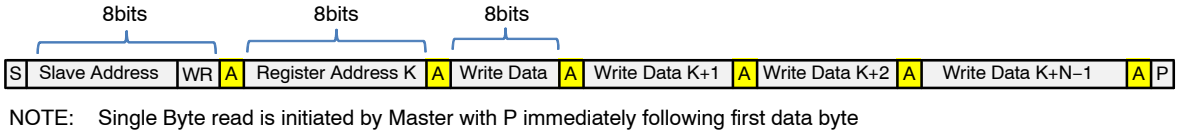


Figure 27. I²C Write Example

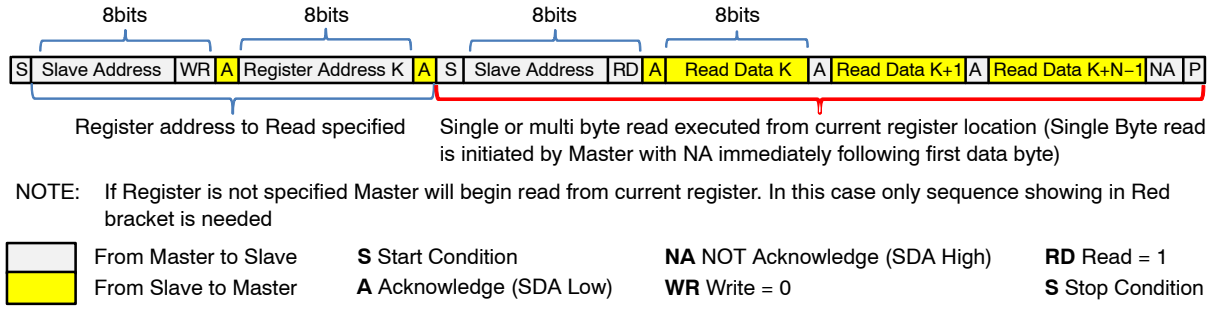


Figure 28. I²C Read Example

I²C Slave Address Selection

The ONA10IV includes a fast−mode (up to 1 MHz) I²C slave controller with 4 slave addresses selectable through shorting the DGND, SCL, SDA, or DV_{DD} pins to the ADDR pin. An additional 4 slave addresses can be attained from swapping the SCL and SDA signals to the SCL and SDA pins. All possible slave address configurations are shown in Table 5. The slave address is determined using the start condition of the first I²C transaction after a power up. It is required that I²C traffic to the chip during power−up be held high or at DV_{DD} to insure that the desired slave address is selected.

Table 5. I2C SLAVE ADDRESS SELECTION (ONA10IV)

			I²C Slave Address (Binary)								I²C Slave Address (Hex)	
DR Pin	SCL Pin	SDA Pin	B6	B5	B4	B3	B2	B1	B0	R/W	Write	Read
DGND	SCL Signal	SDA Signal	0	1	0	0	0	1	1	R/W	46	47
SCL Pin	SCL Signal	SDA Signal	0	1	0	0	1	0	0	R/W	48	49
SDA Pin	SCL Signal	SDA Signal	0	1	0	0	1	0	1	R/W	4A	4B
DV_{DD}	SCL Signal	SDA Signal	0	1	0	0	1	1	0	R/W	4C	4D
DGND	SDA Signal	SCL Signal	1	0	0	1	0	0	0	R/W	90	91
SCL Pin	SDA Signal	SCL Signal	1	0	0	1	0	0	1	R/W	92	93
SDA Pin	SDA Signal	SCL Signal	1	0	0	1	0	1	0	R/W	94	95
DV_{DD}	SDA Signal	SCL Signal	1	0	0	1	0	1	1	R/W	96	97

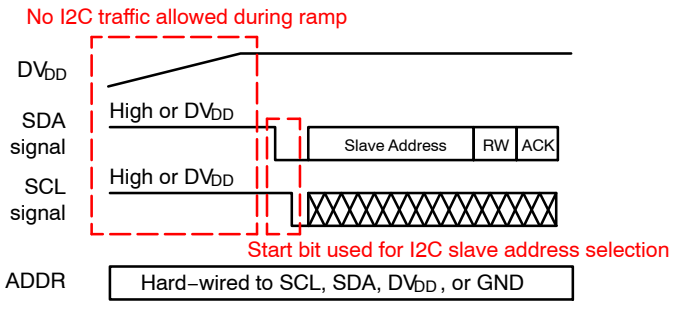


Figure 29. I²C Slave Address Selection on Power−up (ONA10IV)

PCB LAYOUT GUIDELINES & RECOMMENDATIONS

When designing audio applications using the ON Semiconductor ONA10IV 16 W Class−D amplifier with digital inputs, there are PCB layout and design guidelines that should be implemented for optimum performance and reliability in the end application. This section will address the following key topics:

- PCB stackup recommendations
- Grounding layout & considerations
- Key components – bill of materials
- Decoupling capacitor size and placement
- DVDD & digital signal layout
- PVDD & Class−D signal layout
- Thermal management
- Design for EMI considerations

PCB Stackup Recommendations

The ONA10IV is a versatile device that can be incorporated into designs of various sizes, form−factors and layouts. The following stackup recommendations are based on the ONA10IV evaluation kit PCB. This proven design can act as a basis for modifications to meet your specific application requirements:

Table 6.

PCB Thickness	0.063”
PCB Material	High TG FR4
Layer Count	6
Layer Stackup	Top – Signal & output traces, decoupling
	Layer 2 – GND
	Layer 3 – Power (PVDD, DVDD)
	Layer 4 Signal routing
	Layer 5 – GND
	Bottom – Signal & decoupling w/ GND fill
Cu Weight	1 oz.

Grounding Layout & Considerations

ONA10IV grounding layout is extremely important for proper operation and performance. The ground layout guidelines listed here must be followed to ensure good performance and proper device operation.

- Figure 30 and Figure 31 illustrate a suitable ONA10IV layout scheme for a multi−layer PCB design.
- As noted in these figures, decoupling capacitors for all supplies and reference voltages are placed as close as possible to the ONA10IV and on the same PCB layer where practical.
- Top−layer ground flooding and multiple vias to inner ground planes should be used to minimize parasitic inductance.
- Use a minimum of 1 oz Cu, or the equivalent, for ground planes.
- The ground reference for VREG and VREF is AGND. Route AGND back to the system ground separately from PGND routing. Failure to properly decouple VREG & VREF or to isolate AGND from noise may result in

Decoupling Capacitors

- 1 μF (min), low−ESR capacitors are recommended for DVDD, VREG & VREF. VREF and VREG capacitors should be placed close to the ONA10IV and connected to AGND through a low−impedance path.
- Due to the potential for large voltage and current transients during operation at high output power, multiple PVDD decoupling capacitors are recommended. These should include a bulk, low−ESR storage capacitor with stable capacitance at higher DC working voltages (tantalum or electrolytic, for example) of at least 22 μF, as well as additional smaller value capacitors as needed for high−frequency noise decoupling.
- Refer to Figure 30 and Figure 31 for examples.

NOTE: when selecting MLCC capacitors for PVDD decoupling, make sure the capacitance rating vs. DC offset voltage is suitable for your intended application. Generally, capacity of MLCC capacitors derates significantly as DC bias increases, especially for larger capacitance values in smaller package sizes.

DVDD & Digital Signal Layout

- Place a low−ESR 1 μF decoupling capacitor as close as possible to DVDD. Minimize trace inductance.
- Layout all digital audio interface signals using 50 Ω characteristic trace impedance where possible.
- Use pull−up resistors on SD_N & INT_N. These are open−drain I/Os and require an external pull−up to DVDD. Noisy environments may require a lower value pull−up resistor.
- Nominal I^2C pull−up resistor values will be dependent upon several factors, including the I^2C frequency, output drive current of the I2C master and the capacitive load of the I^2C bus. The
- Refer to Figure 30 and Figure 31 for examples.

PVDD & Class−D Signal Layout

- Refer to Figure 30 & Figure 31 for examples of top−layer trace routing and layout for power, output and signal traces.

Thermal Management

For applications that use the ONA10IV at high continuous power ratings or at elevated ambient temperatures, layout techniques must be incorporated to ensure the ONA10IV does not exceed its designed thermal operating range in normal operation and operates as close to nominal operating temperature as possible for best reliability.

Often excessive heat is removed, by careful use of ground planes on various layers.

EMI Considerations

Designing for adequate EMI (Electro−Magnetic Interference) mitigation in Class−D audio applications is a necessity for electronic devices. Although the ONA10IV has I2C programmable options for assisting with EMI mitigation in an application (edge−rate control and spread−spectrum modulation of the Class−D output waveform), the most effective methods for EMI management are incorporated in the board design and layout.

- Output trace lengths and shielding/routing
- Output ferrite beads can also be considered but they have some audio performance trade−offs

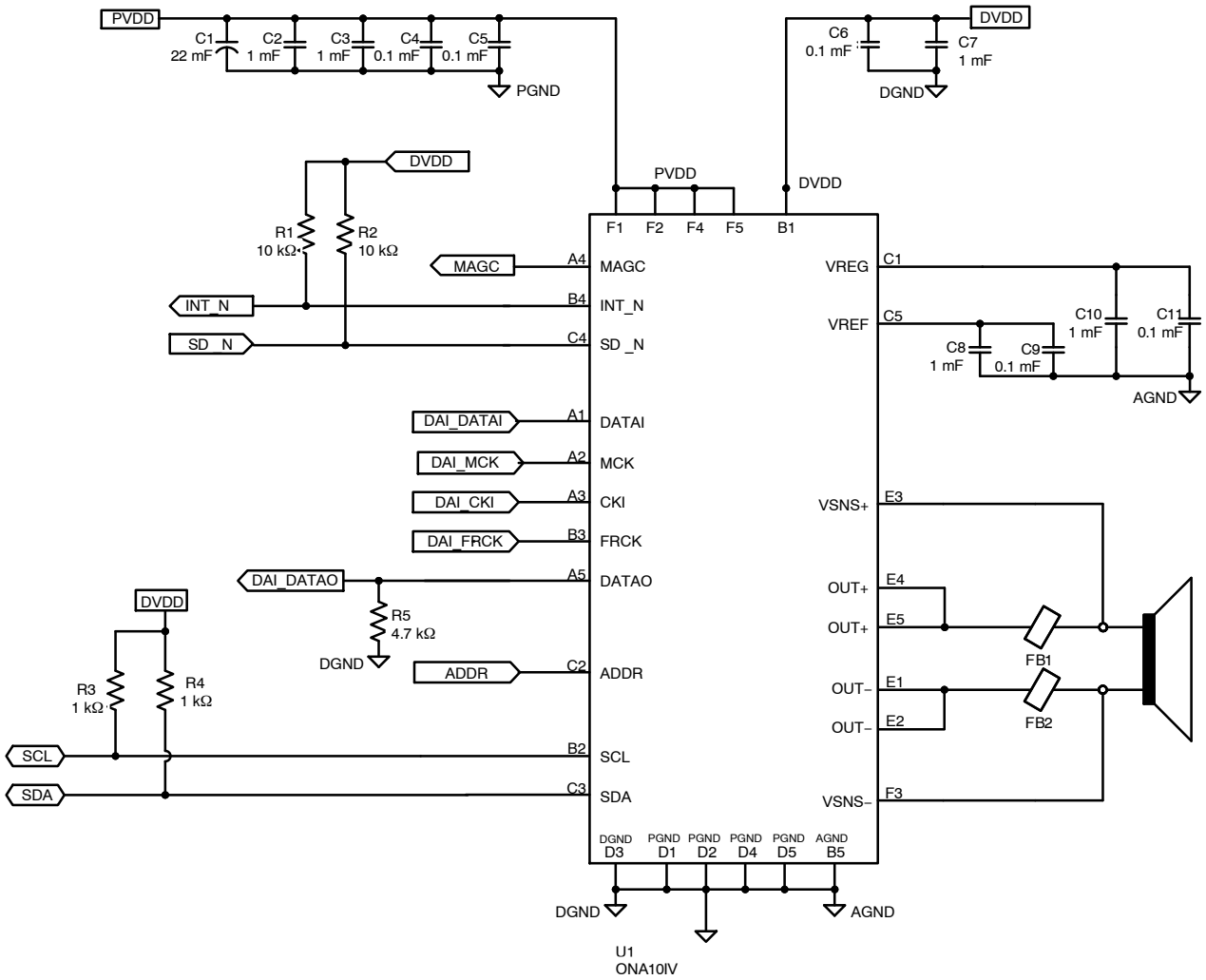


Figure 30. Key Signal Connection Schematic

Table 7. KEY COMPONENT − BILL OF MATERIALS

Ref Des	Qty	Description	Package	Manufacturer	Mfg P/N
U1	1	ONA10IV Digital Input Class−D Audio Amplifier	WLCSP30−330	ON Semiconductor	ONA10IVUCX
C1	1	22 μF capacitor, SMT, Tantalum, ±10%, 50 V	2924	AVX	TAJV226K050RNJ
C2, C3, C7, C8, C10	5	Capacitor, 1 μF, 0603, X7R, ±10%, 50 V	0603	Taiyo Yuden	UMK107AB7105KA−T
C4, C5, C9, C11	4	Capacitor, 0.1 μF, 0402, X7R, ±10%, 50 V	0402	Taiyo Yuden	UMK105B7104KV−FR
C6	1	Capacitor, 0.1 μF, 0402, X7R, ±10%, 6.3 V	0402	Samsung	CL05B104KQ5NNNC
FB1, FB2	2	Ferrite bead, 90 Ω @ 100 MHz, 5 ADC	0805	Vishay	ILHB0805ER900V
R1, R2	2	Resistor, 0402, 10 kΩ, 1%	0402	Yageo	AT0402FRE0710KL
R3, R4	2	Resistor, 0402, 1 kΩ, 1%	0402	Yageo	AT0402BRD071KL
R5	1	Resistor, 0402, 4.7 kΩ, 5%	0402	Yageo	AC0402JR−074K7L

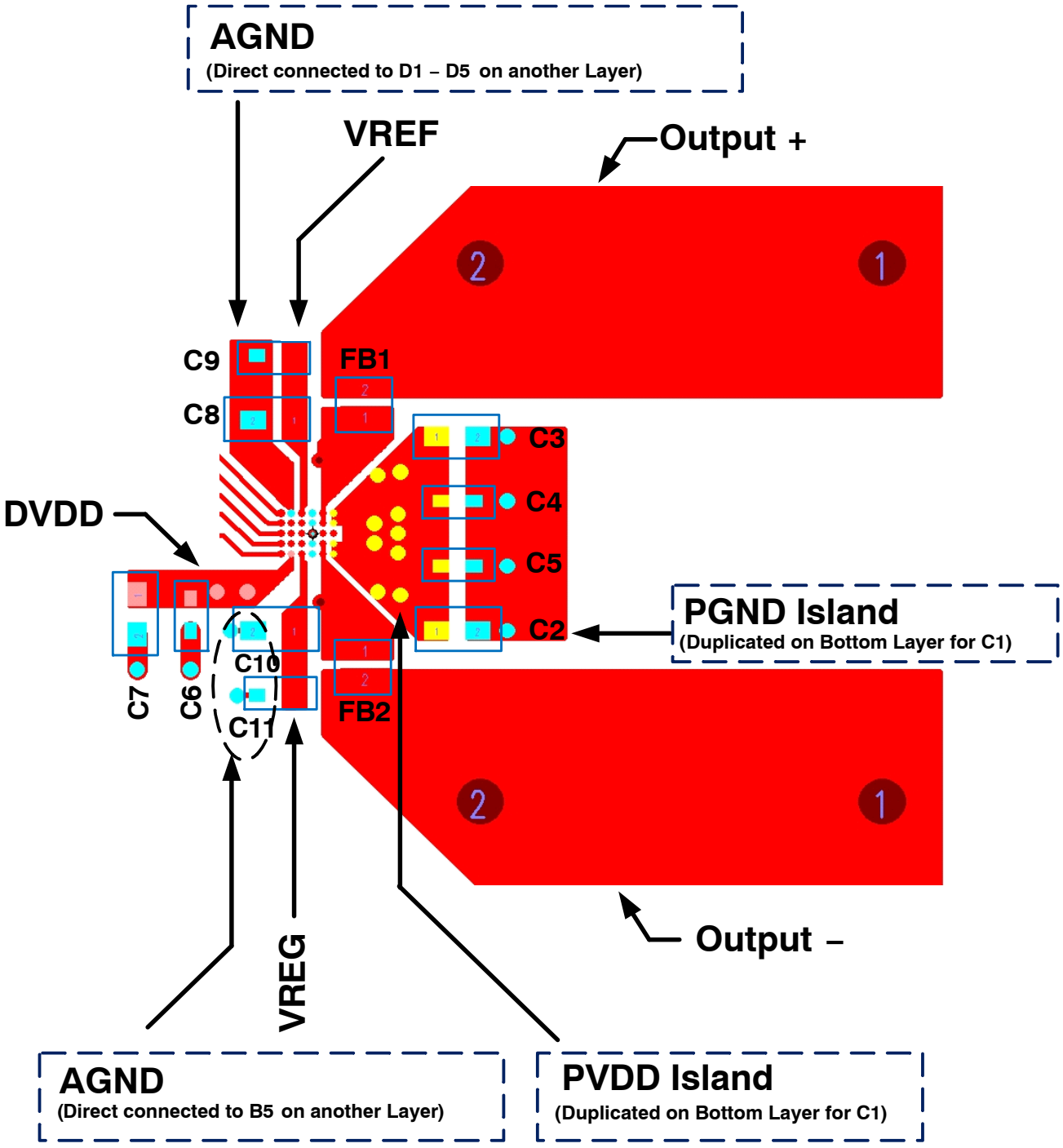


Figure 31. Top Copper Placement of Key Components

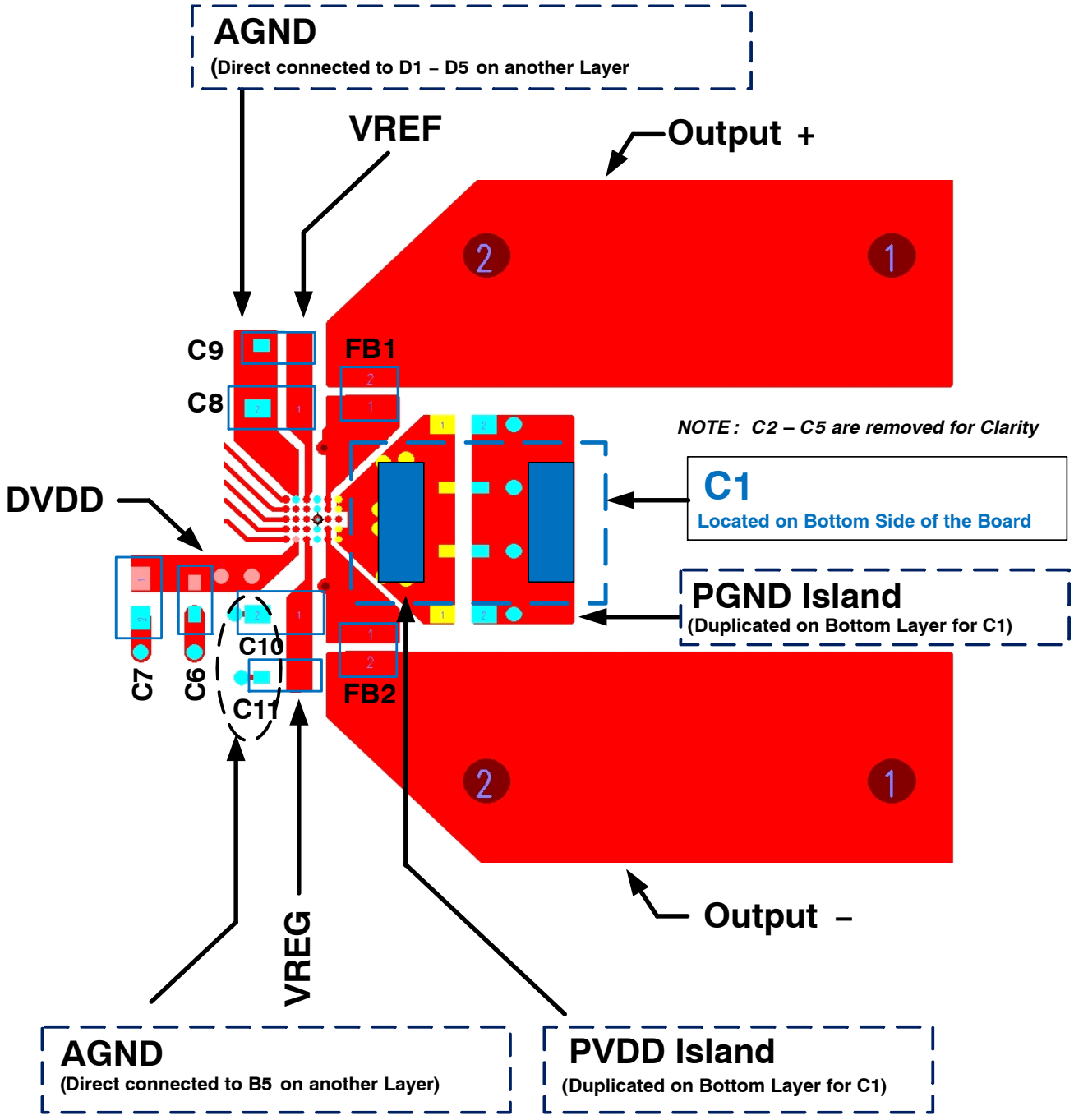
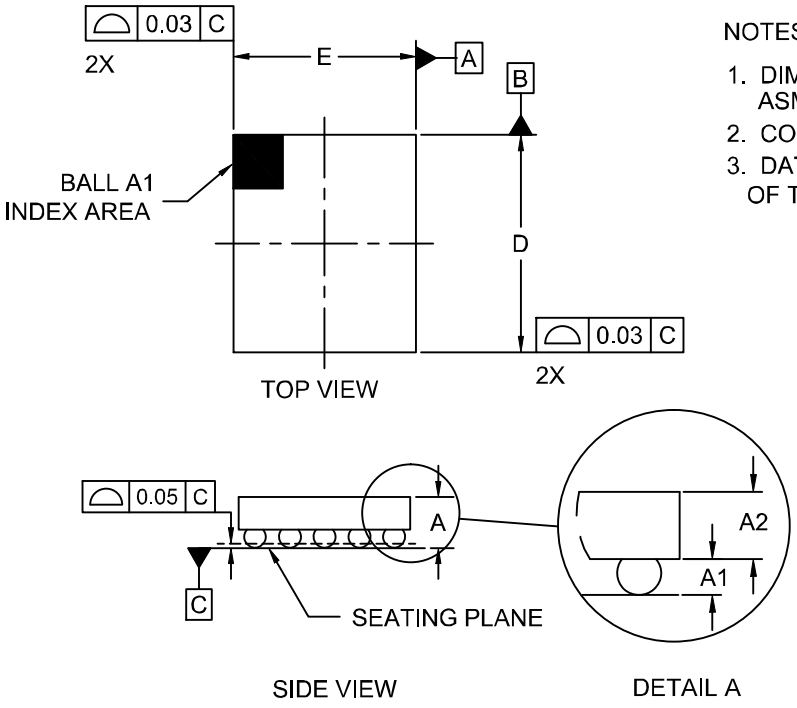


Figure 32. Location for the C1 Bulk Capacitor (Bottom Side of the Board)

ON Semiconductor is licensed by the Philips Corporation to carry the I²C bus protocol.

WLCSP30 2.89x2.31x0.586
CASE 567VB
ISSUE O

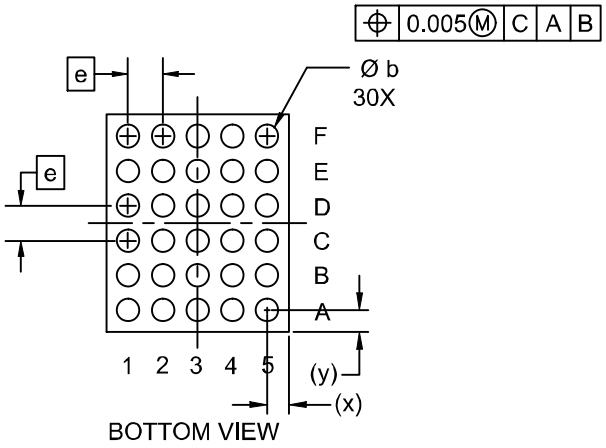
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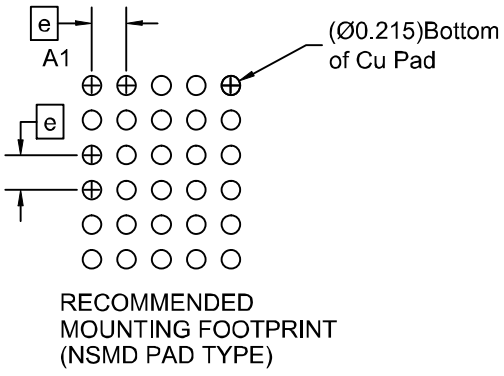


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.547	0.586	0.625
A1	0.187	0.208	0.229
A2	0.360	0.378	0.396
b	0.24	0.26	0.28
D	2.860	2.890	2.920
E	2.280	2.310	2.340
e	0.40 BSC		
x	0.34	0.355	0.37
y	0.43	0.445	0.46





ISSUE	REVISION	DATE
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