# CAT9555

## 16-bit I²C and SMBus I/O Port with Interrupt

## FEATURES

- **400kHz I²C bus compatible***
- **2.3V to 5.5V operation**
- **Low stand-by current**
- **5V tolerant I/Os**
- **16 I/O pins that default to inputs at power-up**
- **High drive capability**
- **Individual I/O configuration**
- **Polarity inversion register**
- **Active low interrupt output**
- **Internal power-on reset**
- **No glitch on power-up**
- **Noise filter on SDA/SCL inputs**
- **Cascadable up to 8 devices**
- **Industrial temperature range**
- **RoHS-compliant 24-lead SOIC and TSSOP, and 24-pad TQFN (4 x 4 mm) packages**

## APPLICATIONS

- **White goods (dishwashers, washing machines)**
- **Handheld devices (cell phones, PDAs, digital cameras)**
- **Data Communications (routers, hubs and servers)**

## DESCRIPTION

The CAT9555 is a CMOS device that provides 16-bit parallel input/output port expansion for I²C and SMBus compatible applications. These I/O expanders provide a simple solution in applications where additional I/Os are needed: sensors, power switches, LEDs, pushbuttons, and fans.

The CAT9555 consists of two 8-bit Configuration ports (input or output), Input, Output and Polarity inversion registers, and an I²C/SMBus-compatible serial interface.

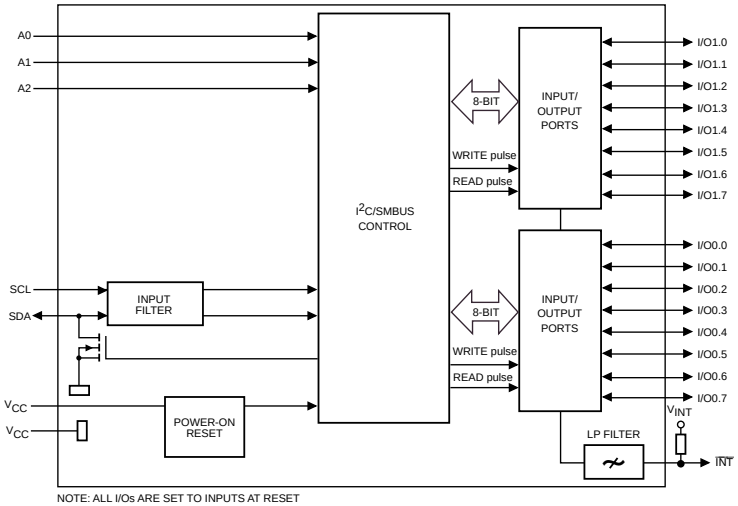
Any of the sixteen I/Os can be configured as an input or output by writing to the configuration register. The system master can invert the CAT9555 input data by writing to the active-high polarity inversion register.

The CAT9555 features an active low interrupt output which indicates to the system master that an input state has changed.

The three address input pins provide the device's extended addressing capability and allow up to eight devices to share the same bus. The fixed part of the I²C slave address is the same as the CAT9554, allowing up to eight of these devices in any combination to be connected on the same bus.

**For Ordering Information details, see page 16.**

## BLOCK DIAGRAM




NOTE: ALL I/Os ARE SET TO INPUTS AT RESET

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

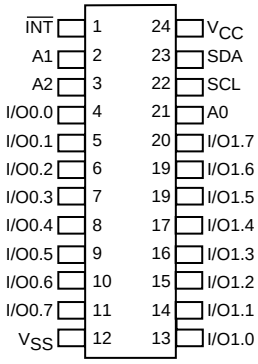




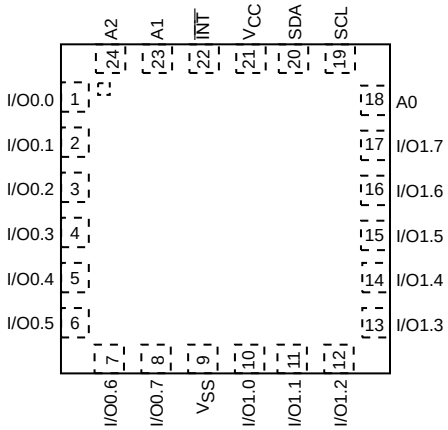
Doc. No. MD-9003, Rev. G

## PIN CONFIGURATION

### SOIC (W) / TSSOP (Y)




### TQFN (HV6)




4 x 4 mm
Top View

## PIN DESCRIPTION

| SOIC / TSSOP | TQFN | PIN NAME | FUNCTION |
|---|---|---|---|
| 1 | 22 | $\overline{INT}$ | Interrupt Output (open drain) |
| 2 | 23 | A1 | Address Input 1 |
| 3 | 24 | A2 | Address Input 2 |
| 4-11 | 1-8 | I/O0.0 - I/O0.7 | I/O Port 0.0 to I/O Port 0.7 |
| 12 | 9 | $V_{SS}$ | Ground |
| 13-20 | 10-17 | I/O1.0 - I/O1.7 | I/O Port 1.0 to I/O Port 1.7 |
| 21 | 18 | A0 | Address Input 0 |
| 22 | 19 | SCL | Serial Clock |
| 23 | 20 | SDA | Serial Data |
| 24 | 21 | $V_{CC}$ | Power Supply |

## ABSOLUTE MAXIMUM RATINGS[1]

$V_{CC}$ with Respect to Ground ..... –0.5V to +6.5V

Voltage on Any Pin with Respect to Ground ..... –0.5V to +5.5V

DC Current on $I/O_0$ to $I/O_7$ ..... ±50 mA

DC Input Current ..... ±20 mA

$V_{CC}$ Supply Current ..... 160mA

$V_{SS}$ Supply Current ..... 200mA

Package Power Dissipation Capability ($T_A$ = 25°C) ..... 1.0W

Junction Temperature ..... +150°C

Storage Temperature ..... -65°C to +150°C

## RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Reference Test Method | Min | Units |
|---|---|---|---|---|
| VZAP[2] | ESD Susceptibility | JEDEC Standard JESD22 | 2000 | Volts |
| ILTH[2] | Latch-up | JEDEC JESD78A | 100 | mA |

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) This parameter is tested initially and after a design or process change that affects the parameter.

## D.C. OPERATING CHARACTERISTICS

$V_{CC}$ = 2.3 to 5.5 V; $V_{SS}$ = 0V; $T_A$ = -40°C to +85°C, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CC}$ | Supply voltage | | 2.3 | — | 5.5 | V |
| $I_{CC}$ | Supply current | Operating mode; $V_{CC}$ = 5.5 V; no load; $f_{SCL}$ = 100 kHz | — | 135 | 200 | µA |
| $I_{stbl}$ | Standby current | Standby mode; $V_{CC}$ = 5.5 V; no load; $V_I$ = $V_{SS}$; $f_{SCL}$ = 0 kHz; I/O = inputs | — | 1.1 | 1.5 | mA |
| $I_{stbh}$ | Standby current | Standby mode; $V_{CC}$ = 5.5 V; no load; $V_I$ = $V_{CC}$; $f_{SCL}$ = 0 kHz; I/O = inputs | — | 0.75 | 1 | µA |
| $V_{POR}$ | Power-on reset voltage | No load; $V_I$ = $V_{CC}$ or VSS | — | 1.5 | 1.65 | V |
| **SCL, SDA, INT** | | | | | | |
| $V_{IL}$ (1) | Low level input voltage | | -0.5 | — | 0.3 $V_{CC}$ | V |
| $V_{IH}$ (1) | High level input voltage | | 0.7 $V_{CC}$ | — | 5.5 | V |
| $I_{OL}$ | Low level output current | $V_{OL}$ = 0.4V | 3 | — | — | mA |
| $I_L$ | Leakage current | $V_I$ = $V_{CC}$ = $V_{SS}$ | – 1 | — | +1 | µA |
| $C_I$ (2) | Input capacitance | $V_I$ = $V_{SS}$ | — | — | 6 | pF |
| $C_O$ (2) | Output capacitance | $V_O$ = $V_{SS}$ | — | — | 8 | pF |
| **A0, A1, A2** | | | | | | |
| $V_{IL}$(1) | Low level input voltage | | -0.5 | — | 0.3 $V_{CC}$ | V |
| $V_{IH}$(1) | High level input voltage | | 0.7 $V_{CC}$ | — | 5.5 | V |
| $I_{LI}$ | Input leakage current | | -1 | — | 1 | µA |
| **I/Os** | | | | | | |
| $V_{IL}$ | Low level input voltage | | -0.5 | — | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | High level input voltage | | 0.7 $V_{CC}$ | — | 5.5 | V |
| $I_{OL}$ | Low level output current | $V_{OL}$ = 0.5 V; $V_{CC}$ = 2..3 V to 5.5 V (3) | 8 | 8 to 20 | — | mA |
| | | $V_{OL}$ = 0.7 V; $V_{CC}$ = 2..3 V to 5.5 V (3) | 10 | 10 to 24 | — | mA |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = – 8 mA; $V_{CC}$ = 2.3 V; (4) | 1.8 | — | — | V |
| | | $I_{OH}$ = – 10 mA; $V_{CC}$ = 2.3 V; (4) | 1.7 | — | — | V |
| | | $I_{OH}$ = – 8 mA; $V_{CC}$ = 3.0 V; (4) | 2.6 | — | — | V |
| | | $I_{OH}$ = – 10 mA; $V_{CC}$ = 3.0 V; (4) | 2.5 | — | — | V |
| | | $I_{OH}$ = – 8 mA; $V_{CC}$ = 4.75 V; (4) | 4.1 | — | — | V |
| | | $I_{OH}$ = – 10 mA; $V_{CC}$ = 4.75 V; (4) | 4.0 | — | — | V |
| $I_{IH}$ | Input leakage current | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ | — | — | 1 | µA |
| $I_{IL}$ | Input leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{SS}$ | — | — | -100 | µA |
| $C_I$ (2) | Input capacitance | | — | — | 5 | pF |
| $C_O$ (2) | Output capacitance | | — | — | 8 | pF |

Notes:
1. $V_{IL}$ min and $V_{IH}$ max are reference values only and are not tested.
2. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
3. Each I/Os must be externally limited to a maximum of 25 mA and each octal (I/O0.0 to I/O0.7 and I/O1.0 to I/O1.7) must be limited to a maximum current of 100 mA for a device total of 200 mA.
4. The total current sourced by all I/Os must be limited to 160 mA.

## A.C. CHARACTERISTICS

$V_{CC}$ = 2.3V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise specified (Note 1).

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency | | 400 | kHz |
| $t_{SP}$ | Input Filter Spike Suppression (SDA, SCL) | | 50 | ns |
| $t_{LOW}$ | Clock Low Period | 1.3 | | µs |
| $t_{HIGH}$ | Clock High Period | 0.6 | | µs |
| $t_R$ (2) | SDA and SCL Rise Time | 20 | 300 | ns |
| $t_F$ (2) | SDA and SCL Fall Time | 20 | 300 | ns |
| $t_{HD:STA}$ | Start Condition Hold Time | 0.6 | | µs |
| $t_{SU:STA}$ | Start Condition Setup Time (for a Repeated Start) | 0.6 | | µs |
| $t_{HD:DAT}$ | Data Input Hold Time | 0 | | ns |
| $t_{SU:DAT}$ | Data In Setup Time | 100 | | ns |
| $t_{SU:STO}$ | Stop Condition Setup Time | 0.6 | | µs |
| $t_{AA}$ | SCL Low to Data Out Valid | | 900 | ns |
| $t_{DH}$ | Data Out Hold Time | 50 | | ns |
| $t_{BUF}$ (2) | Time the Bus must be Free Before a New Transmission Can Start | 1.3 | | µs |
| **Port Timing** | | | | |
| $t_{PV}$ | Output Data Valid | | 200 | ns |
| $t_{PS}$ | Input Data Setup Time | 100 | | ns |
| $t_{PH}$ | Input Data Hold Time | 1 | | µs |
| **Interrupt Timing** | | | | |
| $t_{IV}$ | Interrupt Valid | | 4 | µs |
| $t_{IR}$ | Interrupt Reset | | 4 | µs |

Notes:
1. Test conditions according to "AC Test Conditions" table.
2. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Rise and Fall time | < = 10ns |
| CMOS Input Voltages | $0.2V_{CC}$ to $0.8V_{CC}$ |
| CMOS Input Reference Voltages | $0.3V_{CC}$ to $0.7V_{CC}$ |
| Output Reference Voltages | $0.5V_{CC}$ |
| Output Load: SDA, INT | Current Souce $I_{OL}$ = 3mA; $C_L$ = 100pF |
| Output Load: I/Os | Current Source: $I_{OL}/I_{OH}$ = 10mA; $C_L$ = 50pF |

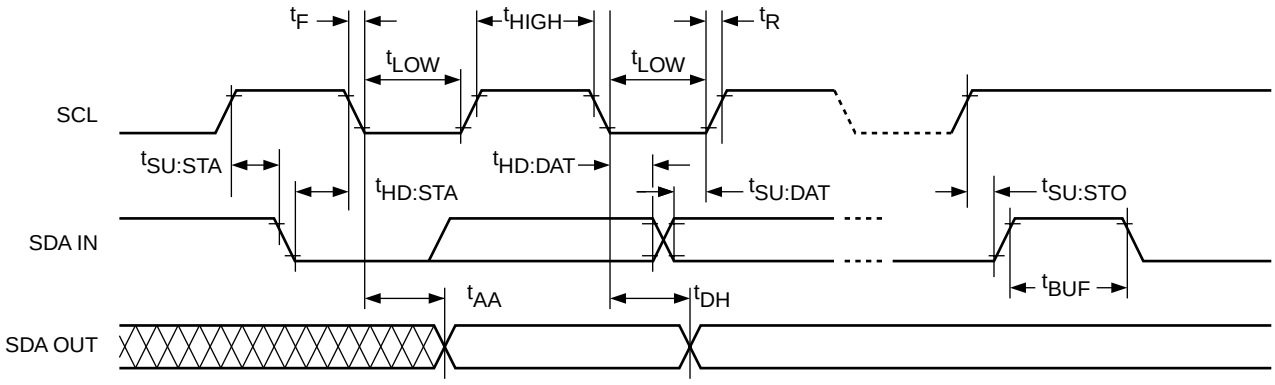



**Figure 1. 2-Wire Serial Interface Timing**

## PIN DESCRIPTION

### SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull-up resistor if it is driven by an open drain output.

### SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs. A pull-up resistor must be connected from SDA line to $V_{CC}$. The value of the pull-up resistor, Rp, can be calculated based on minimum and maximum values from Figure 2 and Figure 3 (see Note).

### A0, A1, A2: Device Address Inputs

These inputs are used for extended addressing capability. The A0, A1, A2 pins should be hardwired to $V_{CC}$ or $V_{SS}$. When hardwired, up to eight CAT9555s may be addressed on a single bus system. The levels on these inputs are compared with corresponding bits, A2, A1, A0, from the slave address byte.

### I/O 0.0 to I/O 0.7, I/O 1.0 to I/O 1.7: Input / Output Ports

Any of these pins may be configured as input or output. The simplified schematic of I/Os is shown in Figure 4. When an I/O is configured as an input, the Q1 and Q2 output transistors are off creating a high impedance input with a weak pull-up resistor (typical 100 kohm). If the I/O pin is configured as an output, the push-pull output stage is enabled. Care should be taken if an external voltage is applied to an I/O pin configured as an output due to the low impedance paths that exist between the pin and either $V_{CC}$ or $V_{SS}$.

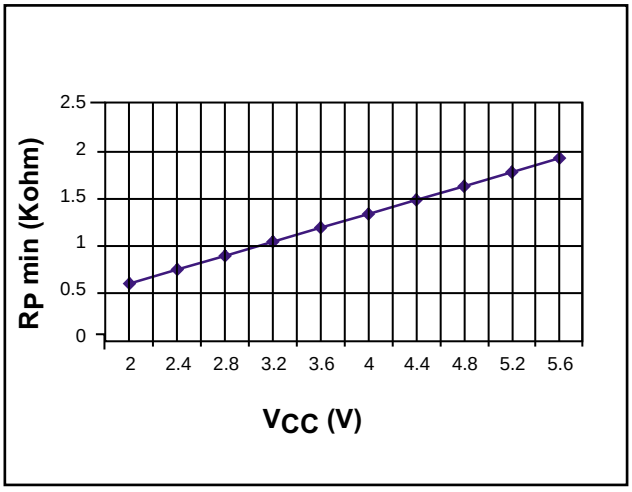



**Figure 2. Minimum Rp as a Function of Supply Voltage ($I_{OL}$ = 3mA @ $V_{OL\ max}$)**

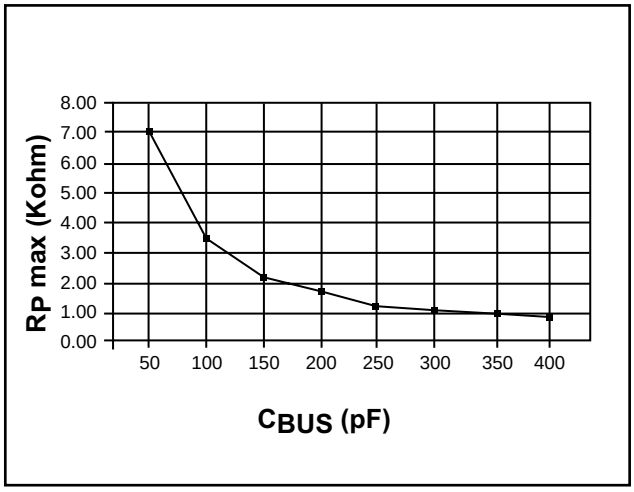



**Figure 3. Maximum Rp Value versus Bus Capacitance (Fast Mode $I^2C$ Bus / $t_{r\ max}$ = 300ns)**

Note: According to the Fast Mode $I^2C$ bus specification, for bus capacitance up to 200pF, the pull up device can be a resistor. For bus loads between 200pF and 400pF, the pull-up device can be a current source (Imax = 3mA) or a switched resistor circuit.

### $\overline{INT}$: Interrupt Output

The open-drain interrupt output is activated when one of the port pins configured as an input changes state (differs from the corresponding input port register bit state). The interrupt is deactivated when the input returns to its previous state or the input port register is read.

Since there are two 8-bit ports that are read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1, or vice versa.

Changing an I/O from an output to an input may cause a false interrupt if the state of the pin does not match the contents of the input port register.

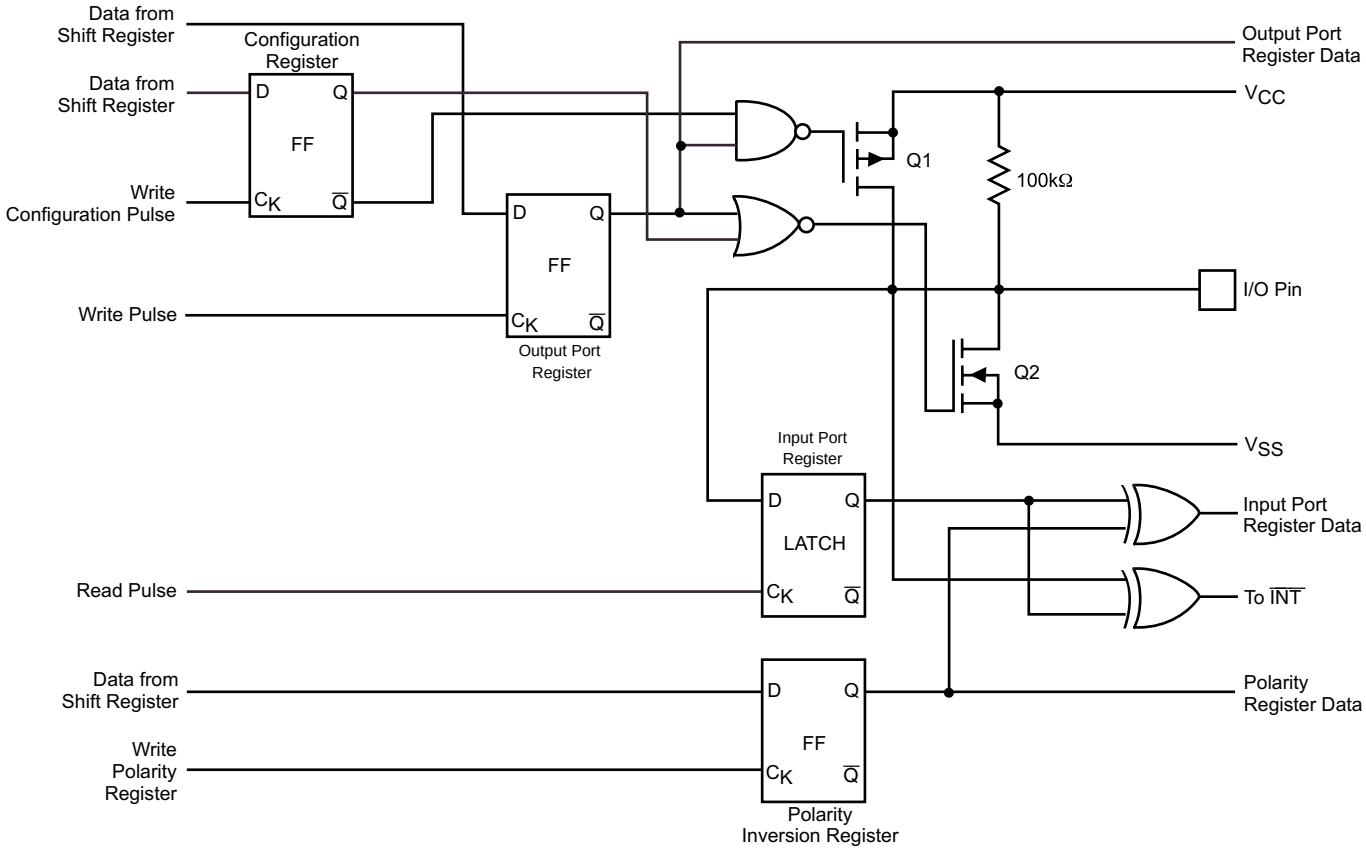



**Figure 4. Simplified Schematic of I/Os**

## FUNCTIONAL DESCRIPTION

The CAT9555 general purpose input/output (GPIO) peripheral provides up to sixteen I/O ports, controlled through an $I^2C$ compatible serial interface

The CAT9555 supports the $I^2C$ Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9555 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

### $I^2C$ Bus Protocol

The features of the $I^2C$ bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 5).

### START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9555 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

### Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9555 for a read or write operation. The four most significant bits of the slave address are fixed as binary 0100 (Figure 6). The CAT9555 uses the next three bits as address bits.

The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7-bit slave address is the R/$\overline{W}$ bit that specifies whether a read or write operation is to be performed. When this bit is set to “1”, a read operation is initiated, and when set to “0”, a write operation is selected.

Following the START condition and the slave address byte, the CAT9555 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT9555 then performs a read or a write operation depending on the state of the R/$\overline{W}$ bit.

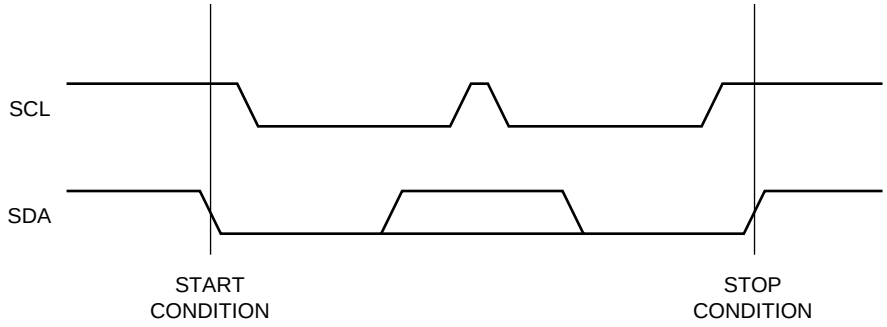



**Figure 5. Start/Stop Timing**

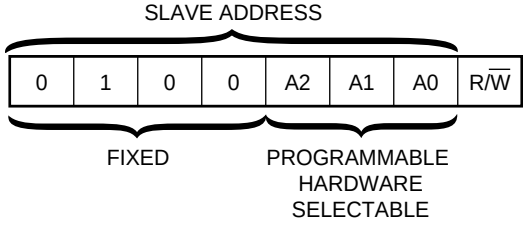



**Figure 6. CAT9555 Slave Address**

### Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 7).

The CAT9555 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each data byte.

When the CAT9555 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9555 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a stop condition to return the CAT9555 to the standby power mode and place the device in a known state.

### Registers and Bus Transactions

The CAT9555 internal registers and their address and function are shown in Table 1.

**Table 1. Register Command Byte**

| Command (hex) | Register |
|---|---|
| 0h | Input Port 0 |
| 1h | Input Port 1 |
| 2h | Output Port 0 |
| 3h | Output Port 1 |
| 4h | Polarity Inversion Port 0 |
| 5h | Polarity Inversion Port 1 |
| 6h | Configuration Port 0 |
| 7h | Configuration Port 1 |

The command byte is the first byte to follow the device address byte during a write/read bus transaction. The register command byte acts as a pointer to determine which register will be written or read.

The input port register is a read only port. It reflects the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.

**Table 2. Registers 0 and 1 – Input Port Registers**

| bit | IO.7 | IO.6 | IO.5 | IO.4 | IO.3 | IO.2 | IO.1 | IO.0 |
|---|---|---|---|---|---|---|---|---|
| default | X | X | X | X | X | X | X | X |
| bit | I1.7 | I1.6 | I1.5 | I1.4 | I1.3 | I1.2 | I1.1 | I1.0 |
| default | X | X | X | X | X | X | X | X |

The default value 'X' is determined by the externally applied logic lavel

**Table 3. Registers 2 and 3 – Output Port Registers**

| bit | O0.7 | O0.6 | O0.5 | O0.4 | O0.3 | O0.2 | O0.1 | O0.0 |
|---|---|---|---|---|---|---|---|---|
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| bit | O1.7 | O1.6 | O1.5 | O1.4 | O1.3 | O1.2 | O1.1 | O1.0 |
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 4. Registers 4 and 5 – Polarity Inversion Registers**

| bit | N0.7 | N0.6 | N0.5 | N0.4 | N0.3 | N0.2 | N0.1 | N0.0 |
|---|---|---|---|---|---|---|---|---|
| default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| bit | N1.7 | N1.6 | N1.5 | N1.4 | N1.3 | N1.2 | N1.1 | N1.0 |
| default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 5. Registers 6 and 7 – Configuration Registers**

| bit | C0.7 | C0.6 | C0.5 | C0.4 | C0.3 | C0.2 | C0.1 | C0.0 |
|---|---|---|---|---|---|---|---|---|
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| bit | C1.7 | C1.6 | C1.5 | C1.4 | C1.3 | C1.2 | C1.1 | C1.0 |
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

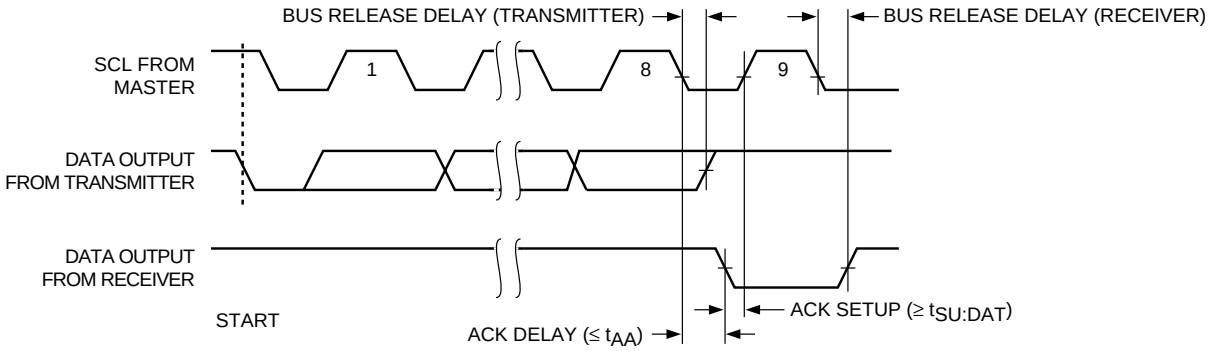



**Figure 7. Acknowledge Timing**

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip-flop controlling the output, not the actual I/O pin value.

The polarity inversion register allows the user to invert the polarity of the input port register data. If a bit in this register is set (“1”) the corresponding input port data is inverted. If a bit in the polarity inversion register is cleared (“0”), the original input port polarity is retained.

The configuration register sets the directions of the ports. Set the bit in the configuration register to enable the corresponding port pin as an input with a high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At power-up, the I/Os are configured as inputs with a weak pull-up resistor to VCC.

### Writing to the Port Registers

Data is transmitted to the CAT9555 registers using the write mode shown in Figure 8 and Figure 9.

The CAT9555 registers are configured to operate at four register pairs: Input Ports, Output Ports, Polarity Inversion Ports and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair. For example, if the first byte of data is sent to the Configuration Port 1 (register 7), the next byte will be stored in the Configuration Port 0 (register 6). Each 8-bit register may be updated independently of the other registers.

### Reading the Port Registers

The CAT9555 registers are read according to the timing diagrams shown in Figure 10 and Figure 11. Data from the register, defined by the command byte, will be sent serially on the SDA line. Data is clocked into the register on the failing edge of the acknowledge clock pulse. After the first byte is read, additional data bytes may be read, but the second read will reflect the data from the other register in the pair. For example, if the first read is data from Input Port 0, the next read data will be from Input Port 1. The transfer is stopped when the master will not acknowledge the data byte received and issue the STOP condition.

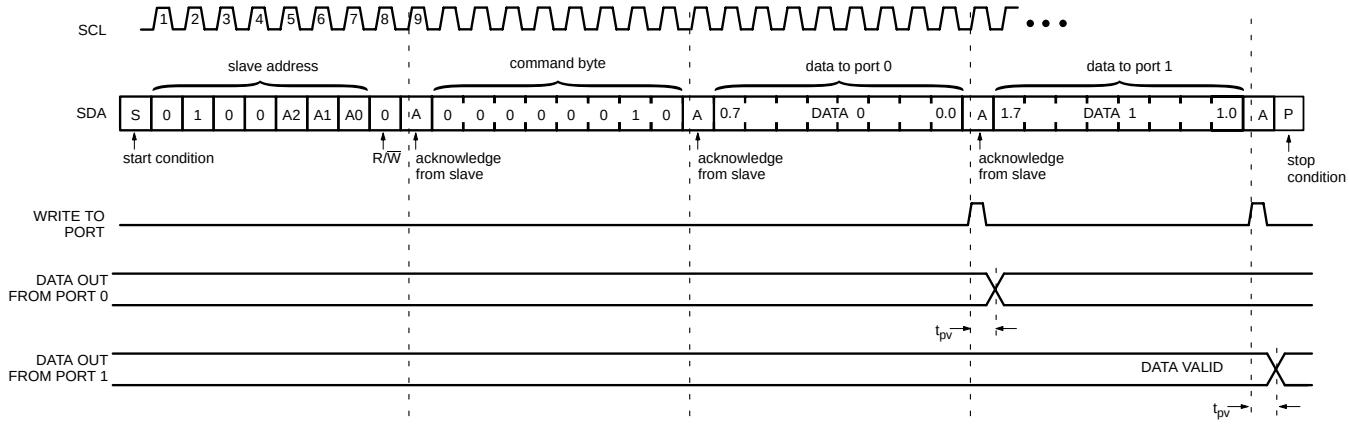



**Figure 8. Write to Output Port Registers**

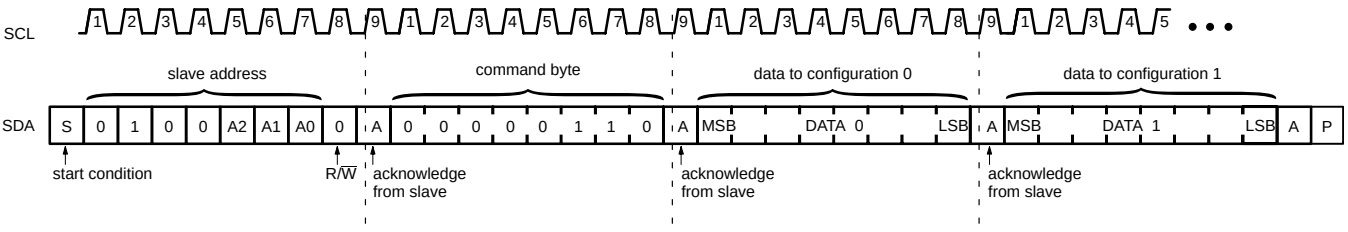
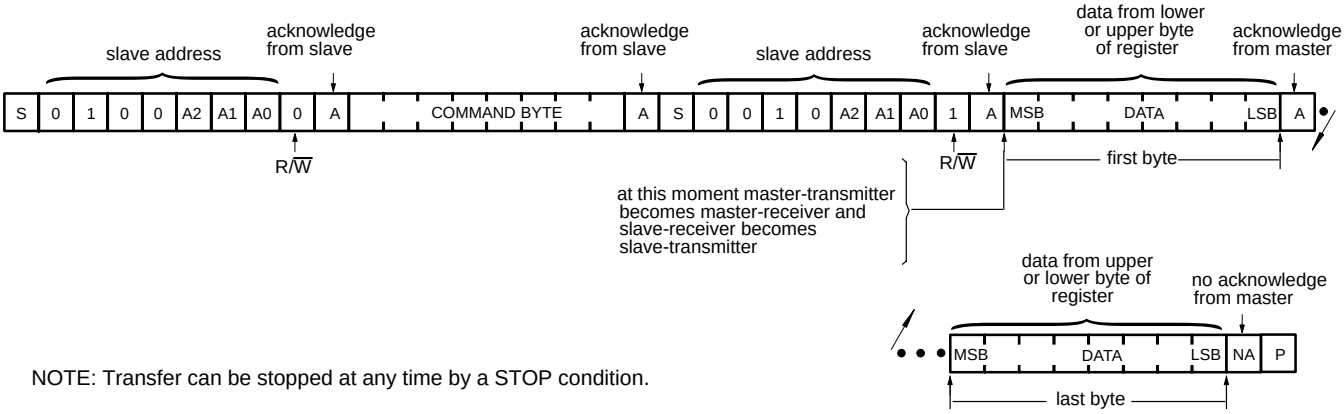



**Figure 9. Write to Configuration Registers**

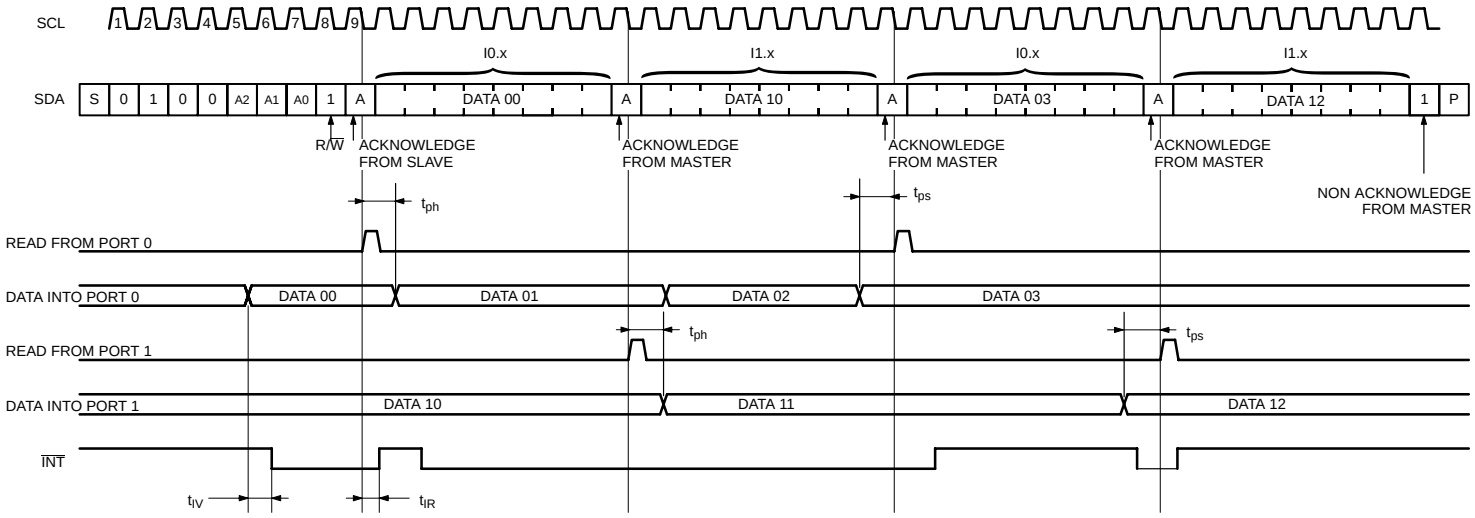
### Power-On Reset Operation

When the power supply is applied to VCC pin, an internal power-on reset pulse holds the CAT9555 in a reset state until VCC reaches $V_{POR}$ level. At this point, the reset condition is released and the internal state machine and the CAT9555 registers are initialized to their default state.




NOTE: Transfer can be stopped at any time by a STOP condition.

**Figure 10. Read from Register**

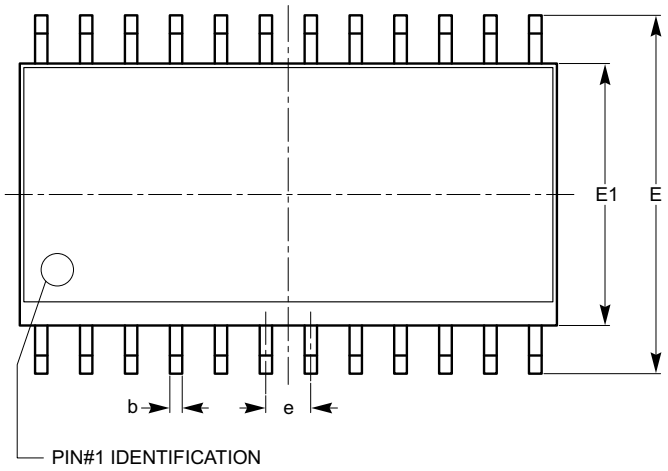



NOTE: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to 00 (read input port register).

**Figure 11. Read Input Port Register**

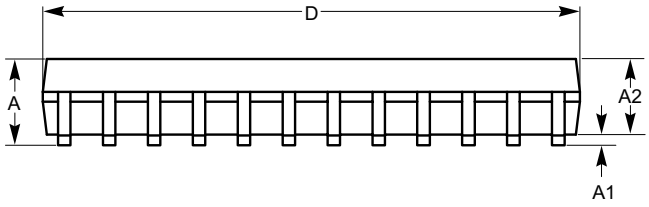
## PACKAGE OUTLINE DRAWINGS

## SOIC 24-Lead 300mils (W)

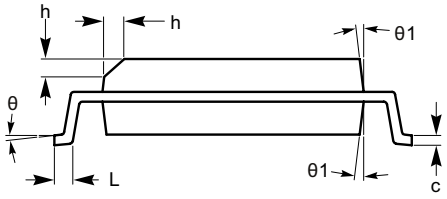



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 2.35 | | 2.65 |
| A1 | 0.10 | | 0.30 |
| A2 | 2.05 | | 2.55 |
| b | 0.31 | | 0.51 |
| c | 0.20 | | 0.33 |
| D | 15.20 | | 15.40 |
| E | 10.11 | | 10.51 |
| E1 | 7.34 | | 7.60 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.75 |
| L | 0.40 | | 1.27 |
| θ | 0° | | 8° |
| θ1 | 5° | | 15° |




SIDE VIEW

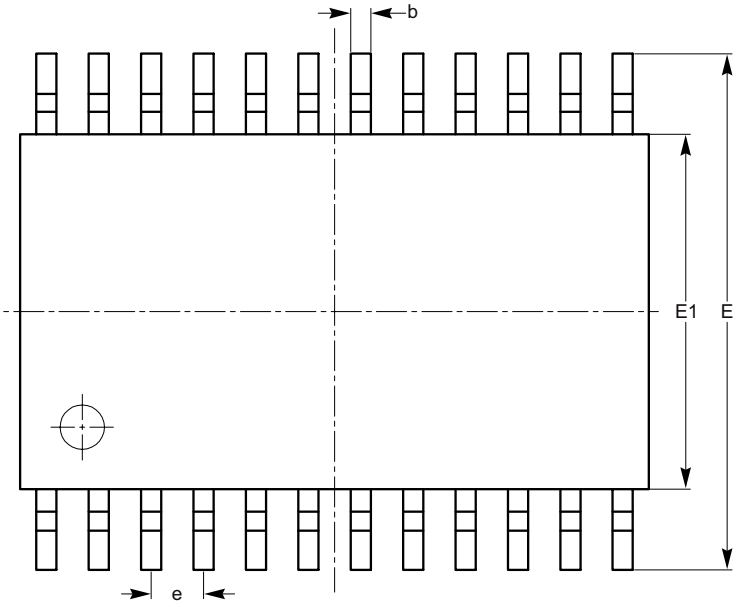



END VIEW

**For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.**

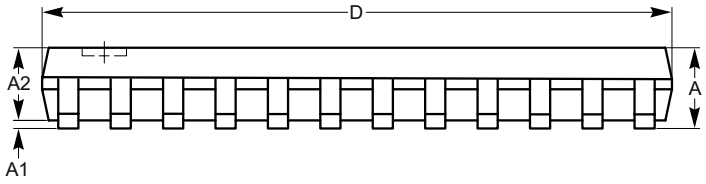
Notes:
1. All dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC Standard MS-013

## TSSOP 24-Lead 4.4 (Y)

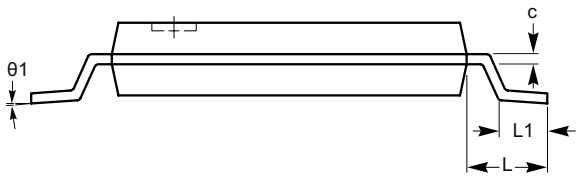



TOP VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 7.70 | 7.80 | 7.90 |
| E | 6.25 | 6.40 | 6.55 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | | 0.65 BSC | |
| L | | 1.00 REF | |
| L1 | 0.50 | 0.60 | 0.70 |
| θ1 | 0° | | 8° |




SIDE VIEW

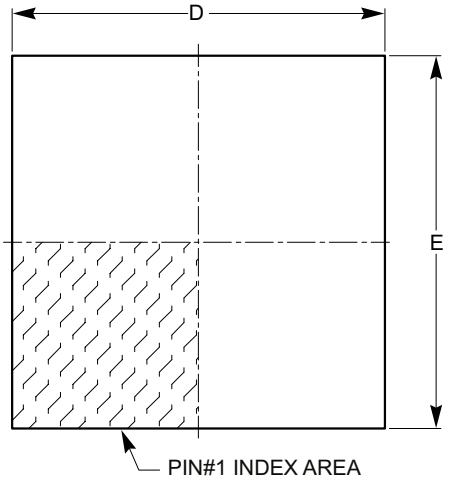



END VIEW

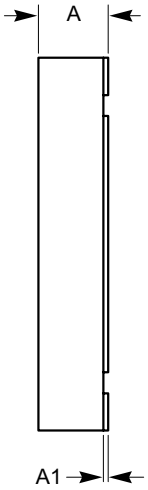
**For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.**

Notes:
1. All dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC Standard MO-153

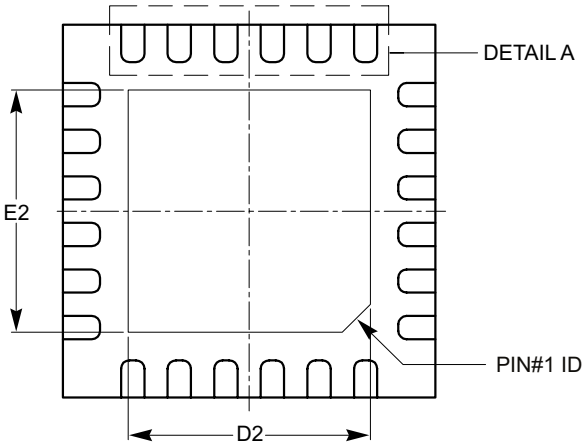
## TQFN 24-Pad 4 x 4mm (HV6)




TOP VIEW

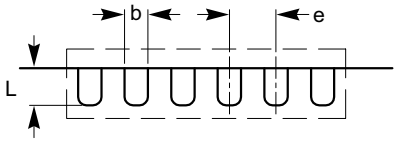



SIDE VIEW

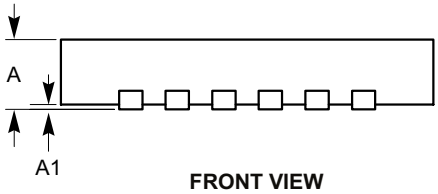



BOTTOM VIEW

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.70 | 2.80 | 2.90 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.70 | 2.80 | 2.90 |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |




DETAIL A

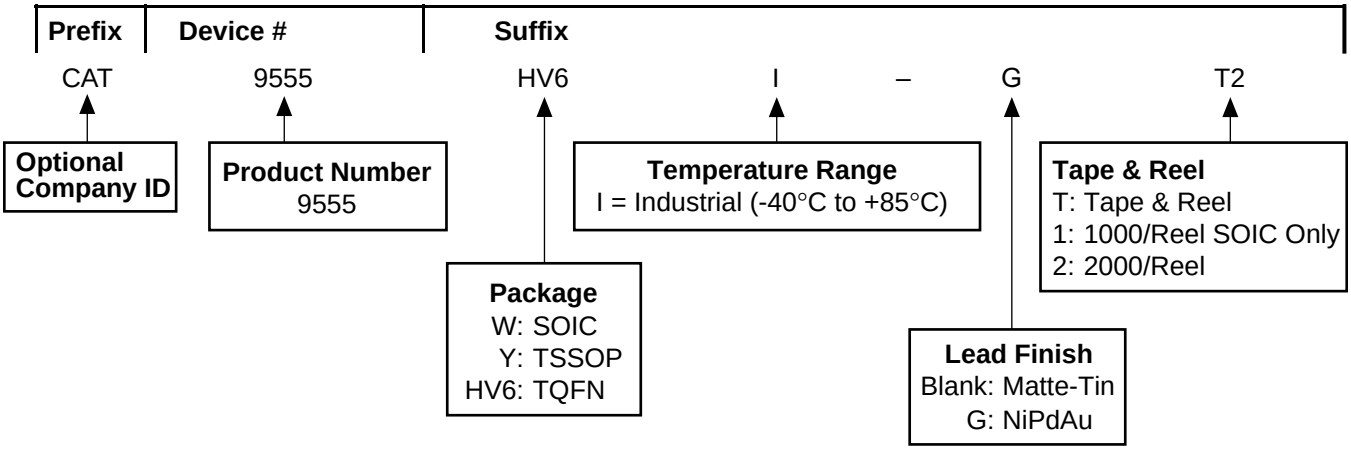



FRONT VIEW

**For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.**

Notes:
1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MO-220

## EXAMPLE OF ORDERING INFORMATION




## ORDERING PART NUMBER

| Part Number | Package | Lead Finish |
|---|---|---|
| CAT9555WI | SOIC | Matte-Tin |
| CAT9555WI-T1 | SOIC | Matte-Tin |
| CAT9555YI | TSSOP | Matte-Tin |
| CAT9555YI-T2 | TSSOP | Matte-Tin |
| CAT9555HV6I | TQFN | Matte-Tin |
| CAT9555HV6I-T2 | TQFN | Matte-Tin |
| CAT9555HV6I-G | TQFN | NiPdAu |
| CAT9555HV6I-GT2 | TQFN | NiPdAu |

Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is Matte-Tin for SOIC and TSSOP packages and NiPdAu on TQFN package.
(3) The device used in the above example is a CAT9555HV6I-GT2 (TQFN, Industrial Temperature, NiPdAu, 2000 pcs / Reel).
(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

## REVISION HISTORY

| Date | Rev. | Reason |
|---|---|---|
| 12/9/2004 | A | *Advance Information* - Initial Issue |
| 1/7/2005 | B | *Advance Information* - Minor changes |
| 03/11/05 | C | *Advance Information* -<br>Edit Features<br>Edit Ordering Information |
| 09/25/06 | D | Initial Release |
| 03/12/07 | E | Update Ordering Information: Tape and Reel for SOIC package |
| 06/07/07 | F | Update Figure 6 |
| 01/21/08 | G | Add NiPdAu lead finish for TQFN package<br>Update Example of Ordering Information<br>Update Package Outline Drawings<br>Change document number from 8551 |



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