S72MS-P based MCP/PoP Products

1.8 Volt-only x16 Flash Memory and SDRAM on Split Bus
NAND Interface ORNAND™ Flash on Bus 1
Mobile SDRAM on Bus 2

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S72MS-P_00 **Revision** 01 **Issue Date** September 14, 2006

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Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

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When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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S72MS-P based MCP/PoP Products

1.8 Volt-only x16 Flash Memory and SDRAM on Split Bus NAND Interface ORNAND™ Flash on Bus 1 Mobile SDRAM on Bus 2

Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 1.7 to 1.95V**
- **Flash access time: 25 ns for ORNAND Flash**
- **Mobile SDRAM burst frequency: 104 MHz (SDR), 133 MHz (DDR)**
- **ORNAND bus width: x8 or x16**
- **Package:**
- **11.0 x 13.0 mm MCP**
- **Operating Temperature**
- **–25°C to +85°C (wireless)**

The S72MS series is a product line of stacked packages and consists of:

- **One or two NAND Interface ORNAND die**
- **Separate bus for one or more Mobile SDRAM die**

The products covered by this document are listed in the table below.

Device	ORNAND Flash Density		DRAM Density		
	1024Mb	512Mb	512Mb	256Mb	128Mb
S72MS512PE0HF94V		X (x8)		X (x16 SDR)	

For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S30MS-P	S30MS-P_00
256 Mb Mobile SDR-DRAM Type 5	SDRAM_10

Publication Number S72MS-P_00 **Revision** 01 **Issue Date** September 14, 2006

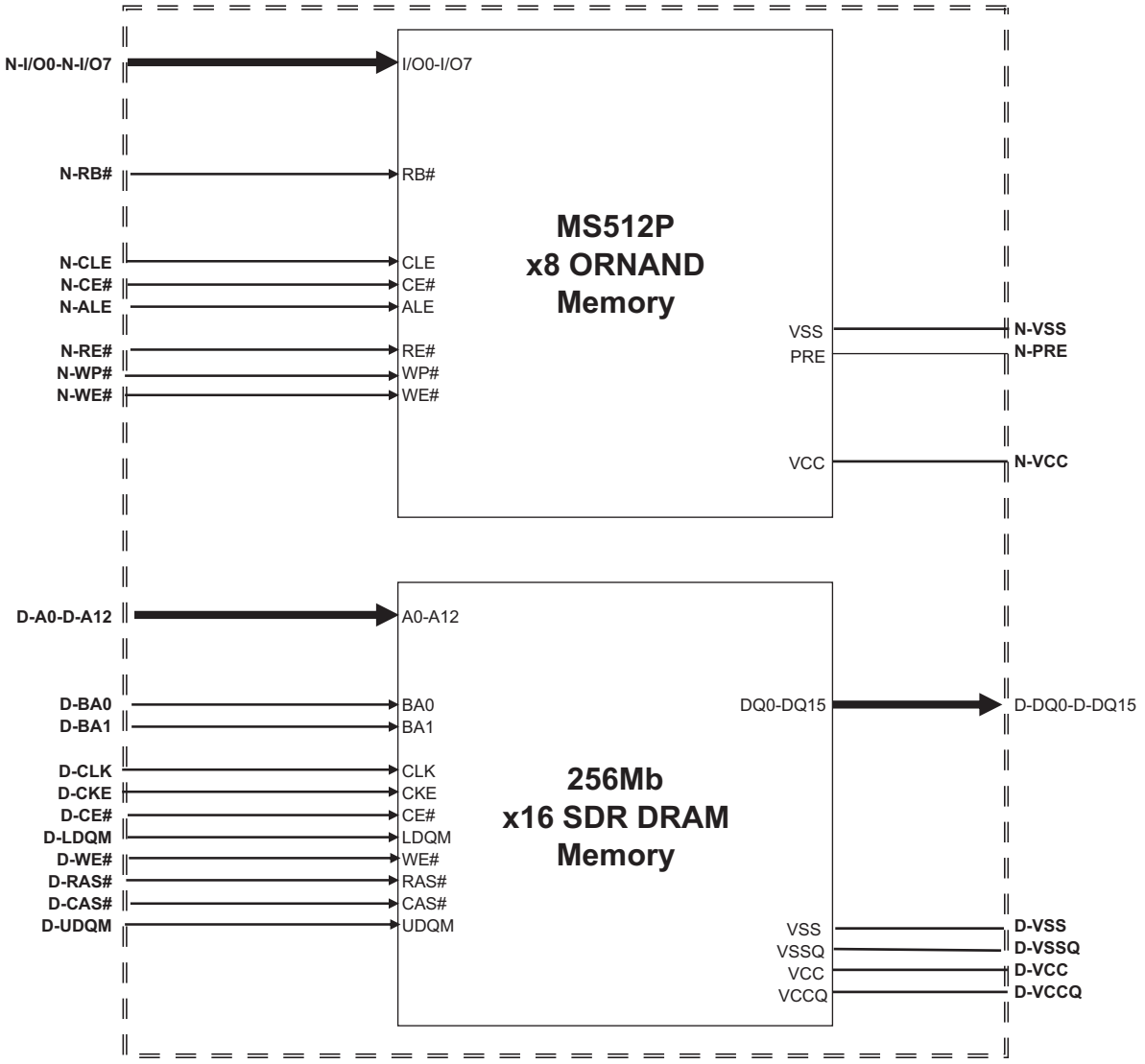
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1. Product Selector Guide

Device-Model#	ORNAND Flash Density	ORNAND Bus Width	ECC Required	DRAM Density	DRAM Speed	DRAM Supplier	Package
S72MS512PE0HF94V	512 Mb	x8	Yes	256 Mb	104 MHz (SDR)	Type 5	MCP 11x13mm 137-ball

2. Product Block Diagram

2.1 ORNAND Flash + DRAM MCP

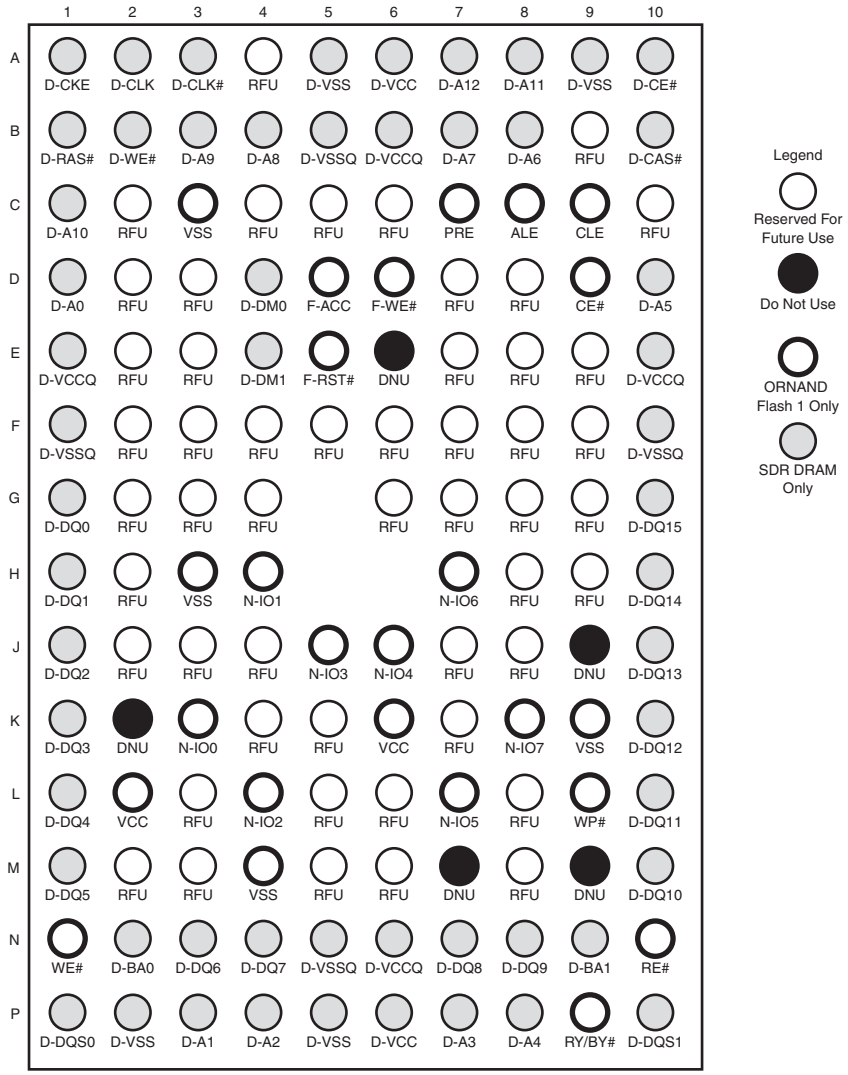


Note

1. *For MCPs, V_{SS} is shared between all Flash (NOR and ORNAND). Also, V_{SSQ} is tied to V_{SS} internally within the MCP.*

3. Connection Diagrams

3.1 512 Mb x8 ORNAND Flash with 256 Mb DRAM



3.1.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150×C for prolonged periods of time.

3.1.2 Look-ahead Ballout for Future Designs

Please refer to the Design-in Scalable Wireless Solutions with Spansion Products application note (publication number: Design_Scalable_Wireless_A0_E). Contact your local Spansion sales representative for more details.

3.2 DRAM Input/Output Descriptions

D-Amax-D-A0	SDRAM Address inputs
D-DQ15-D-DQ0	SDRAM Data input/output
D-CLK	SDRAM System Clock
D-CE#	SDRAM Chip Select
D-CKE	SDRAM Clock Enable
D-BA1-BA0	SDRAM Bank Select
D-RAS#	SDRAM Row Address Strobe
D-CAS#	SDRAM Column Address Strobe
D-DM1-D-DM0	SDRAM Data Input Mask
D-WE#	SDRAM Write Enable input
D-V_{SS}	SDRAM Ground
D-CLK#	DDR SDRAM Clock - in addition to D-CLK, this signal is available for DDRAMs that need CLK# for normal operations
D-V_{SSQ}	SDRAM Input/Output Buffer ground
D-V_{CCQ}	SDRAM Input/Output Buffer power supply
D-V_{CC}	SDRAM device power supply
D-DQS0 - D-DQS1	DDR SDRAM Data Strobe pins. DQS provides the read data strobes (as output) and the write data strobes (as input). Each DQS pin corresponds to eight DQ pins, respectively.

Note
Some of the signal descriptions specifically apply to DDR DRAM only.

3.2.1 ORNAND Signal Descriptions

N-PRE	ORNAND Power-On Read Enable. Tie to V_{SS} on customer board if not used
N-ALE	ORNAND Address Latch Enable
N-CLE	ORNAND Command Latch Enable
N-CE#	ORNAND Chip-enablE
N-WP#	ORNAND Write-protect
N-WE#	ORNAND Write-enable
N-RE#	ORNAND Read-enable
N-RY/BY#	ORNAND Ready-Busy
N-I/O0-N-I/O15	ORNAND I/O Signals (I/O0-I/O7 for x8 bus width)
N-V_{CC}	ORNAND Power Supply

4. Ordering Information

The order number is formed by a valid combinations of the following:

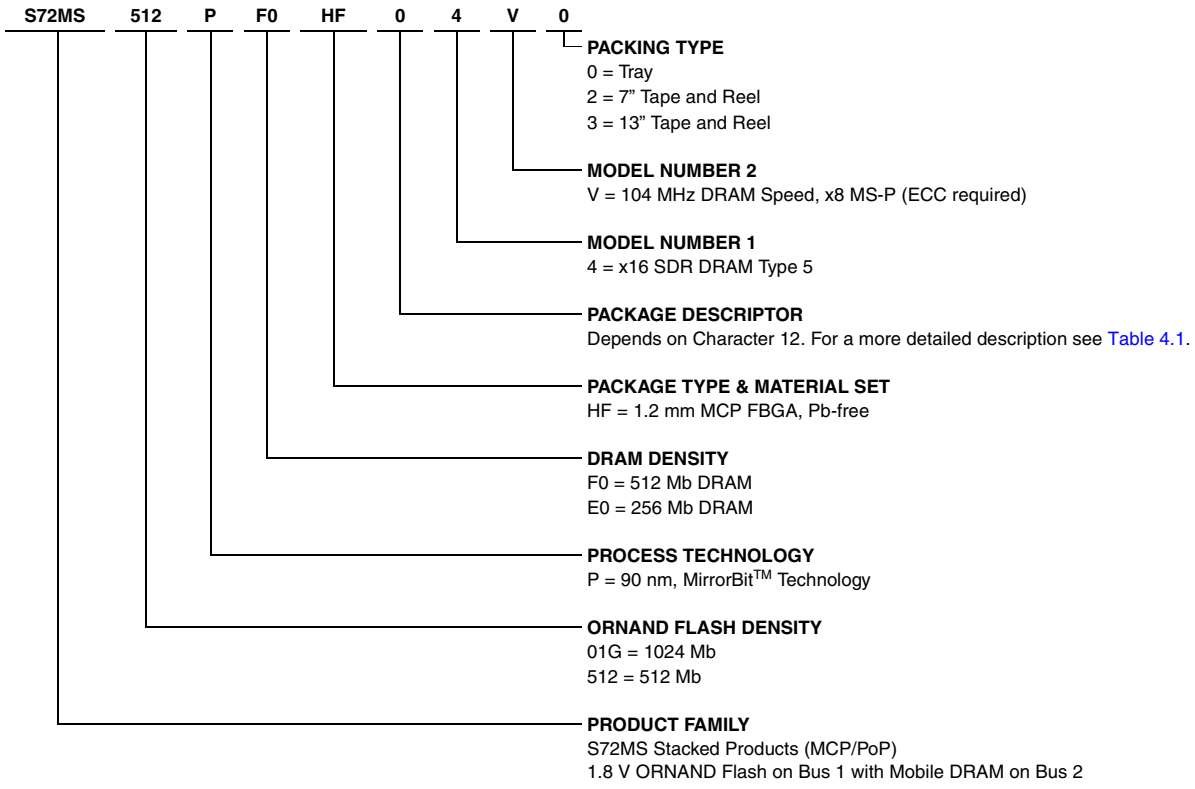


Table 4.1 Character Position Descriptions (Sheet 1 of 2)

Character 12	Character 13	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
H, J, or G	0	7x9 mm	56	0.35 mm
	1	7x9 mm	80	
	2	8x11.6 mm	64	
	3	8x11.6 mm	84	
	4	9x12 mm	84	
	5	9x12 mm	115	
	6	9x12 mm	137	
	7	11x13 mm	84	
	8	11x13 mm	115	
	9	11x13 mm	137	

Table 4.1 Character Position Descriptions (Sheet 2 of 2)

Character 12	Character 13	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
K	A	11x11 mm	112	0.45 mm
	B	11x11 mm	112	0.50 mm
	D	12x12 mm	128	0.45 mm
	F	12x12 mm	128	0.50 mm
	G	14x14 mm	152	0.45 mm
	H	14x14 mm	152	0.50 mm
	J	15x15 mm	160	0.45 mm
	K	15x15 mm	160	0.50 mm
	L	17x17 mm	192	0.45 mm
	M	17x17 mm	192	0.50 mm

4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

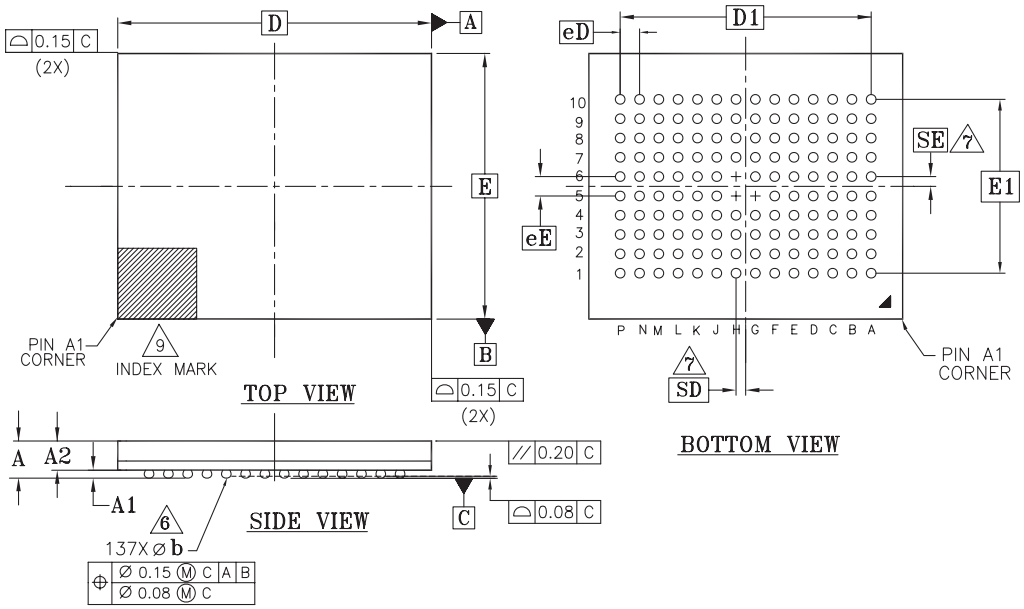
S72MS-P Valid Combinations				ORNAND Flash Bus Width	DRAM Supplier	DRAM Speed	Package Type	Package Markings
Base Ordering Number	Package & Material Set	Package Descriptor	Packing Type					
S72MS512PE0	HF	9	0, 2, 3 (Note 1)	x8 (ECC)	Type 5	104 MHz	11x13 mm (MCP)	(Note 2)

Notes:

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading* S *and packing type designator from ordering part number.*

5. Physical Dimensions

5.1 TLK137—137-ball Fine-Pitch Ball Grid Array (FBGA) 13 x 11 mm Package



PACKAGE	TLK 137			
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.79	---	0.96	BODY THICKNESS
D		13.00 BSC.		BODY SIZE
E		11.00 BSC.		BODY SIZE
D1		10.40 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		14		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		137		BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD SE		0.40 BSC.		SOLDER BALL PLACEMENT
		G5,H5,H6		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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6. Revision History

6.1 Revision 01 (September 14, 2006)

Initial release.

Colophon

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