Freescale Semiconductor
Technical Data

Document Number: MPC8323EEC
Rev. 3, 02/2010

MPC8323E PowerQUICC™ II Pro Integrated Communications Processor Family Hardware Specifications

This document provides an overview of the MPC8323E PowerQUICC™ II Pro processor features. The MPC8323E is a cost-effective, highly integrated communications processor that addresses the requirements of several networking applications, including ADSL SOHO and residential gateways, modem/routers, industrial control, and test and measurement applications. The MPC8323E extends current PowerQUICC offerings, adding higher CPU performance, additional functionality, and faster interfaces, while addressing the requirements related to time-to-market, price, power consumption, and board real estate. This document describes the MPC8323E, and unless otherwise noted, the information also applies to the MPC8323, MPC8321E, and MPC8321.

To locate published errata or updates for this document, refer to the MPC8323E product summary page on our website listed on the back cover of this document or contact your local Freescale sales office.

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1 Overview

The MPC8323E incorporates the e300c2 (MPC603e-based) core built on Power Architecture™ technology, which includes 16 Kbytes of L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The e300c2 core does not contain a floating point unit (FPU). The MPC8323E also includes a 32-bit PCI controller, four DMA channels, a security engine, and a 32-bit DDR1/DDR2 memory controller.

A new communications complex based on QUICC Engine™ technology forms the heart of the networking capability of the MPC8323E. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). Note that the MPC8321 and MPC8321E do not support UTOPIA. A block diagram of the MPC8323E is shown in Figure 1.

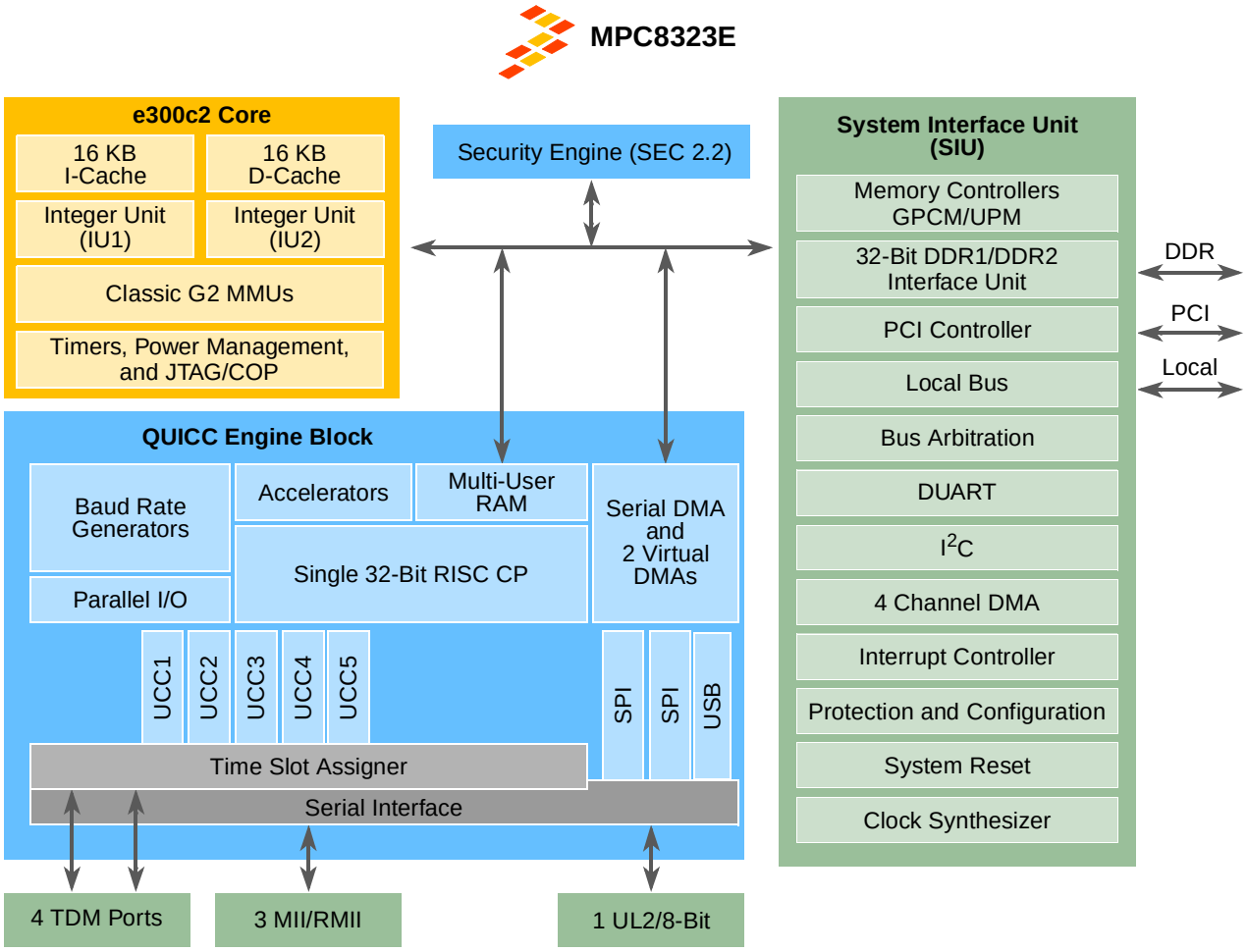


Figure 1. MPC8323E Block Diagram

Each of the five UCCs can support a variety of communication protocols: 10/100 Mbps Ethernet, serial ATM, HDLC, UART, and BISYNC—and, in the MPC8323E and MPC8323, multi-PHY ATM and ATM support for up to OC-3 speeds.

NOTE

The QUICC Engine block can also support a UTOPIA level 2 capable of supporting 31 multi-PHY (MPC8323E- and MPC8323-specific).

The MPC8323E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

1.1 MPC8323E Features

Major features of the MPC8323E are as follows:

- High-performance, low-power, and cost-effective single-chip data-plane/control-plane solution for ATM or IP/Ethernet packet processing (or both).
- MPC8323E QUICC Engine block offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards.
- Single platform architecture supports the convergence of IP packet networks and ATM networks.
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR1 and DDR2.
- An e300c2 core built on Power Architecture technology with 16-Kbyte instruction and data caches, and dual integer units.
- Peripheral interfaces such as 32-bit PCI (2.2) interface up to 66-MHz operation, 16-bit local bus interface up to 66-MHz operation, and USB 2.0 (full-/low-speed).
- Security engine provides acceleration for control and data plane security protocols.
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration.

1.1.1 Protocols

The protocols are as follows:

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- Support for 64 channels of HDLC/transparent

1.1.2 Serial Interfaces

The MPC8323E serial interfaces are as follows:

- Support for one UL2 interface with 31 multi-PHY addresses (MPC8323E and MPC8323 only)
- Support for up to three 10/100 Mbps Ethernet interfaces using MII or RMII
- Support for up to four T1/E1/J1/E3 or DS-3 serial interfaces (TDM)
- Support for dual UART and SPI interfaces and a single I^2C interface

1.2 QUICC Engine Block

The QUICC Engine block is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine block has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
  - 10/100 Mbps Ethernet/IEEE 802.3® standard
  - IP support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
  - ATM protocol through UTOPIA interface (note that the MPC8321 and MPC8321E do not support the UTOPIA interface)
  - HDLC /transparent up to 70-Mbps full-duplex
  - HDLC bus up to 10 Mbps
  - Asynchronous HDLC
  - UART
  - BISYNC up to 2 Mbps
  - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface (UPC1) supporting 31 multi-PHYs (MPC8323E- and MPC8323-specific)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- Thirteen independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus) and FCC (fast Ethernet, HDLC, transparent, and ATM).

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i® standard, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8323E DDR1/DDR2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266-MHz data rate
- Support for two ×16 devices
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 1 chip select only
- FCRAM, ECC, hardware/software calibration, bit deskew, QIN stage, or atomic logic are not supported.

1.5 PCI Controller

The MPC8323E PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8323E. The MPC8323E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DDn}	–0.3 to 1.26	V	—
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I^2C, SPI, MII, RMII, MII management, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.6	V	—
Input voltage	DDR1/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2
	DDR1/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2
	Local bus, DUART, CLKIN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

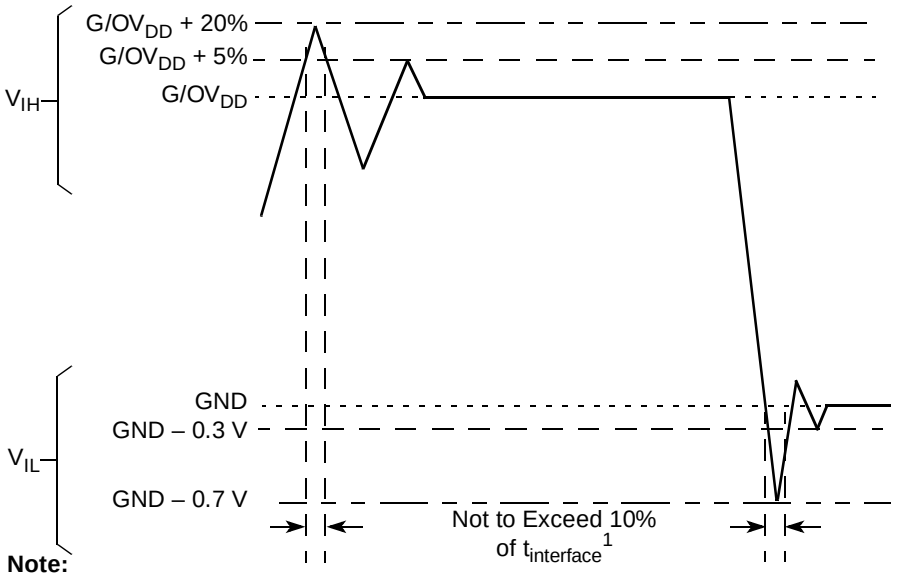
Table 2 provides the recommended operating conditions for the MPC8323E. Note that these values are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	1
PLL supply voltage	AV_{DD}	1.0 V ± 50 mV	V	1
DDR1 and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage	OV_{DD}	3.3 V ± 300 mV	V	1
Junction temperature	T_A/T_J	0 to 105	°C	2

Note:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Minimum temperature is specified with T_A; maximum temperature is specified with T_J.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8323E



Note:
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV_{DD} = 3.3 V
PCI signals	25	
DDR1 signal	18	GV_{DD} = 2.5 V
DDR2 signal	18	GV_{DD} = 1.8 V
DUART, system control, I2C, SPI, JTAG	42	OV_{DD} = 3.3 V
GPIO signals	42	OV_{DD} = 3.3 V

2.1.4 Input Capacitance Specification

Table 4 describes the input capacitance for the CLKIN pin in the MPC8323E.

Table 4. Input Capacitance Specification

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input capacitance for all pins except CLKIN	C_I	6	8	pF	—
Input capacitance for CLKIN	C_{ICLKIN}	10	—	pF	1

Note:
1. The external clock generator should be able to drive 10 pF.

2.2 Power Sequencing

The device does not require the core supply voltage (V_{DD}) and IO supply voltages (GV_{DD} and OV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

Note that there is no specific power down sequence requirement for the device. I/O voltage supplies (GV_{DD} and OV_{DD}) do not have any ordering requirements with respect to one another.

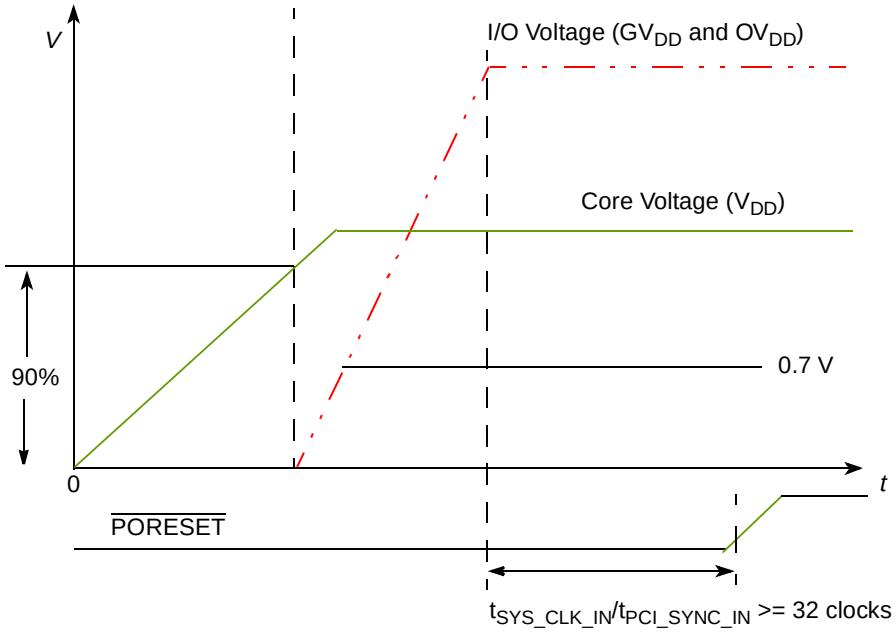


Figure 3. MPC8323E Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation for this family of MPC8323E devices is shown in Table 5.

Table 5. MPC8323E Power Dissipation

CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Core Frequency (MHz)	Typical	Maximum	Unit	Notes
133	200	266	0.74	1.48	W	1, 2, 3
133	200	333	0.78	1.62	W	1, 2, 3

Notes:
1. The values do not include I/O supply power (OV_{DD} and GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a nominal voltage of V_{DD} = 1.0 V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the MPC8323MDS evaluation board using WC process silicon.
3. Maximum power is based on a voltage of V_{DD} = 1.07 V, WC process, a junction T_J = 110°C, and an artificial smoke test.

Table 6 shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V R_s = 20 Ω R_t = 50 Ω 1 pair of clocks	266 MHz, 1 × 32 bits	0.212	0.367	—	W	—

Table 6. Estimated Typical I/O Power Dissipation (continued)

Local bus I/O load = 25 pF 1 pair of clocks	66 MHz, 32 bits	—	—	0.12	W	—
PCI I/O load = 30 pF	66 MHz, 32 bits	—	—	0.057	W	—
QUICC Engine block and other I/Os	UTOPIA 8-bit 31 PHYs	—	—	0.041	W	Mutiply by number of interfaces used.
	TDM serial	—	—	0.001	W	
	TDM nibble	—	—	0.004	W	
	HDLC/TRAN serial	—	—	0.003	W	
	HDLC/TRAN nibble	—	—	0.025	W	
	DUART	—	—	0.017	W	
	MIIs	—	—	0.009	W	
	RMII	—	—	0.009	W	
	Ethernet management	—	—	0.002	W	
	USB	—	—	0.001	W	
	SPI	—	—	0.001	W	
	Timer output	—	—	0.002	W	

NOTE

$AV_{DD}n$ (1.0 V) is estimated to consume 0.05 W (under normal operating conditions and ambient temperature).

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8323E.

NOTE

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of VCC; fall time refers to transitions from 90% to 10% of VCC.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8323E.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V

Table 7. CLKIN DC Electrical Characteristics (continued)

CLKIN input current	$0 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±5	μA
PCI_SYNC_IN input current	$0 V \le V_{IN} \le 0.5 V$ or $OV_{DD} – 0.5 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±5	μA
PCI_SYNC_IN input current	$0.5 V \le V_{IN} \le OV_{DD} – 0.5 V$	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 8 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8323E.

Table 8. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN rise and fall time	t_{KH}, t_{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core, security, and QUICC Engine block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

5 RESET Initialization

This section describes the AC electrical specifications for the reset initialization timing requirements of the MPC8323E. Table 9 provides the reset initialization AC timing specifications for the reset component(s).

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI_SYNC_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8323E is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8323E is in PCI agent mode	32	—	$t_{PCI_SYNC_IN}$	1

Table 9. RESET Initialization Timing Specifications (continued)

HRESET/SRESET assertion (output)	512	—	$t_{PCI_SYNC_IN}$	1
HRESET negation to SRESET negation (output)	16	—	$t_{PCI_SYNC_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8323E is in PCI agent mode	4	—	$t_{PCI_SYNC_IN}$	1
Input hold time for POR config signals with respect to negation of HRESET	0	—	ns	—
Time for the MPC8323E to turn off POR configuration signals with respect to the assertion of HRESET	—	4	ns	3
Time for the MPC8323E to turn on POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI_SYNC_IN}$	1, 3

Notes:

1. $t_{PCI_SYNC_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the MPC8323E is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8323E PowerQUICC™ II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the MPC8323E is in PCI host mode. See the *MPC8323E PowerQUICC™ II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

5.1 Reset Signals DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	µA	—

Note:

1. This specification applies when operating from 3.3 V supply.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR1 and DDR2 SDRAM interface of the MPC8323E. Note that DDR1 SDRAM is D*n*_GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is D*n*_GV_{DD}(typ) = 1.8 V. The AC electrical specifications are the same for DDR1 and DDR2 SDRAM.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8323E when D*n*_GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MVREF*n*$_{REF}$	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	MVREF*n*$_{REF}$ – 0.04	MVREF*n*$_{REF}$ + 0.04	V	3
Input high voltage	V_{IH}	MVREF*n*$_{REF}$ + 0.125	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF*n*$_{REF}$ – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	µA	4
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. MVREF*n*$_{REF}$ is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n*$_{REF}$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF*n*$_{REF}$. This rail should track variations in the DC level of MVREF*n*$_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 13 provides the DDR2 capacitance when D*n*_GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25 °C, V_{OUT} = D*n*_GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR1 SDRAM component(s) of the MPC8323E when D*n*_GV_{DD}(typ) = 2.5 V.

Table 14. DDR1 SDRAM DC Electrical Characteristics for D*n*_GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MVREF*n*$_{REF}$	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	MVREF*n*$_{REF}$ – 0.04	MVREF*n*$_{REF}$ + 0.04	V	3
Input high voltage	V_{IH}	MVREF*n*$_{REF}$ + 0.15	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF*n*$_{REF}$ – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	µA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. MVREF*n*$_{REF}$ is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n*$_{REF}$ may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF*n*$_{REF}$. This rail should track variations in the DC level of MVREF*n*$_{REF}$.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 15 provides the DDR1 capacitance D*n*_GV_{DD}(typ) = 2.5 V.

Table 15. DDR1 SDRAM Capacitance for D*n*_GV_{DD}(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = D*n*_GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR1 and DDR2 SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

Table 16 provides the input AC timing specifications for the DDR2 SDRAM (D*n*_GV_{DD}(typ) = 1.8 V).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with D*n*_GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MVREFn_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MVREFn_{REF} + 0.25	—	V	—

Table 17 provides the input AC timing specifications for the DDR1 SDRAM (D*n*_GV_{DD}(typ) = 2.5 V).

Table 17. DDR1 SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with D*n*_GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MVREFn_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MVREFn_{REF} + 0.31	—	V	—

Table 18 provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 18. DDR1 and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with D*n*_GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MDM 266 MHz 200 MHz	t_{CISKEW}	 –750 –1250	 750 1250	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

Figure 4 shows the input timing diagram for the DDR controller.

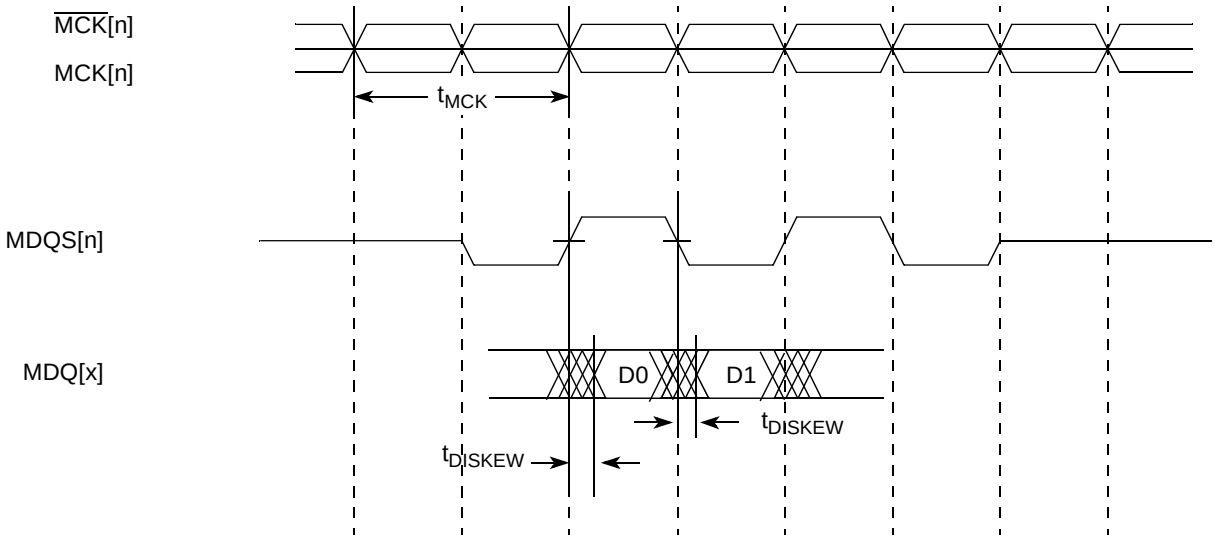


Figure 4. DDR Input Timing Diagram

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

Table 19 provides the output AC timing specifications for the DDR1 and DDR2 SDRAM interfaces.

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with D*n*_GV$_{DD}$ of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK cycle time, (MCK/$\overline{\text{MCK}}$ crossing)	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.5 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 2.5 3.5	 — —	ns	3
$\overline{\text{MCS}}$ output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 2.5 3.5	 — —	ns	3
$\overline{\text{MCS}}$ output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 2.5 3.5	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4

Table 19. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with D*n*_GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 0.9 1.0	 — —	ns	5
MDQ/MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8323E PowerQUICC™ II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

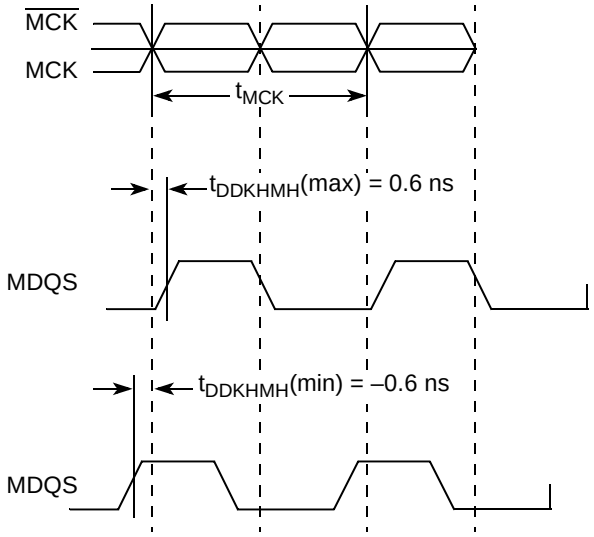


Figure 5. Timing Diagram for t_{DDKHMH}

Figure 6 shows the DDR1 and DDR2 SDRAM output timing diagram.

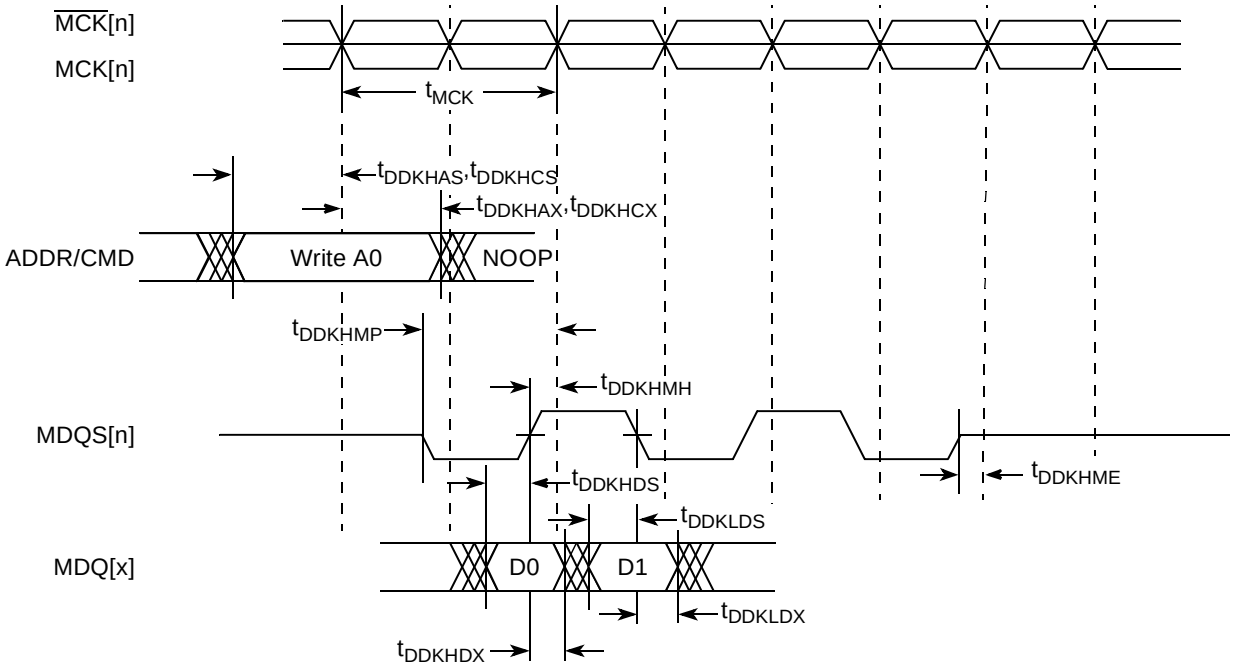


Figure 6. DDR1 and DDR2 SDRAM Output Timing Diagram

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8323E.

7.1 DUART DC Electrical Characteristics

Table 20 provides the DC electrical characteristics for the DUART interface of the MPC8323E.

Table 20. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 21 provides the AC timing parameters for the DUART interface of the MPC8323E.

Table 21. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet and MII Management

This section provides the AC and DC electrical characteristics for Ethernet and MII management.

8.1 Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics

The electrical characteristics specified here apply to all MII (media independent interface) and RMII (reduced media independent interface), except MDIO (management data input/output) and MDC

(management data clock). The MII and RMII are defined for 3.3 V. The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 DC Electrical Characteristics

All MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 22. The potential applied to the input of a MII or RMII receiver may exceed the potential of the receiver's power supply (that is, a MII driver powered from a 3.6-V supply driving V_{OH} into a MII receiver powered from a 2.5-V supply). Tolerance for dissimilar MII driver and receiver supply potentials is implicit in these specifications.

Table 22. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	OV_{DD} = Min	2.40	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.2 MII and RMII AC Timing Specifications

The AC timing specifications for MII and RMII are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns

Table 23. MII Transmit AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 7 shows the MII transmit AC timing diagram.

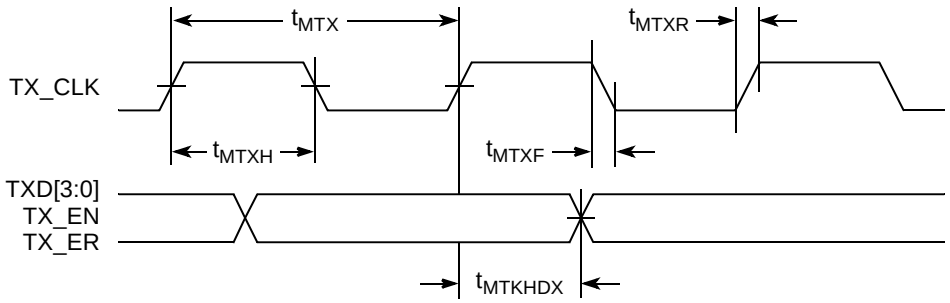


Figure 7. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns

Table 24. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 8 provides the AC test load.

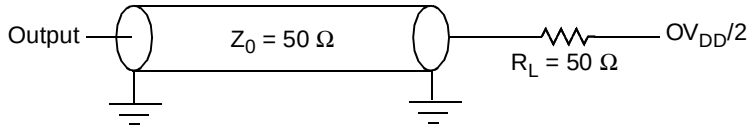


Figure 8. AC Test Load

Figure 9 shows the MII receive AC timing diagram.

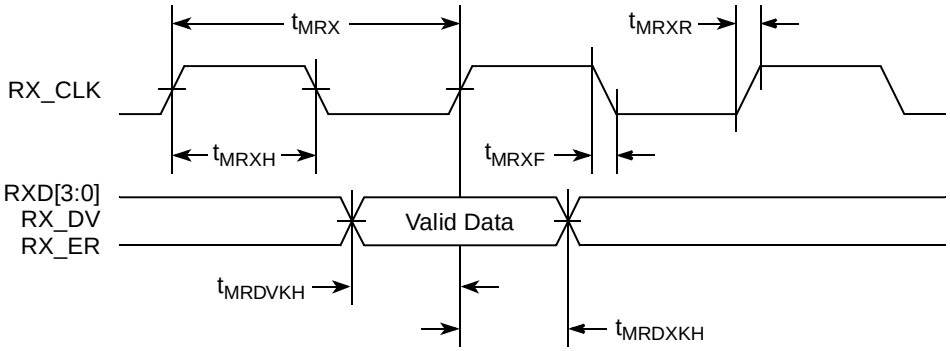


Figure 9. MII Receive AC Timing Diagram

8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.2.1 RMII Transmit AC Timing Specifications

Table 23 provides the RMII transmit AC timing specifications.

Table 25. RMII Transmit AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the RMII transmit AC timing diagram.

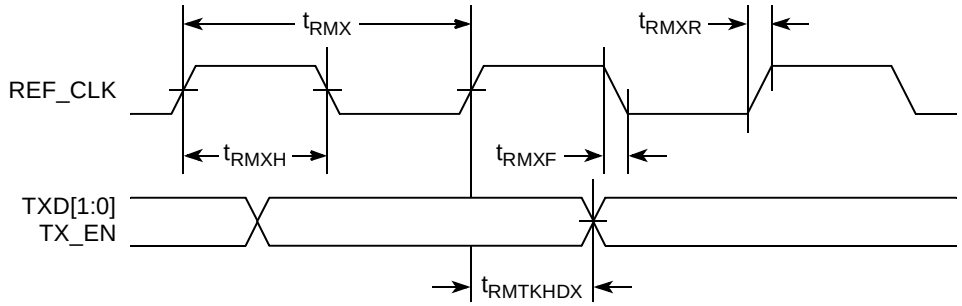


Figure 10. RMII Transmit AC Timing Diagram

8.2.2.2 RMII Receive AC Timing Specifications

Table 24 provides the RMII receive AC timing specifications.

Table 26. RMII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns

Table 26. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load.

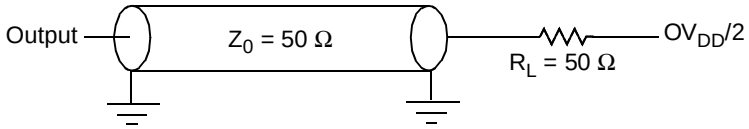


Figure 11. AC Test Load

Figure 12 shows the RMII receive AC timing diagram.

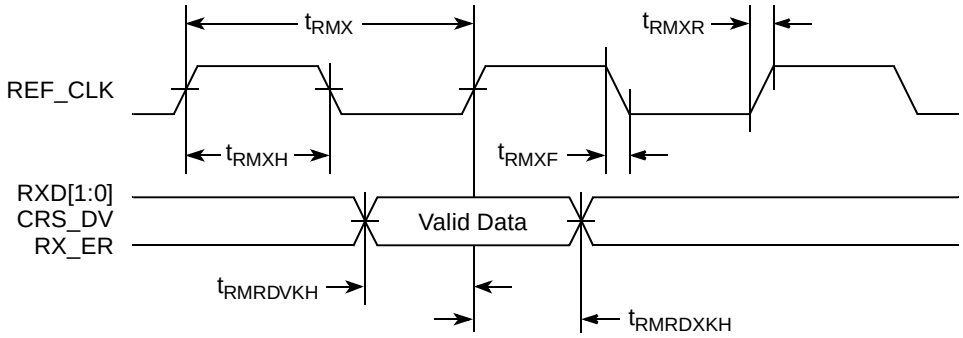


Figure 12. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, and RMII are specified in Section 8.1, “Ethernet Controller (10/100 Mbps)—MII/RMII Electrical Characteristics.”

8.3.1 MII Management DC Electrical Characteristics

MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 27.

Table 27. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	OV_{DD} = Min	2.10	OV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	OV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$		—	±5	μA

8.3.2 MII Management AC Electrical Specifications

Table 28 provides the MII management AC timing specifications.

Table 28. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	—
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	—
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 13 shows the MII management AC timing diagram.

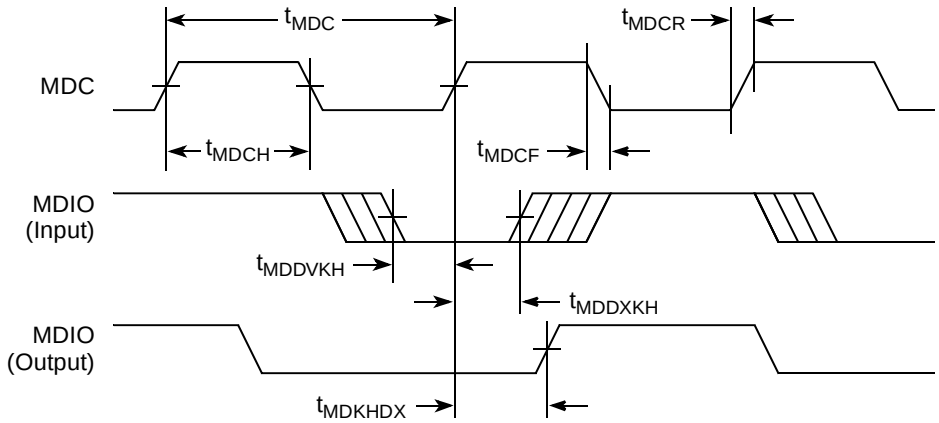


Figure 13. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8323E.

9.1 Local Bus DC Electrical Characteristics

Table 29 provides the DC electrical characteristics for the local bus interface.

Table 29. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	µA

9.2 Local Bus AC Electrical Specifications

Table 30 describes the general timing parameters of the local bus interface of the MPC8323E.

Table 30. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock (LCLK*n*)	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock (LCLK*n*)	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5

Table 30. Local Bus General Timing Parameters (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock (LCLK*n*) to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock (LCLK*n*) to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8
Local bus clock (LCLK*n*) duty cycle	t_{LBDC}	47	53	%	—
Local bus clock (LCLK*n*) jitter specification	t_{LBRJ}	—	400	ps	—
Delay between the input clock (PCI_SYNC_IN) of local bus output clock (LCLK*n*)	t_{LBCDL}	—	1.7	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 14 provides the AC test load for the local bus.

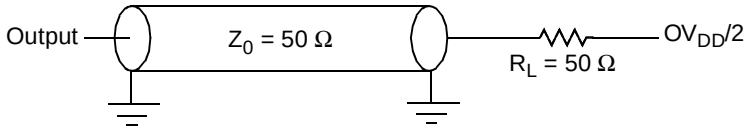


Figure 14. Local Bus C Test Load

Figure 15 through Figure 17 show the local bus signals.

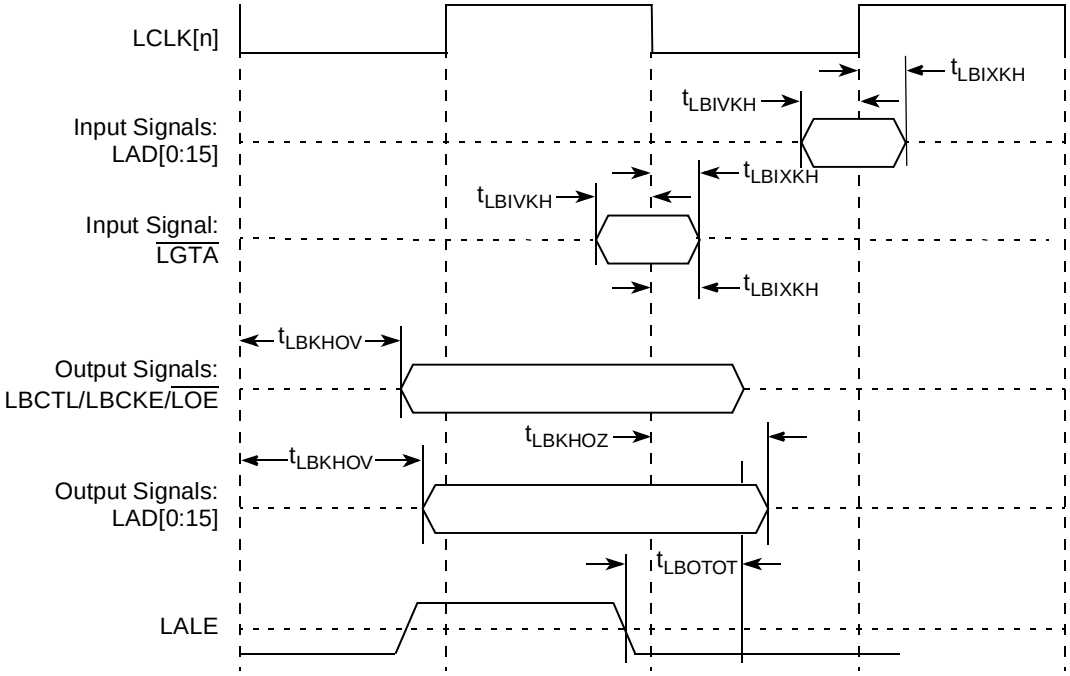


Figure 15. Local Bus Signals, Nonspecial Signals Only

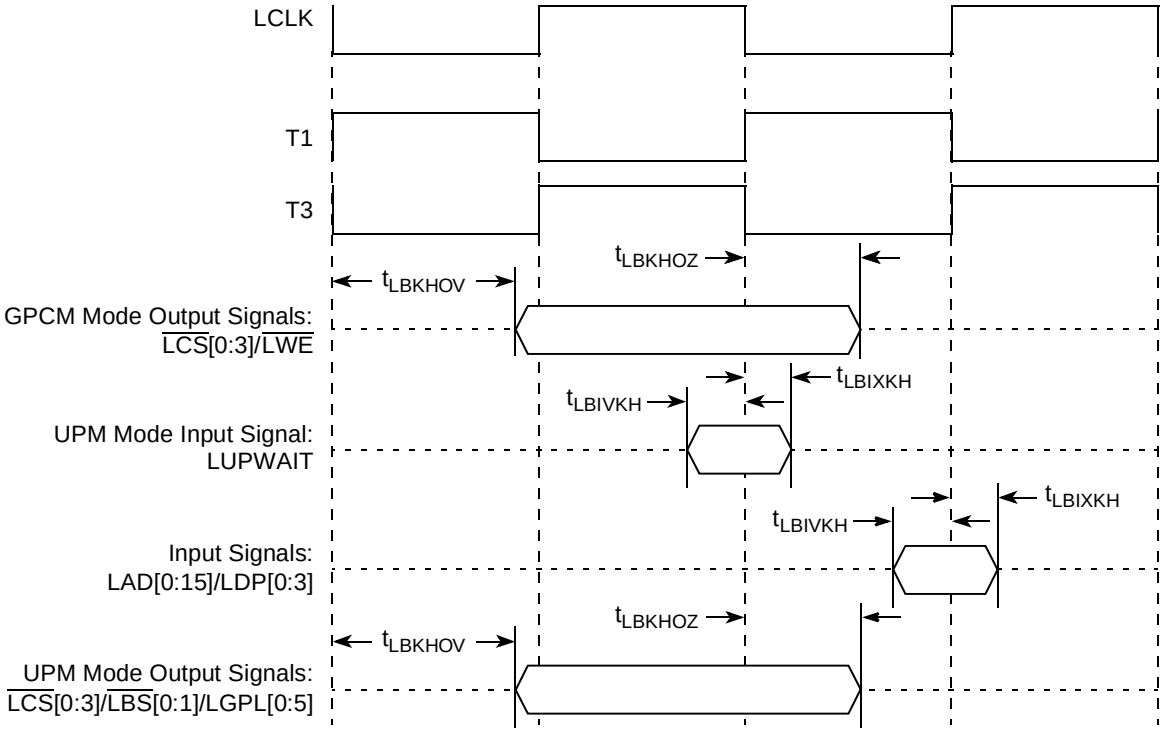


Figure 16. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2

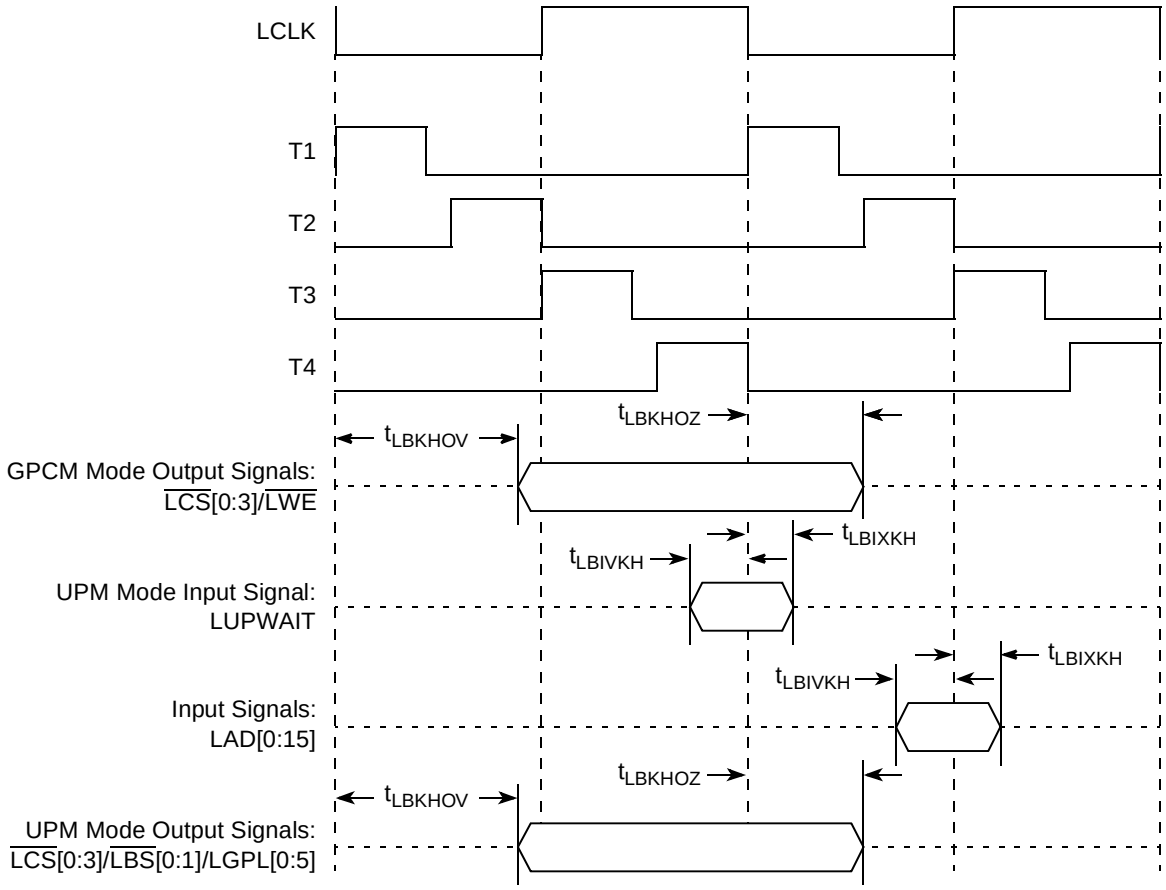


Figure 17. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8323E.

10.1 JTAG DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E.

Table 31. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V

Table 31. JTAG Interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8323E. Table 32 provides the JTAG AC timing specifications as defined in Figure 19 through Figure 22.

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 15 15	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5

Table 32. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 14). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the MPC8323E.

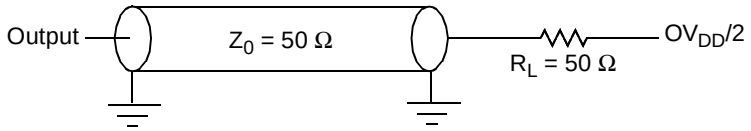


Figure 18. AC Test Load for the JTAG Interface

Figure 19 provides the JTAG clock input timing diagram.

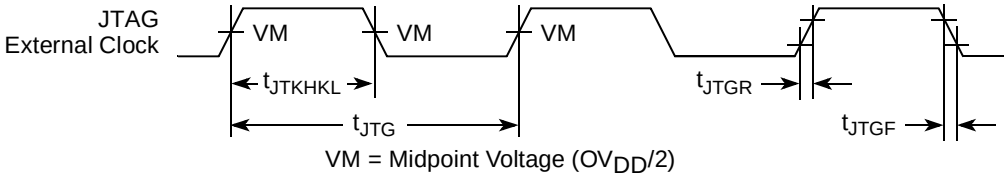


Figure 19. JTAG Clock Input Timing Diagram

Figure 20 provides the $\overline{\text{TRST}}$ timing diagram.

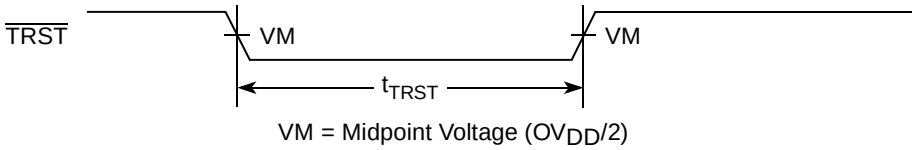


Figure 20. $\overline{\text{TRST}}$ Timing Diagram

Figure 21 provides the boundary-scan timing diagram.

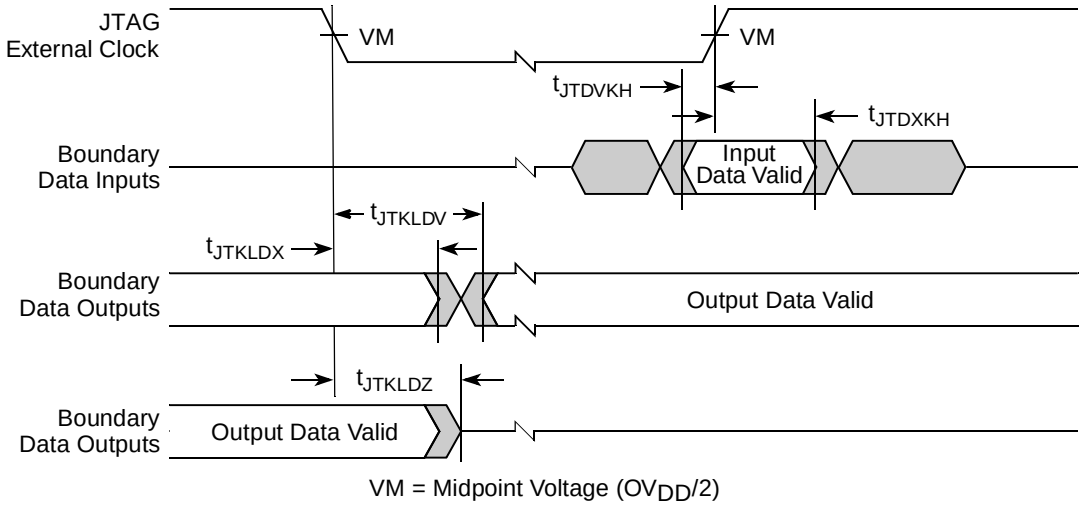


Figure 21. Boundary-Scan Timing Diagram

Figure 22 provides the test access port timing diagram.

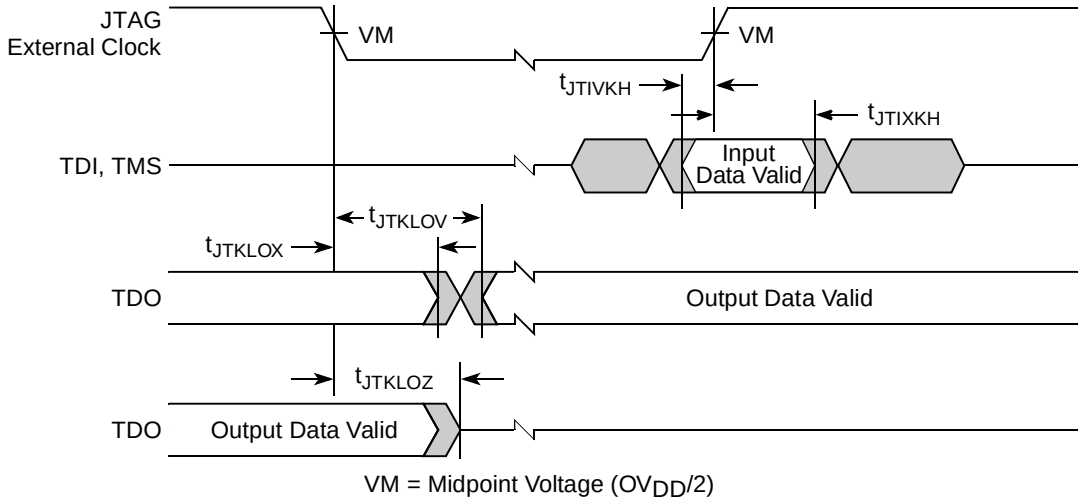


Figure 22. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8323E.

11.1 I²C DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the I²C interface of the MPC8323E.

Table 33. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8323E PowerQUICC™ II Pro Integrated Communications Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 34 provides the AC timing parameters for the I²C interface of the MPC8323E.

Table 34. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	μs

Table 34. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 33).

Parameter	Symbol[1]	Min	Max	Unit
Rise time of both SDA and SCL signals	t_{I2CR}	20 + 0.1 C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	20 + 0.1 C_b[4]	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8323E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

Figure 23 provides the AC test load for the I²C.

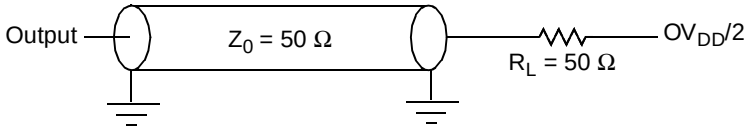


Figure 23. I²C AC Test Load

Figure 24 shows the AC timing diagram for the I²C bus.

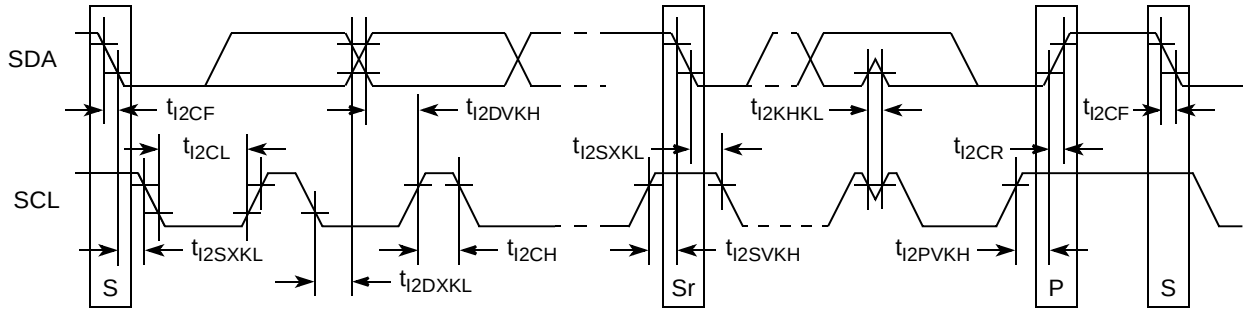


Figure 24. I²C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8323E.

12.1 PCI DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the PCI interface of the MPC8323E.

Table 35. PCI DC Electrical Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.3	0.8	V
High-level output voltage	V_{OH}	OV_{DD} = min, I_{OH} = –100 µA	OV_{DD} – 0.2	—	V
Low-level output voltage	V_{OL}	OV_{DD} = min, I_{OL} = 100 µA	—	0.2	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	µA

Notes:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.
2. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.3 Local Bus Specifications.*

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8323E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8323E is configured as a host or agent device. Table 36 shows the PCI AC timing specifications at 66 MHz.

Table 36. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedence	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Table 37 shows the PCI AC timing specifications at 33 MHz.

Table 37. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedence	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 25 provides the AC test load for PCI.

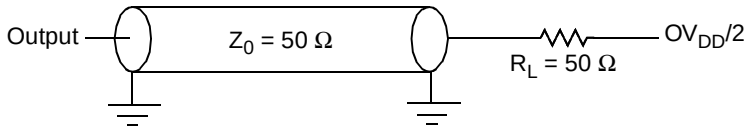


Figure 25. PCI AC Test Load

Figure 26 shows the PCI input AC timing conditions.

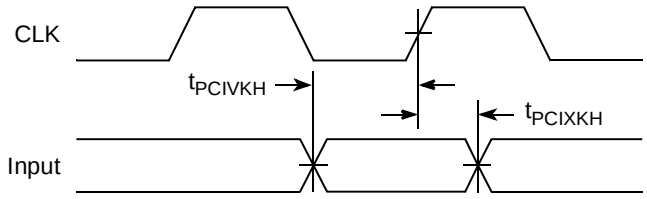


Figure 26. PCI Input AC Timing Measurement Conditions

Figure 27 shows the PCI output AC timing conditions.

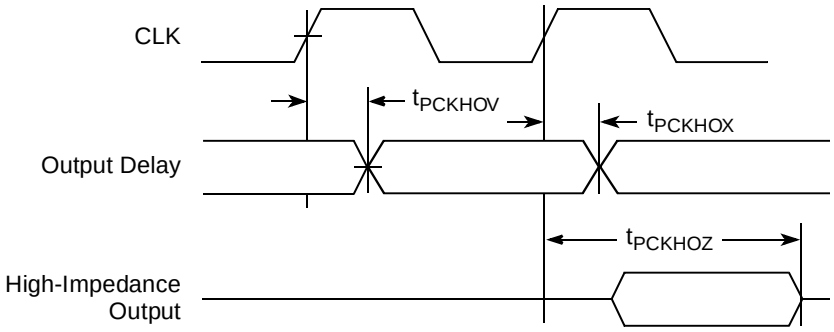


Figure 27. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8323E.

13.1 Timer DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the MPC8323E timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 38. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

13.2 Timer AC Timing Specifications

Table 39 provides the timer input and output AC timing specifications.

Table 39. Timer Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Figure 28 provides the AC test load for the timers.

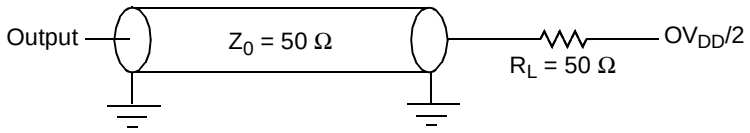


Figure 28. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8323E.

14.1 GPIO DC Electrical Characteristics

Table 11 provides the DC electrical characteristics for the MPC8323E GPIO.

Table 40. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

Table 41 provides the GPIO input and output AC timing specifications.

Table 41. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 29 provides the AC test load for the GPIO.

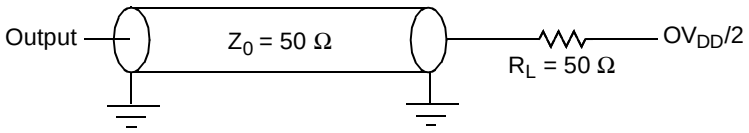


Figure 29. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8323E.

15.1 IPIC DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the external interrupt pins of the MPC8323E.

Table 42. IPIC DC Electrical Characteristics[1,2]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	µA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ_OUT}}$, $\overline{\text{MCP_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ_OUT}}$ and $\overline{\text{MCP_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

15.2 IPIC AC Timing Specifications

Table 43 provides the IPIC input and output AC timing specifications.

Table 43. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8323E.

16.1 SPI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the MPC8323E SPI.

Table 44. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

16.2 SPI AC Timing Specifications

Table 45 and provide the SPI input and output AC timing specifications.

Table 45. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 30 provides the AC test load for the SPI.

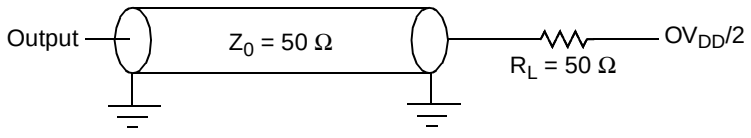
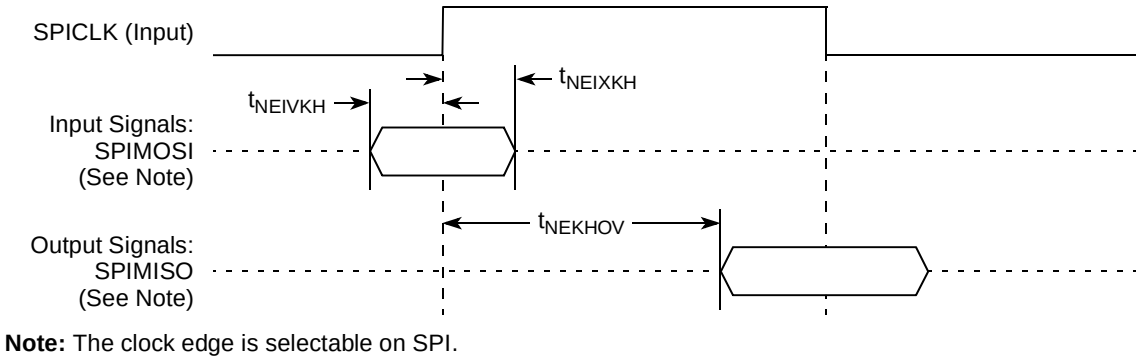


Figure 30. SPI AC Test Load

Figure 31 and Figure 32 represent the AC timing from Table 45. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

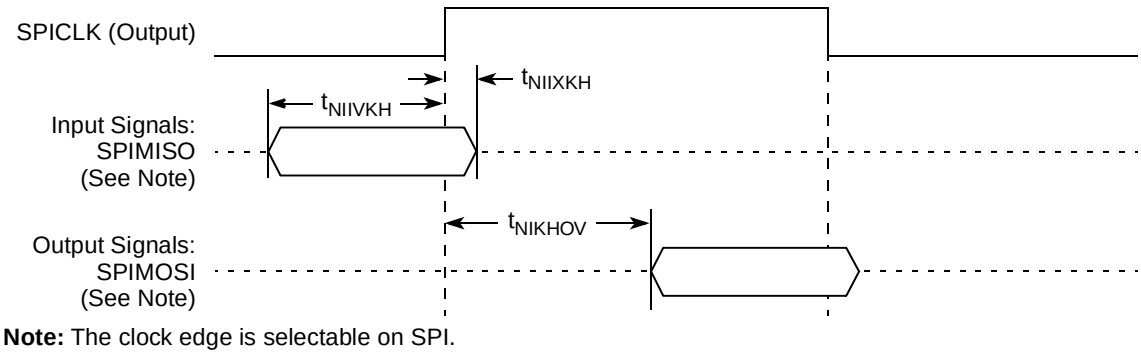
Figure 31 shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 31. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 32 shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 32. SPI AC Timing in Master Mode (Internal Clock) Diagram

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8323E.

17.1 TDM/SI DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the MPC8323E TDM/SI.

Table 46. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V

Table 46. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

17.2 TDM/SI AC Timing Specifications

Table 47 provides the TDM/SI input and output AC timing specifications.

Table 47. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	12	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 33 provides the AC test load for the TDM/SI.

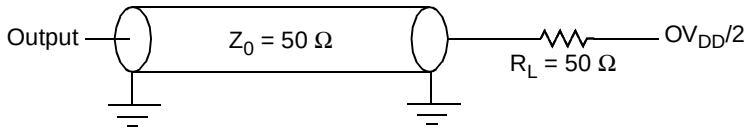
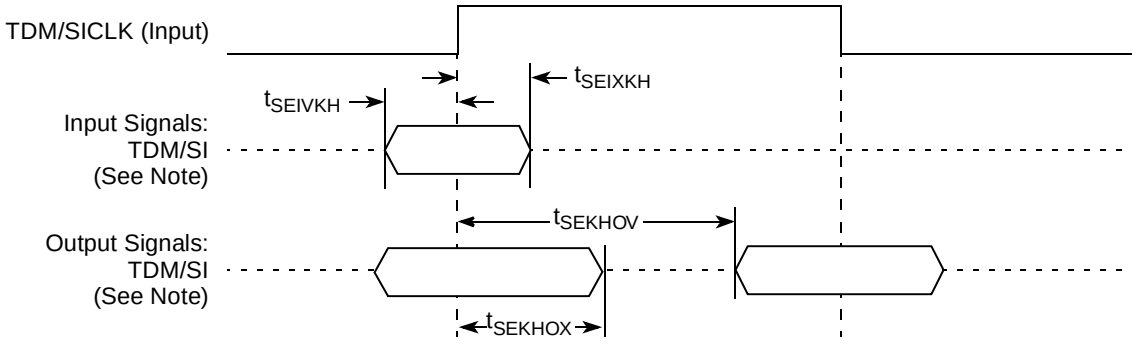


Figure 33. TDM/SI AC Test Load

Figure 34 represents the AC timing from Table 47. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.



Note: The clock edge is selectable on TDM/SI.

Figure 34. TDM/SI AC Timing (External Clock) Diagram

18 UTOPIA

This section describes the UTOPIA DC and AC electrical specifications of the MPC8323E.

NOTE

The MPC8321E and MPC8321 do not support UTOPIA.

18.1 UTOPIA DC Electrical Characteristics

Table 48 provides the DC electrical characteristics for the MPC8323E UTOPIA.

Table 48. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

18.2 UTOPIA AC Timing Specifications

Table 49 provides the UTOPIA input and output AC timing specifications.

Table 49. UTOPIA AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
UTOPIA outputs—Internal clock delay	t_{UIKHOV}	0	5.5	ns
UTOPIA outputs—External clock delay	t_{UEKHOV}	1	8	ns
UTOPIA outputs—Internal clock high impedance	t_{UIKHOX}	0	5.5	ns
UTOPIA outputs—External clock high impedance	t_{UEKHOX}	1	8	ns
UTOPIA inputs—Internal clock input setup time	t_{UIIVKH}	8	—	ns
UTOPIA inputs—External clock input setup time	t_{UEIVKH}	4	—	ns
UTOPIA inputs—Internal clock input hold time	t_{UIIXKH}	0	—	ns
UTOPIA inputs—External clock input hold time	t_{UEIXKH}	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 35 provides the AC test load for the UTOPIA.

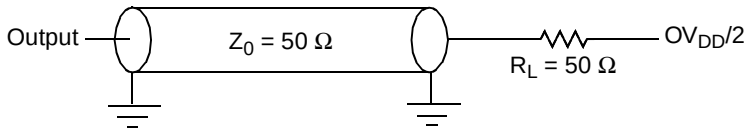


Figure 35. UTOPIA AC Test Load

Figure 36 and Figure 37 represent the AC timing from Table 49. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 36 shows the UTOPIA timing with external clock.

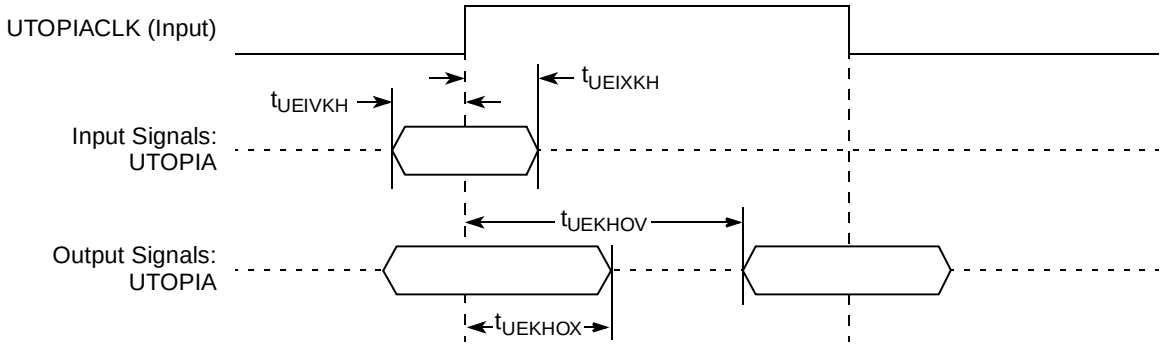


Figure 36. UTOPIA AC Timing (External Clock) Diagram

Figure 37 shows the UTOPIA timing with internal clock.

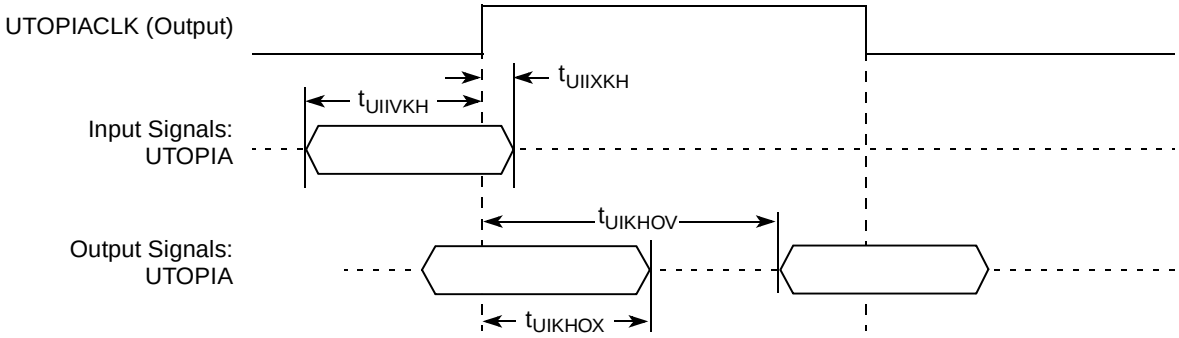


Figure 37. UTOPIA AC Timing (Internal Clock) Diagram

19 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART of the MPC8323E.

19.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the MPC8323E HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 50. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA

19.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Table 51 provides the input and output AC timing specifications for HDLC, BISYNC, and transparent UART protocols.

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	5.5	ns
Outputs—External clock delay	t_{HEKHOV}	1	10	ns
Outputs—Internal clock high impedance	t_{HIKHOX}	0	5.5	ns
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	0	—	ns

Table 51. HDLC, BISYNC, and Transparent UART AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 52. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	5.5	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	10	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	5.5	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	8	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	4	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	0	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{UAIKHOX}$ symbolizes the outputs internal timing (UAI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 38 provides the AC test load.

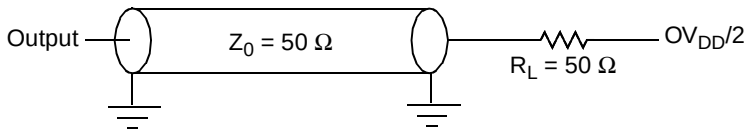
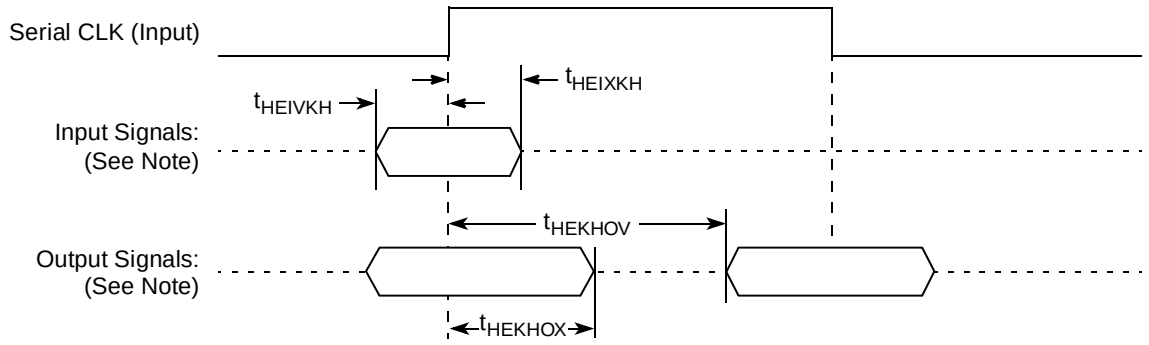


Figure 38. AC Test Load

Figure 39 and Figure 40 represent the AC timing from Table 51. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

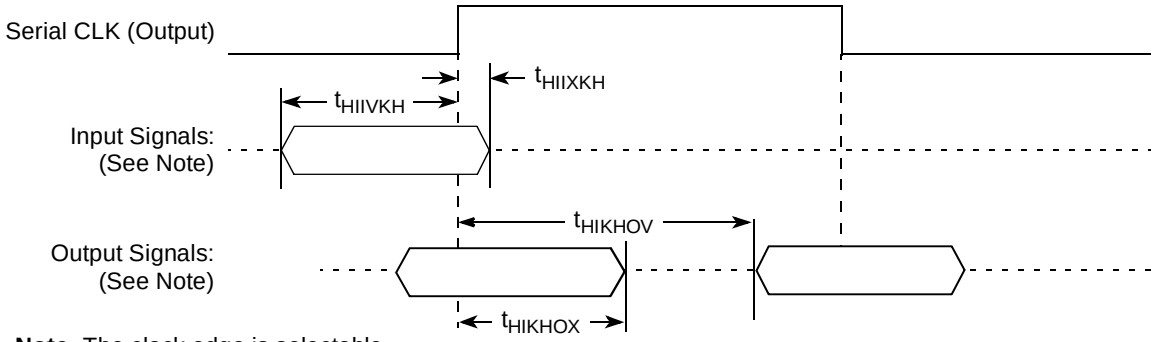
Figure 39 shows the timing with external clock.



Note: The clock edge is selectable.

Figure 39. AC Timing (External Clock) Diagram

Figure 40 shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 40. AC Timing (Internal Clock) Diagram

20 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8323E.

20.1 USB DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the USB interface.

Table 53. USB DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

20.2 USB AC Electrical Specifications

Table 54 describes the general timing parameters of the USB interface of the MPC8323E.

Table 54. USB General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	—
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full speed transitions
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low speed transitions

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

Figure 41 provide the AC test load for the USB.

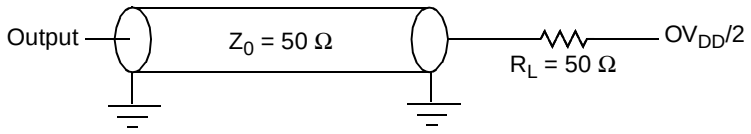


Figure 41. USB AC Test Load

21 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8323E is available in a thermally enhanced Plastic Ball Grid Array (PBGA); see Section 21.1, "Package Parameters for the MPC8323E PBGA," and Section 21.2, "Mechanical Dimensions of the MPC8323E PBGA," for information on the PBGA.

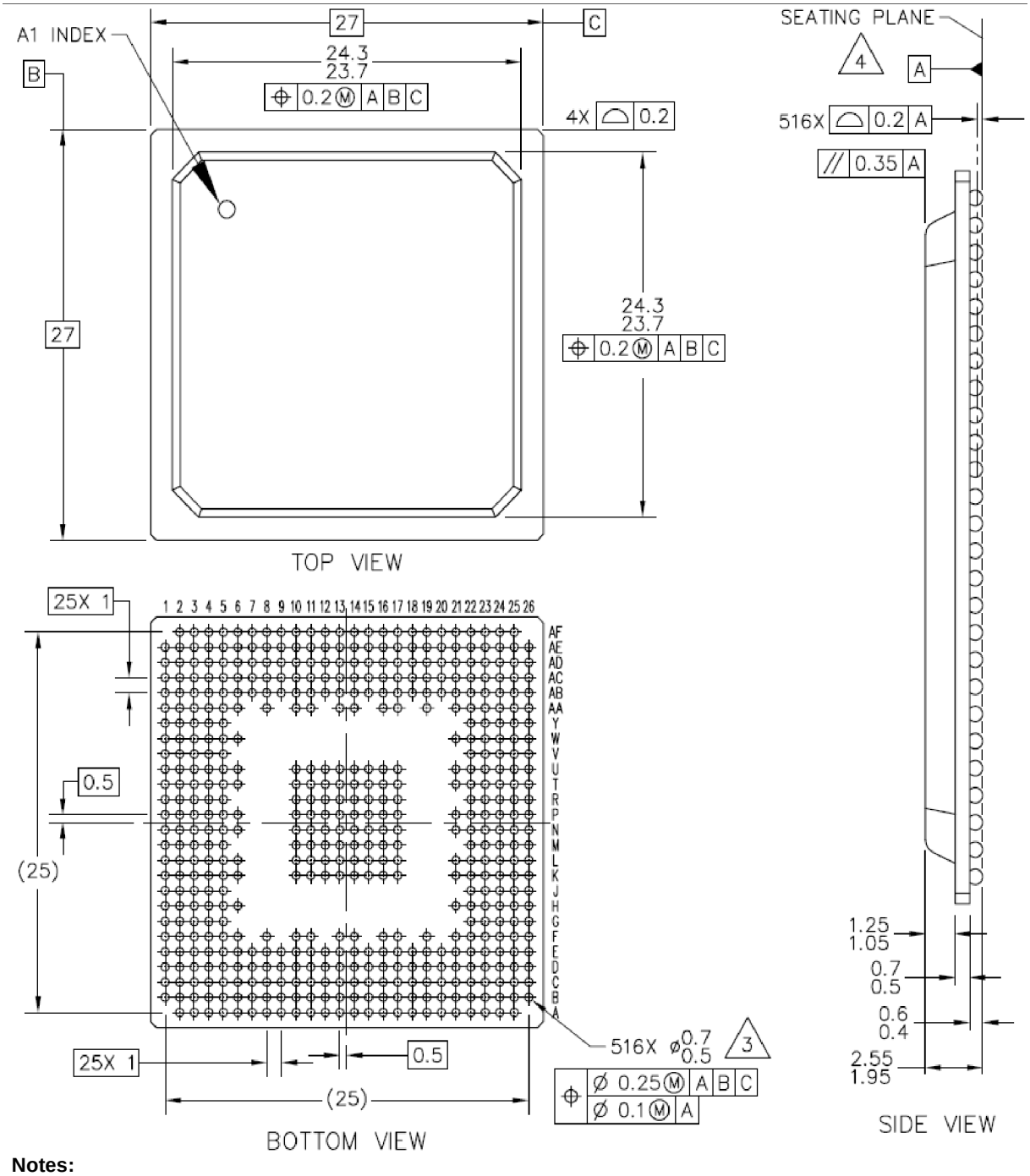
21.1 Package Parameters for the MPC8323E PBGA

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 PBGA.

Package outline	27 mm × 27 mm
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.6 mm

21.2 Mechanical Dimensions of the MPC8323E PBGA

Figure 42 shows the mechanical dimensions and bottom surface nomenclature of the MPC8323E, 516-PBGA package.



Notes:

1.All dimensions are in millimeters.

2.Dimensions and tolerances per ASME Y14.5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 42. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8323E PBGA

21.3 Pinout Listings

Table 55 shows the pin list of the MPC8323E.

Table 55. MPC8323E PBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Controller Interface				
MEMC_MDQ0	AE9	IO	GV_{DD}	—
MEMC_MDQ1	AD10	IO	GV_{DD}	—
MEMC_MDQ2	AF10	IO	GV_{DD}	—
MEMC_MDQ3	AF9	IO	GV_{DD}	—
MEMC_MDQ4	AF7	IO	GV_{DD}	—
MEMC_MDQ5	AE10	IO	GV_{DD}	—
MEMC_MDQ6	AD9	IO	GV_{DD}	—
MEMC_MDQ7	AF8	IO	GV_{DD}	—
MEMC_MDQ8	AE6	IO	GV_{DD}	—
MEMC_MDQ9	AD7	IO	GV_{DD}	—
MEMC_MDQ10	AF6	IO	GV_{DD}	—
MEMC_MDQ11	AC7	IO	GV_{DD}	—
MEMC_MDQ12	AD8	IO	GV_{DD}	—
MEMC_MDQ13	AE7	IO	GV_{DD}	—
MEMC_MDQ14	AD6	IO	GV_{DD}	—
MEMC_MDQ15	AF5	IO	GV_{DD}	—
MEMC_MDQ16	AD18	IO	GV_{DD}	—
MEMC_MDQ17	AE19	IO	GV_{DD}	—
MEMC_MDQ18	AF17	IO	GV_{DD}	—
MEMC_MDQ19	AF19	IO	GV_{DD}	—
MEMC_MDQ20	AF18	IO	GV_{DD}	—
MEMC_MDQ21	AE18	IO	GV_{DD}	—
MEMC_MDQ22	AF20	IO	GV_{DD}	—
MEMC_MDQ23	AD19	IO	GV_{DD}	—
MEMC_MDQ24	AD21	IO	GV_{DD}	—
MEMC_MDQ25	AF22	IO	GV_{DD}	—
MEMC_MDQ26	AC21	IO	GV_{DD}	—
MEMC_MDQ27	AF21	IO	GV_{DD}	—
MEMC_MDQ28	AE21	IO	GV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MDQ29	AD20	IO	GV_{DD}	—
MEMC_MDQ30	AF23	IO	GV_{DD}	—
MEMC_MDQ31	AD22	IO	GV_{DD}	—
MEMC_MDM0	AC9	O	GV_{DD}	—
MEMC_MDM1	AD5	O	GV_{DD}	—
MEMC_MDM2	AE20	O	GV_{DD}	—
MEMC_MDM3	AE22	O	GV_{DD}	—
MEMC_MDQS0	AE8	IO	GV_{DD}	—
MEMC_MDQS1	AE5	IO	GV_{DD}	—
MEMC_MDQS2	AC19	IO	GV_{DD}	—
MEMC_MDQS3	AE23	IO	GV_{DD}	—
MEMC_MBA0	AD16	O	GV_{DD}	—
MEMC_MBA1	AD17	O	GV_{DD}	—
MEMC_MBA2	AE17	O	GV_{DD}	—
MEMC_MA0	AD12	O	GV_{DD}	—
MEMC_MA1	AE12	O	GV_{DD}	—
MEMC_MA2	AF12	O	GV_{DD}	—
MEMC_MA3	AC13	O	GV_{DD}	—
MEMC_MA4	AD13	O	GV_{DD}	—
MEMC_MA5	AE13	O	GV_{DD}	—
MEMC_MA6	AF13	O	GV_{DD}	—
MEMC_MA7	AC15	O	GV_{DD}	—
MEMC_MA8	AD15	O	GV_{DD}	—
MEMC_MA9	AE15	O	GV_{DD}	—
MEMC_MA10	AF15	O	GV_{DD}	—
MEMC_MA11	AE16	O	GV_{DD}	—
MEMC_MA12	AF16	O	GV_{DD}	—
MEMC_MA13	AB16	O	GV_{DD}	—
$\overline{\text{MEMC_MWE}}$	AC17	O	GV_{DD}	—
$\overline{\text{MEMC_MRAS}}$	AE11	O	GV_{DD}	—
$\overline{\text{MEMC_MCAS}}$	AD11	O	GV_{DD}	—
$\overline{\text{MEMC_MCS}}$	AC11	O	GV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MCKE	AD14	O	GV_{DD}	3
MEMC_MCK	AF14	O	GV_{DD}	—
$\overline{\text{MEMC_MCK}}$	AE14	O	GV_{DD}	—
MEMC_MODT	AF11	O	GV_{DD}	—
Local Bus Controller Interface				
LAD0	N25	IO	OV_{DD}	—
LAD1	P26	IO	OV_{DD}	—
LAD2	P25	IO	OV_{DD}	—
LAD3	R26	IO	OV_{DD}	—
LAD4	R25	IO	OV_{DD}	—
LAD5	T26	IO	OV_{DD}	—
LAD6	T25	IO	OV_{DD}	—
LAD7	U25	IO	OV_{DD}	—
LAD8	M24	IO	OV_{DD}	—
LAD9	N24	IO	OV_{DD}	—
LAD10	P24	IO	OV_{DD}	—
LAD11	R24	IO	OV_{DD}	—
LAD12	T24	IO	OV_{DD}	—
LAD13	U24	IO	OV_{DD}	—
LAD14	U26	IO	OV_{DD}	—
LAD15	V26	IO	OV_{DD}	—
LA16	K25	O	OV_{DD}	—
LA17	L25	O	OV_{DD}	—
LA18	L26	O	OV_{DD}	—
LA19	L24	O	OV_{DD}	—
LA20	M26	O	OV_{DD}	—
LA21	M25	O	OV_{DD}	—
LA22	N26	O	OV_{DD}	—
LA23	AC24	O	OV_{DD}	—
LA24	AC25	O	OV_{DD}	—
LA25	AB23	O	OV_{DD}	—
$\overline{\text{LCS0}}$	AB24	O	OV_{DD}	4

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS1}}$	AB25	O	OV_{DD}	4
$\overline{\text{LCS2}}$	AA23	O	OV_{DD}	4
$\overline{\text{LCS3}}$	AA24	O	OV_{DD}	4
$\overline{\text{LWE0}}$	Y23	O	OV_{DD}	4
$\overline{\text{LWE1}}$	W25	O	OV_{DD}	4
LBCTL	V25	O	OV_{DD}	4
RST_LALE/M1LALE/M2LALE	V24	O	OV_{DD}	—
CFG_RESET_SOURCE[0]/LSDA10/LGPL0	L23	IO	OV_{DD}	—
CFG_RESET_SOURCE[1]/$\overline{\text{LSDWE}}$/LGPL1	K23	IO	OV_{DD}	—
$\overline{\text{LSDRAS}}$/LGPL2/$\overline{\text{LOE}}$	J23	O	OV_{DD}	4
CFG_RESET_SOURCE[2]/$\overline{\text{LSDCAS}}$/LGPL3	H23	IO	OV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	G23	IO	OV_{DD}	4
LGPL5	AC22	O	OV_{DD}	4
PD_XLB_CLOCK_OUT/LCLK0/ PD_MG2XLB_ENC_CLOCK/CORE_CLK_OUT	Y24	O	OV_{DD}	—
PD_XLB2MG_DDR_CLOCK/LCLK1/ PD_MG2XLB_ENC_SYNC	Y25	O	OV_{DD}	—
DUART				
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	G1	IO	OV_{DD}	—
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	G2	IO	OV_{DD}	—
$\overline{\text{UART_CTS1}}$/MSRCID2 (DDR ID)/LSRCID2	H3	IO	OV_{DD}	—
$\overline{\text{UART_RTS1}}$/MSRCID3 (DDR ID)/LSRCID3	K3	IO	OV_{DD}	—
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	H2	IO	OV_{DD}	—
UART_SIN2/MDVAL (DDR ID)/LDVAL	H1	IO	OV_{DD}	—
$\overline{\text{UART_CTS2}}$	J3	IO	OV_{DD}	—
$\overline{\text{UART_RTS2}}$	K4	IO	OV_{DD}	—
I^2C interface				
IIC_SDA/$\overline{\text{CKSTOP_OUT}}$	AE24	IO	OV_{DD}	2
IIC_SCL/$\overline{\text{CKSTOP_IN}}$	AF24	IO	OV_{DD}	2
Programmable Interrupt Controller				
$\overline{\text{MCP_OUT}}$	AD25	O	OV_{DD}	—
$\overline{\text{IRQ0}}$/$\overline{\text{MCP_IN}}$	AD26	I	OV_{DD}	—
$\overline{\text{IRQ1}}$	K1	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ2}}$	K2	I	OV_{DD}	—
$\overline{\text{IRQ3}}$	J2	I	OV_{DD}	—
$\overline{\text{IRQ4}}$	J1	I	OV_{DD}	—
$\overline{\text{IRQ5}}$	AE26	I	OV_{DD}	—
$\overline{\text{IRQ6}}$/$\overline{\text{CKSTOP_OUT}}$	AE25	IO	OV_{DD}	—
$\overline{\text{IRQ7}}$/$\overline{\text{CKSTOP_IN}}$	AF25	I	OV_{DD}	—
$\overline{\text{CFG_CLKIN_DIV}}$	F1	I	OV_{DD}	—
CFG_LBIU_MUX_EN	M23	I	OV_{DD}	—
JTAG				
TCK	W26	I	OV_{DD}	—
TDI	Y26	I	OV_{DD}	4
TDO	AA26	O	OV_{DD}	3
TMS	AB26	I	OV_{DD}	4
$\overline{\text{TRST}}$	AC26	I	OV_{DD}	4
TEST				
TEST_MODE	N23	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	T23	O	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AC23	IO	OV_{DD}	1
$\overline{\text{PORESET}}$	AD23	I	OV_{DD}	—
$\overline{\text{SRESET}}$	AD24	IO	OV_{DD}	2
Clocks				
CLKIN	R3	I	OV_{DD}	—
$\overline{\text{CLKIN}}$	P4	O	OV_{DD}	—
PCI_SYNC_OUT	V1	O	OV_{DD}	3
RTC_PIT_CLOCK	U23	I	OV_{DD}	—
PCI_SYNC_IN/PCI_CLK	V2	I	OV_{DD}	—
PCI_CLK0/clkpd_cerisc1_ipg_clkout/DPTC_OSC	T3	O	OV_{DD}	—
PCI_CLK1/clkpd_half_cemb4ucc1_ipg_clkout/ CLOCK_XLB_CLOCK_OUT	U2	O	OV_{DD}	—
PCI_CLK2/clkpd_third_cesog_ipg_clkout/ cecl_ipg_ce_clock	R4	O	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Supplies				
$AV_{DD}1$	P3	I	$AV_{DD}1$	—
$AV_{DD}2$	AA1	I	$AV_{DD}2$	—
$AV_{DD}3$	AB15	I	$AV_{DD}3$	—
$AV_{DD}4$	C24	I	$AV_{DD}4$	—
MVREF1	AB8	I	DDR reference voltage	—
MVREF2	AB17	I	DDR reference voltage	—
PCI				
$\overline{\text{PCI_INTA}}$ /$\overline{\text{IRQ_OUT}}$	AF2	O	OV_{DD}	2
$\overline{\text{PCI_RESET_OUT}}$	AE2	O	OV_{DD}	—
PCI_AD0/MSRCID0 (DDR ID)	L1	IO	OV_{DD}	—
PCI_AD1/MSRCID1 (DDR ID)	L2	IO	OV_{DD}	—
PCI_AD2/MSRCID2 (DDR ID)	M1	IO	OV_{DD}	—
PCI_AD3/MSRCID3 (DDR ID)	M2	IO	OV_{DD}	—
PCI_AD4/MSRCID4 (DDR ID)	L3	IO	OV_{DD}	—
PCI_AD5/MDVAL (DDR ID)	N1	IO	OV_{DD}	—
PCI_AD6	N2	IO	OV_{DD}	—
PCI_AD7	M3	IO	OV_{DD}	—
PCI_AD8	P1	IO	OV_{DD}	—
PCI_AD9	R1	IO	OV_{DD}	—
PCI_AD10	N3	IO	OV_{DD}	—
PCI_AD11	N4	IO	OV_{DD}	—
PCI_AD12	T1	IO	OV_{DD}	—
PCI_AD13	R2	IO	OV_{DD}	—
PCI_AD14/ECID_TMODE_IN	T2	IO	OV_{DD}	—
PCI_AD15	U1	IO	OV_{DD}	—
PCI_AD16	Y2	IO	OV_{DD}	—
PCI_AD17	Y1	IO	OV_{DD}	—
PCI_AD18	AA2	IO	OV_{DD}	—
PCI_AD19	AB1	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_AD20	AB2	IO	OV_{DD}	—
PCI_AD21	Y4	IO	OV_{DD}	—
PCI_AD22	AC1	IO	OV_{DD}	—
PCI_AD23	AA3	IO	OV_{DD}	—
PCI_AD24	AA4	IO	OV_{DD}	—
PCI_AD25	AD1	IO	OV_{DD}	—
PCI_AD26	AD2	IO	OV_{DD}	—
PCI_AD27	AB3	IO	OV_{DD}	—
PCI_AD28	AB4	IO	OV_{DD}	—
PCI_AD29	AE1	IO	OV_{DD}	—
PCI_AD30	AC3	IO	OV_{DD}	—
PCI_AD31	AC4	IO	OV_{DD}	—
PCI_C_$\overline{BE0}$	M4	IO	OV_{DD}	—
PCI_C_$\overline{BE1}$	T4	IO	OV_{DD}	—
PCI_C_$\overline{BE2}$	Y3	IO	OV_{DD}	—
PCI_C_$\overline{BE3}$	AC2	IO	OV_{DD}	—
PCI_PAR	U3	IO	OV_{DD}	—
$\overline{PCI_FRAME}$	W1	IO	OV_{DD}	5
$\overline{PCI_TRDY}$	W4	IO	OV_{DD}	5
$\overline{PCI_IRDY}$	W2	IO	OV_{DD}	5
$\overline{PCI_STOP}$	V4	IO	OV_{DD}	5
$\overline{PCI_DEVSEL}$	W3	IO	OV_{DD}	5
PCI_IDSEL	P2	I	OV_{DD}	—
$\overline{PCI_SERR}$	U4	IO	OV_{DD}	5
$\overline{PCI_PERR}$	V3	IO	OV_{DD}	5
$\overline{PCI_REQ0}$	AD4	IO	OV_{DD}	—
$\overline{PCI_REQ1}$/CPCI_HS_ES	AE3	I	OV_{DD}	—
$\overline{PCI_REQ2}$	AF3	I	OV_{DD}	—
$\overline{PCI_GNT0}$	AD3	IO	OV_{DD}	—
$\overline{PCI_GNT1}$/CPCI_HS_LED	AE4	O	OV_{DD}	—
$\overline{PCI_GNT2}$/CPCI_HS_ENUM	AF4	O	OV_{DD}	—
M66EN	L4	I	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE/GPIO				
GPIO_PA0/SER1_TXD[0]/TDMA_TXD[0]/USBTXN	G3	IO	OV_{DD}	—
GPIO_PA1/SER1_TXD[1]/TDMA_TXD[1]/USBTXP	F3	IO	OV_{DD}	—
GPIO_PA2/SER1_TXD[2]/TDMA_TXD[2]	F2	IO	OV_{DD}	—
GPIO_PA3/SER1_TXD[3]/TDMA_TXD[3]	E3	IO	OV_{DD}	—
GPIO_PA4/SER1_RXD[0]/TDMA_RXD[0]/USBRXP	E2	IO	OV_{DD}	—
GPIO_PA5/SER1_RXD[1]/TDMA_RXD[1]/USBRXN	E1	IO	OV_{DD}	—
GPIO_PA6/SER1_RXD[2]/TDMA_RXD[2]/USBRXD	D3	IO	OV_{DD}	—
GPIO_PA7/SER1_RXD[3]/TDMA_RXD[3]	D2	IO	OV_{DD}	—
GPIO_PA8/SER1_CD/TDMA_REQ/$\overline{\text{USBOE}}$	D1	IO	OV_{DD}	—
GPIO_PA9 TDMA_CLKO	C3	IO	OV_{DD}	—
GPIO_PA10/SER1_CTS/TDMA_RSYNC	C2	IO	OV_{DD}	—
GPIO_PA11/TDMA_STROBE	C1	IO	OV_{DD}	—
GPIO_PA12/SER1_RTS/TDMA_TSYNC	B1	IO	OV_{DD}	—
GPIO_PA13/CLK9/BRGO9	H4	IO	OV_{DD}	—
GPIO_PA14/CLK11/BRGO10	G4	IO	OV_{DD}	—
GPIO_PA15/BRGO7	J4	IO	OV_{DD}	—
GPIO_PA16/ LA0 (LBIU)	K24	IO	OV_{DD}	—
GPIO_PA17/ LA1 (LBIU)	K26	IO	OV_{DD}	—
GPIO_PA18/Enet2_TXD[0]/SER2_TXD[0]/ TDMB_TXD[0]/LA2 (LBIU)	G25	IO	OV_{DD}	—
GPIO_PA19/Enet2_TXD[1]/SER2_TXD[1]/ TDMB_TXD[1]/LA3 (LBIU)	G26	IO	OV_{DD}	—
GPIO_PA20/Enet2_TXD[2]/SER2_TXD[2]/ TDMB_TXD[2]/LA4 (LBIU)	H25	IO	OV_{DD}	—
GPIO_PA21/Enet2_TXD[3]/SER2_TXD[3]/ TDMB_TXD[3]/LA5 (LBIU)	H26	IO	OV_{DD}	—
GPIO_PA22/Enet2_RXD[0]/SER2_RXD[0]/ TDMB_RXD[0]/LA6 (LBIU)	C25	IO	OV_{DD}	—
GPIO_PA23/Enet2_RXD[1]/SER2_RXD[1]/ TDMB_RXD[1]/LA7 (LBIU)	C26	IO	OV_{DD}	—
GPIO_PA24/Enet2_RXD[2]/SER2_RXD[2]/ TDMB_RXD[2]/LA8 (LBIU)	D25	IO	OV_{DD}	—
GPIO_PA25/Enet2_RXD[3]/SER2_RXD[3]/ TDMB_RXD[3]/LA9 (LBIU)	D26	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PA26/Enet2_RX_ER/SER2_CD/TDMB_REQ/ LA10 (LBIU)	E26	IO	OV_{DD}	—
GPIO_PA27/Enet2_TX_ER/TDMB_CLKO/LA11 (LBIU)	F25	IO	OV_{DD}	—
GPIO_PA28/Enet2_RX_DV/SER2_CTS/ TDMB_RSYNC/LA12 (LBIU)	E25	IO	OV_{DD}	—
GPIO_PA29/Enet2_COL/RXD[4]/SER2_RXD[4]/ TDMB_STROBE/LA13 (LBIU)	J25	IO	OV_{DD}	—
GPIO_PA30/Enet2_TX_EN/SER2_RTS/ TDMB_TSYNC/LA14 (LBIU)	F26	IO	OV_{DD}	—
GPIO_PA31/Enet2_CRS/SDET LA15 (LBIU)	J26	IO	OV_{DD}	—
GPIO_PB0/Enet3_TXD[0]/SER3_TXD[0]/ TDMC_TXD[0]	A13	IO	OV_{DD}	—
GPIO_PB1/Enet3_TXD[1]/SER3_TXD[1]/ TDMC_TXD[1]	B13	IO	OV_{DD}	—
GPIO_PB2/Enet3_TXD[2]/SER3_TXD[2]/ TDMC_TXD[2]	A14	IO	OV_{DD}	—
GPIO_PB3/Enet3_TXD[3]/SER3_TXD[3]/ TDMC_TXD[3]	B14	IO	OV_{DD}	—
GPIO_PB4/Enet3_RXD[0]/SER3_RXD[0]/ TDMC_RXD[0]	B8	IO	OV_{DD}	—
GPIO_PB5/Enet3_RXD[1]/SER3_RXD[1]/ TDMC_RXD[1]	A8	IO	OV_{DD}	—
GPIO_PB6/Enet3_RXD[2]/SER3_RXD[2]/ TDMC_RXD[2]	A9	IO	OV_{DD}	—
GPIO_PB7/Enet3_RXD[3]/SER3_RXD[3]/ TDMC_RXD[3]	B9	IO	OV_{DD}	—
GPIO_PB8/Enet3_RX_ER/SER3_CD/TDMC_REQ	A11	IO	OV_{DD}	—
GPIO_PB9/Enet3_TX_ER/TDMC_CLKO	B11	IO	OV_{DD}	—
GPIO_PB10/Enet3_RX_DV/SER3_CTS/ TDMC_RSYNC	A10	IO	OV_{DD}	—
GPIO_PB11/Enet3_COL/RXD[4]/SER3_RXD[4]/ TDMC_STROBE	A15	IO	OV_{DD}	—
GPIO_PB12/Enet3_TX_EN/SER3_RTS/ TDMC_TSYNC	B12	IO	OV_{DD}	—
GPIO_PB13/Enet3_CRS/SDET	B15	IO	OV_{DD}	—
GPIO_PB14/CLK12	D9	IO	OV_{DD}	—
GPIO_PB15 UPC1_TxADDR[4]	D14	IO	OV_{DD}	—
GPIO_PB16 UPC1_RxADDR[4]	B16	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PB17/BRGO1/CE_EXT_REQ1	D10	IO	OV_{DD}	—
GPIO_PB18/Enet4_TXD[0]/SER4_TXD[0]/ TDMD_TXD[0]	C10	IO	OV_{DD}	—
GPIO_PB19/Enet4_TXD[1]/SER4_TXD[1]/ TDMD_TXD[1]	C9	IO	OV_{DD}	—
GPIO_PB20/Enet4_TXD[2]/SER4_TXD[2]/ TDMD_TXD[2]	D8	IO	OV_{DD}	—
GPIO_PB21/Enet4_TXD[3]/SER4_TXD[3]/ TDMD_TXD[3]	C8	IO	OV_{DD}	—
GPIO_PB22/Enet4_RXD[0]/SER4_RXD[0]/ TDMD_RXD[0]	C15	IO	OV_{DD}	—
GPIO_PB23/Enet4_RXD[1]/SER4_RXD[1]/ TDMD_RXD[1]	C14	IO	OV_{DD}	—
GPIO_PB24/Enet4_RXD[2]/SER4_RXD[2]/ TDMD_RXD[2]	D13	IO	OV_{DD}	—
GPIO_PB25/Enet4_RXD[3]/SER4_RXD[3]/ TDMD_RXD[3]	C13	IO	OV_{DD}	—
GPIO_PB26/Enet4_RX_ER/SER4_CD/TDMD_REQ	C12	IO	OV_{DD}	—
GPIO_PB27/Enet4_TX_ER/TDMD_CLKO	D11	IO	OV_{DD}	—
GPIO_PB28/Enet4_RX_DV/SER4_CTS/ TDMD_RSYNC	D12	IO	OV_{DD}	—
GPIO_PB29/Enet4_COL/RXD[4]/SER4_RXD[4]/ TDMD_STROBE	D7	IO	OV_{DD}	—
GPIO_PB30/Enet4_TX_EN/SER4_RTS/ TDMD_TSYNC	C11	IO	OV_{DD}	—
GPIO_PB31/Enet4_CRS/SDET	C7	IO	OV_{DD}	—
GPIO_PC0/UPC1_TxDATA[0]/SER5_TXD[0]	A18	IO	OV_{DD}	—
GPIO_PC1/UPC1_TxDATA[1]/SER5_TXD[1]	A19	IO	OV_{DD}	—
GPIO_PC2/UPC1_TxDATA[2]/SER5_TXD[2]	B18	IO	OV_{DD}	—
GPIO_PC3/UPC1_TxDATA[3]/SER5_TXD[3]	B19	IO	OV_{DD}	—
GPIO_PC4/UPC1_TxDATA[4]	A24	IO	OV_{DD}	—
GPIO_PC5/UPC1_TxDATA[5]	B24	IO	OV_{DD}	—
GPIO_PC6/UPC1_TxDATA[6]	A23	IO	OV_{DD}	—
GPIO_PC7/UPC1_TxDATA[7]	B26	IO	OV_{DD}	—
GPIO_PC8/UPC1_RxDATA[0]/SER5_RXD[0]	A21	IO	OV_{DD}	—
GPIO_PC9/UPC1_RxDATA[1]/SER5_RXD[1]	B20	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PC10/UPC1_RxDATA[2]/SER5_RXD[2]	B21	IO	OV_{DD}	—
GPIO_PC11/UPC1_RxDATA[3]/SER5_RXD[3]	A20	IO	OV_{DD}	—
GPIO_PC12/UPC1_RxDATA[4]	D19	IO	OV_{DD}	—
GPIO_PC13/UPC1_RxDATA[5]/LSRCID0	C18	IO	OV_{DD}	—
GPIO_PC14/UPC1_RxDATA[6]/LSRCID1	D18	IO	OV_{DD}	—
GPIO_PC15/UPC1_RxDATA[7]/LSRCID2	A25	IO	OV_{DD}	—
GPIO_PC16/UPC1_TxADDR[0]	C21	IO	OV_{DD}	—
GPIO_PC17/UPC1_TxADDR[1]/LSRCID3	D22	IO	OV_{DD}	—
GPIO_PC18/UPC1_TxADDR[2]/LSRCID4	C23	IO	OV_{DD}	—
GPIO_PC19/UPC1_TxADDR[3]/LDVAL	D23	IO	OV_{DD}	—
GPIO_PC20/UPC1_RxADDR[0]	C17	IO	OV_{DD}	—
GPIO_PC21/UPC1_RxADDR[1]	D17	IO	OV_{DD}	—
GPIO_PC22/UPC1_RxADDR[2]	C16	IO	OV_{DD}	—
GPIO_PC23/UPC1_RxADDR[3]	D16	IO	OV_{DD}	—
GPIO_PC24/UPC1_RxSOC/SER5_CD	A16	IO	OV_{DD}	—
GPIO_PC25/UPC1_RxCLAV	D20	IO	OV_{DD}	—
GPIO_PC26/UPC1_RxPRTY/CE_EXT_REQ2	E23	IO	OV_{DD}	—
GPIO_PC27/UPC1_RxEN	B17	IO	OV_{DD}	—
GPIO_PC28/UPC1_TxSOC	B22	IO	OV_{DD}	—
GPIO_PC29/UPC1_TxCLAV/SER5_CTS	A17	IO	OV_{DD}	—
GPIO_PC30/UPC1_TxPRTY	A22	IO	OV_{DD}	—
GPIO_PC31/UPC1_TxEN/SER5_RTS	C20	IO	OV_{DD}	—
GPIO_PD0/SPIMOSI	A2	IO	OV_{DD}	—
GPIO_PD1/SPIMISO	B2	IO	OV_{DD}	—
GPIO_PD2/SPICLK	B3	IO	OV_{DD}	—
GPIO_PD3/SPISEL	A3	IO	OV_{DD}	—
GPIO_PD4/SPI_MDIO/CE_MUX_MDIO	A4	IO	OV_{DD}	—
GPIO_PD5/SPI_MDC/CE_MUX_MDC	B4	IO	OV_{DD}	—
GPIO_PD6/CLK8/BRGO16/CE_EXT_REQ3	F24	IO	OV_{DD}	—
GPIO_PD7/GTM1_TIN1/GTM2_TIN2/CLK5	G24	IO	OV_{DD}	—
GPIO_PD8/$\overline{\text{GTM1_TGATE1}}$/$\overline{\text{GTM2_TGATE2}}$/CLK6	H24	IO	OV_{DD}	—
GPIO_PD9/$\overline{\text{GTM1_TOUT1}}$	D24	IO	OV_{DD}	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO_PD10/GTM1_TIN2/GTM2_TIN1/CLK17	J24	IO	OV_{DD}	—
GPIO_PD11/$\overline{\text{GTM1_TGATE2}}$/$\overline{\text{GTM2_TGATE1}}$	B25	IO	OV_{DD}	—
GPIO_PD12/$\overline{\text{GTM1_TOUT2}}$/$\overline{\text{GTM2_TOUT1}}$	C4	IO	OV_{DD}	—
GPIO_PD13/GTM1_TIN3/GTM2_TIN4/BRGO8	D4	IO	OV_{DD}	—
GPIO_PD14/$\overline{\text{GTM1_TGATE3}}$/$\overline{\text{GTM2_TGATE4}}$	D5	IO	OV_{DD}	—
GPIO_PD15/$\overline{\text{GTM1_TOUT3}}$	A5	IO	OV_{DD}	—
GPIO_PD16/GTM1_TIN4/GTM2_TIN3	B5	IO	OV_{DD}	—
GPIO_PD17/$\overline{\text{GTM1_TGATE4}}$/$\overline{\text{GTM2_TGATE3}}$	C5	IO	OV_{DD}	—
GPIO_PD18/$\overline{\text{GTM1_TOUT4}}$/$\overline{\text{GTM2_TOUT3}}$	A6	IO	OV_{DD}	—
GPIO_PD19/CE_RISC1_INT/CE_EXT_REQ4	B6	IO	OV_{DD}	—
GPIO_PD20/CLK18/BRGO6	D21	IO	OV_{DD}	—
GPIO_PD21/CLK16/BRGO5/UPC1_CLKO	C19	IO	OV_{DD}	—
GPIO_PD22/CLK4/BRGO9/UCC2_CLKO	A7	IO	OV_{DD}	—
GPIO_PD23/CLK3/BRGO10/UCC3_CLKO	B7	IO	OV_{DD}	—
GPIO_PD24/CLK10/BRGO2/UCC4_CLKO	A12	IO	OV_{DD}	—
GPIO_PD25/CLK13/BRGO16/UCC5_CLKO	B10	IO	OV_{DD}	—
GPIO_PD26/CLK2/BRGO4/UCC1_CLKO	E4	IO	OV_{DD}	—
GPIO_PD27/CLK1/BRGO3	F4	IO	OV_{DD}	—
GPIO_PD28/CLK19/BRGO11	D15	IO	OV_{DD}	—
GPIO_PD29/CLK15/BRGO8	C6	IO	OV_{DD}	—
GPIO_PD30/CLK14	D6	IO	OV_{DD}	—
GPIO_PD31/CLK7/BRGO15	E24	IO	OV_{DD}	—
Power anf Ground Supplies				
GV_{DD}	AA8, AA10, AA11, AA13, AA14, AA16, AA17, AA19, AA21, AB9, AB10, AB11, AB12, AB14, AB18, AB20, AB21, AC6, AC8, AC14, AC18	GV_{DD}	—	—
OV_{DD}	E5, E6, E8, E9, E10, E12, E14, E15, E16, E18, E19, E20, E22, F5, F6, F8, F10, F14, F16, F19, F22, G22, H5, H6, H21, J5, J22, K21, K22, L5, L6, L22, M5, M22, N5, N21, N22, P6, P22, P23, R5, R23, T5, T21, T22, U6, U22, V5, V22, W22, Y5, AB5, AB6, AC5	OV_{DD}	—	—

Table 55. MPC8323E PBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	K10, K11, K12, K13, K14, K15, K16, K17, L10, L17, M10, M17, N10, N17, P10, P17, R10, R17, T10, T17, U10, U11, U12, U13, U14, U15, U16, U17	V_{DD}	—	—
V_{SS}	B23, E7, E11, E13, E17, E21, F11, F13, F17, F21, F23, G5, H22, K5, K6, L11, L12, L13, L14, L15, L16, L21, M11, M12, M13, M14, M15, M16, N6, N11, N12, N13, N14, N15, N16, P5, P11, P12, P13, P14, P15, P16, P21, R11, R12, R13, R14, R15, R16, R22, T6, T11, T12, T13, T14, T15, T16, U5, U21, V23, W5, W6, W21, W23, W24, Y22, AA5, AA6, AA22, AA25, AB7, AB13, AB19, AB22, AC10, AC12, AC16, AC20	V_{SS}	—	—
No Connect				
NC	C22	—	—	—

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG and local bus pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow the PCI specification's recommendation.
6. This pin must always be tied to GND.

22 Clocking

Figure 43 shows the internal distribution of clocks within the MPC8323E.

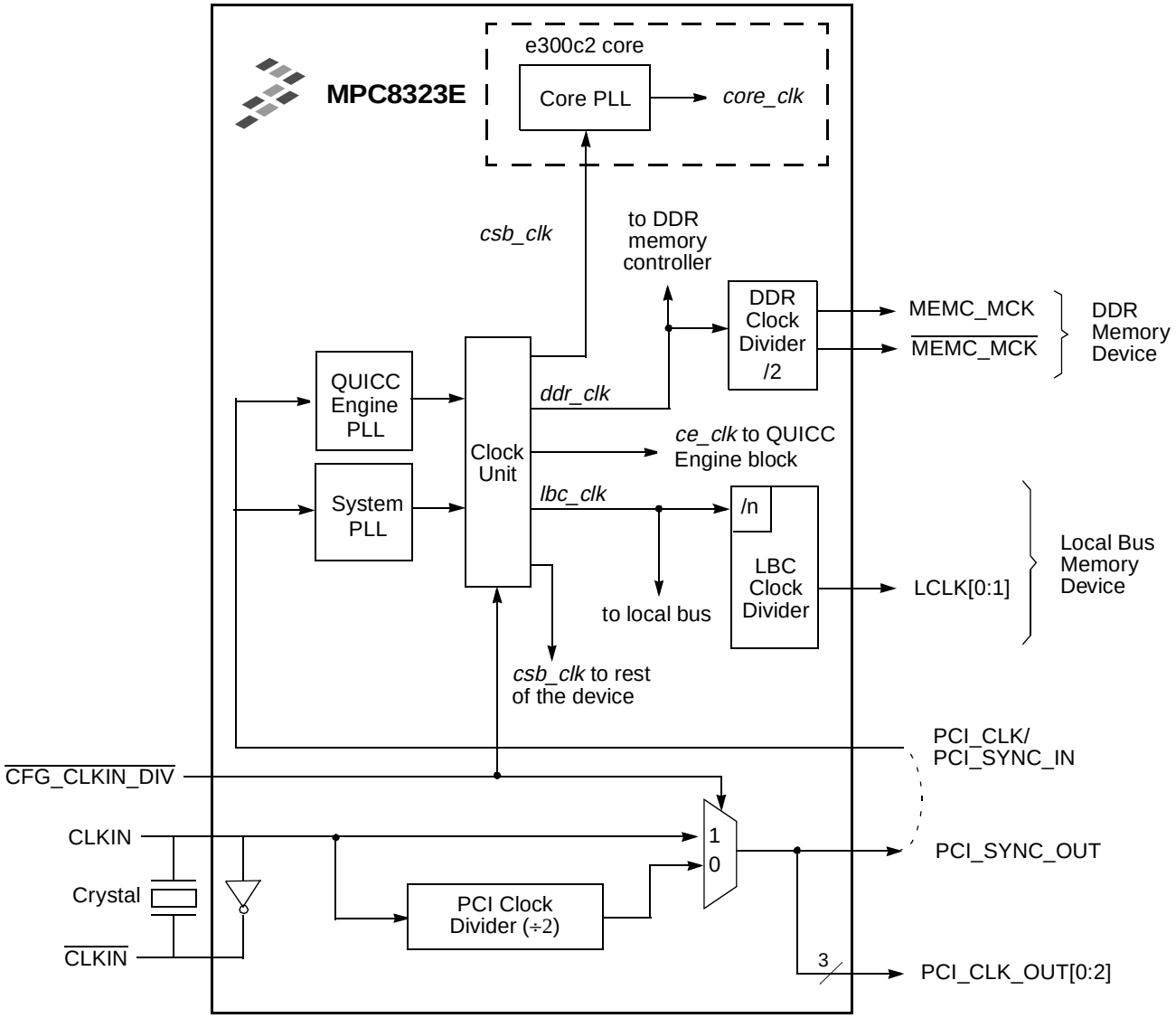


Figure 43. MPC8323E Clock Subsystem

The primary clock source for the MPC8323E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode, respectively.

22.1 Clocking in PCI Host Mode

When the MPC8323E is configured as a PCI host device (RCWH[PCIHOST] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexors. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

22.1.1 PCI Clock Outputs (PCI_CLK_OUT[0:2])

When the MPC8323E is configured as a PCI host, it provides three separate clock output signals, PCI_CLK_OUT[0:2], for external PCI agents.

When the device comes out of reset, the PCI clock outputs are disabled and are actively driven to a steady low state. Each of the individual clock outputs can be enabled (enable toggling of the clock) by setting its corresponding OCCR[PCICOE*n*] bit. All output clocks are phase-aligned to each other.

22.2 Clocking in PCI Agent Mode

When the MPC8323E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal should be tied to GND, and the clock output signals, PCI_CLK_OUT*n* and PCI_SYNC_OUT, are not used.

22.3 System Clock Domains

As shown in Figure 43, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create three major clock domains:

- The coherent system bus clock (*csb_clk*)
- The QUICC Engine clock (*ce_clk*)
- The internal clock for the DDR controller (*ddr_clk*)
- The internal clock for the local bus controller (*lb_clk*)

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = [\text{PCI_SYNC_IN} \times (1 + \sim\overline{\text{CFG_CLKIN_DIV}})] \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG_CLKIN_DIV}}$) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300c2 core. A second PLL inside the core multiplies up the *csb_clk* frequency to create the internal clock for the core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See the “Reset Configuration” section in the *MPC8323E PowerQUICC™ II Pro Communications Processor Reference Manual* for more information.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

When CLKIN is the primary input clock,

ce_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

When PCI_CLK is the primary input clock,

ce_clk = [primary clock input × CEPMF × (1 + ~CFG_CLKIN_DIV)] ÷ (1 + CEPDF)

See the "QUICC Engine PLL Multiplication Factor" section and the "QUICC Engine PLL Division Factor" section in the *MPC8323E PowerQUICC™ II Pro Communications Processor Reference Manual* for more information.

The DDR SDRAM memory controller operates with a frequency equal to twice the frequency of *csb_clk*. Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The local bus memory controller operates with a frequency equal to the frequency of *csb_clk*. Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the LBC clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBC clock divider ratio is controlled by LCCR[CLKDIV]. See the "LBC Bus Clock and Clock Ratios" section in the *MPC8323E PowerQUICC™ II Pro Communications Processor Reference Manual* for more information.

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. These units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 56 specifies which units have a configurable clock frequency. Refer to the "System Clock Control Register (SCCR)" section in the *MPC8323E PowerQUICC™ II Pro Communications Processor Reference Manual* for a detailed description.

Table 56. Configurable Clock Units

Unit	Default Frequency	Options
Security core, I2C, SAP, TPR	*csb_clk*	Off, *csb_clk*/2, *csb_clk*/3
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

NOTE

Setting the clock ratio of these units must be performed prior to any access to them.

Table 57 provides the operating frequencies for the 8323E PBGA under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for PBGA

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	333	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
QUICC Engine frequency (*ce_clk*)	200	MHz

Table 57. Operating Frequencies for PBGA (continued)

Characteristic[1]	Max Operating Frequency	Unit
DDR1/DDR2 memory bus frequency (MCLK)[2]	133	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (CLKIN or PCI_CLK)	66	MHz

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2 The DDR1/DDR2 data rate is 2× the DDR1/DDR2 memory bus frequency.
3 The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

22.4 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

NOTE

System PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 300–600 MHz.

Table 58. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

As described in Section 22, “Clocking,” the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG_CLKIN_DIV}}$ configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59

shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options

CFG_CLKIN_DIV_B at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1		100	
High	0100	4 : 1	100	133	
High	0101	5 : 1	125		
High	0110	6 : 1			
High	0111	7 : 1			
High	1000	8 : 1			
High	1001	9 : 1			
High	1010	10 : 1			
High	1011	11 : 1			
High	1100	12 : 1			
High	1101	13 : 1			
High	1110	14 : 1			
High	1111	15 : 1			
High	0000	16 : 1			
Low	0010	2 : 1			133
Low	0011	3 : 1		100	
Low	0100	4 : 1		133	
Low	0101	5 : 1			
Low	0110	6 : 1			
Low	0111	7 : 1			
Low	1000	8 : 1			
Low	1001	9 : 1			
Low	1010	10 : 1			
Low	1011	11 : 1			
Low	1100	12 : 1			
Low	1101	13 : 1			
Low	1110	14 : 1			
Low	1111	15 : 1			
Low	0000	16 : 1			

1 CFG_CLKIN_DIV_B is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV_B must be pulled up (high) in agent mode.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

22.5 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 60 shows the encodings for RCWL[COREPLL]. COREPLL values not listed in Table 60 should be considered reserved.

Table 60. e300 Core PLL Configuration

RCWL[COREPLL]			***core_clk* : *csb_clk* Ratio**	**VCO Divider**
0-1	**2-5**	**6**		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	÷2
01	**0001**	0	1:1	÷4
10	**0001**	0	1:1	÷8
11	**0001**	0	1:1	÷8
00	**0001**	1	1.5:1	÷2
01	**0001**	1	1.5:1	÷4
10	**0001**	1	1.5:1	÷8
11	**0001**	1	1.5:1	÷8
00	**0010**	0	2:1	÷2
01	**0010**	0	2:1	÷4
10	**0010**	0	2:1	÷8
11	**0010**	0	2:1	÷8
00	**0010**	1	2.5:1	÷2
01	**0010**	1	2.5:1	÷4
10	**0010**	1	2.5:1	÷8
11	**0010**	1	2.5:1	÷8
00	**0011**	0	3:1	÷2
01	**0011**	0	3:1	÷4
10	**0011**	0	3:1	÷8
11	**0011**	0	3:1	÷8

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 500–800 MHz.

22.6 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. Table 61 shows the multiplication factor encodings for the QUICC Engine PLL.

Table 61. QUICC Engine PLL Multiplication Factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF)
00000–00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001–11111	0	Reserved

The RCWL[CEVCOD] denotes the QUICC Engine PLL VCO internal frequency as shown in Table 62.

Table 62. QUICC Engine PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine VCO frequency is in the range of 300–600 MHz. The QUICC Engine frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine frequencies should be selected according to the performance requirements.

The QUICC Engine VCO frequency is derived from the following equations:

$$ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$$

$$\text{QUICC Engine VCO Frequency} = ce_clk \times \text{VCO divider} \times (1 + \text{CEPDF})$$

22.7 Suggested PLL Configurations

To simplify the PLL configurations, the MPC8323E might be separated into two clock domains. The first domain contain the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. Table 63 shows suggested PLL configurations for 33, 25, and 66 MHz input clocks.

Table 63. Suggested PLL Configurations

Conf No.	SPMF	Core PLL	CEMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0110	0	33.33	133.33	266.66	200
2	0100	0000101	1000	0	25	100	250	200
3	0010	0000100	0011	0	66.67	133.33	266.66	200
4	0100	0000101	0110	0	33.33	133.33	333.33	200
5	0101	0000101	1000	0	25	125	312.5	200
6	0010	0000101	0011	0	66.67	133.33	333.33	200

23 Thermal

This section describes the thermal specifications of the MPC8323E.

23.1 Thermal Characteristics

Table 64 provides the package thermal characteristics for the 516 27 × 27 mm PBGA of the MPC8323E.

Table 64. Package Thermal Characteristics for PBGA

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single-layer board (1s)	$R_{\theta JA}$	28	°C/W	1, 2
Junction-to-ambient natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	21	°C/W	1, 2 ,3
Junction-to-ambient (@200 ft/min)	Single-layer board (1s)	$R_{\theta JMA}$	23	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	13	°C/W	4
Junction-to-case	—	$R_{\theta JC}$	9	°C/W	5

Table 64. Package Thermal Characteristics for PBGA (continued)

Characteristic	Board type	Symbol	Value	Unit	Notes
Junction-to-package top	Natural convection	Ψ_{JT}	2	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

23.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

23.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

23.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

23.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

23.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics 800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

23.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

23.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the

interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_C = case temperature of the package (°C)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
P_D = power dissipation (W)

24 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8323E.

24.1 System Clocking

The MPC8323E includes three PLLs.

- The system PLL ($AV_{DD}2$) generates the system clock from the externally supplied CLKIN input. The frequency ratio between the system and CLKIN is selected using the system PLL ratio configuration bits as described in Section 22.4, “System PLL Configuration.”
- The e300 core PLL ($AV_{DD}3$) generates the core clock as a slave to the system clock. The frequency ratio between the e300 core clock and the system clock is selected using the e300 PLL ratio configuration bits as described in Section 22.5, “Core PLL Configuration.”
- The QUICC Engine PLL ($AV_{DD}1$) which uses the same reference as the system PLL. The QUICC Engine block generates or uses external sources for all required serial interface clocks.

24.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each $AV_{DD}n$ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 44, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 44 shows the PLL power supply filter circuit.

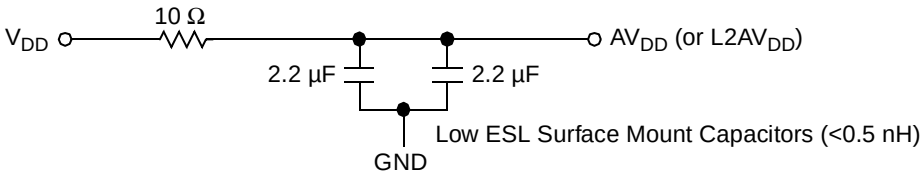


Figure 44. PLL Power Supply Filter Circuit

24.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8323E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8323E system, and the MPC8323E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8323E. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

24.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, or GV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, OV_{DD}, and GND pins of the MPC8323E.

24.5 Output Buffer DC Impedance

The MPC8323E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 45). The

output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

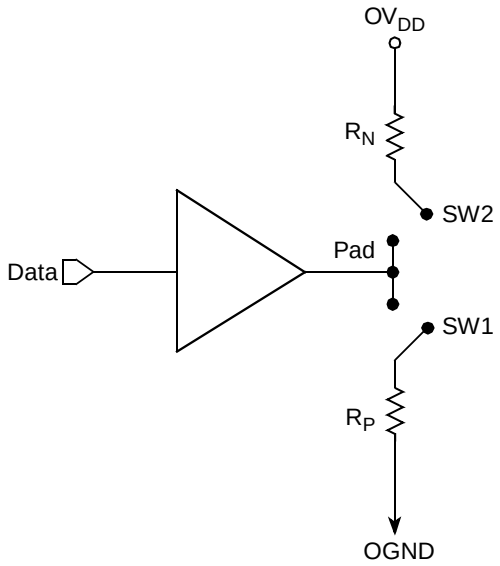


Figure 45. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 65. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

24.6 Configuration Pin Multiplexing

The MPC8323E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

24.7 Pull-Up Resistor Requirements

The MPC8323E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins, Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see AN3361, “MPC8321E/MPC8323E PowerQUICC™ Design Checklist,” Rev. 1.

25 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 25.1, “Part Numbers Fully Addressed by This Document.”

25.1 Part Numbers Fully Addressed by This Document

Table 66 provides the Freescale part numbering nomenclature for the MPC8323E family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.

Table 66. Part Numbering Nomenclature

MPC	*nnnn*	*E*	*C*	*VR*	*AF*	*D*	*C*	*A*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR Frequency**	**QUICC Engine Frequency**	**Revision Level**
MPC	8323	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	VR = Pb-free PBGA ZQ = Pb PBGA	AD = 266 MHz AF = 333 MHz	D = 266 MHz	C = 200 MHz	Contact local Freescale sales office

Notes:

1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 21, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

25.2 Part Marking

Parts are marked as in the example shown in Figure 46.



PBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 46. Freescale Part Marking for PBGA Devices

26 Document Revision History

Table 67 provides a revision history for this hardware specification.

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
3	12/2009	• Removed references for note 4 from Table 1. • Added Figure 2 in Section 2.1.2, “Power Supply Voltage Specification. • Added symbol T_A in Table 2. • Added footnote 2 in Table 2. • Added a note in Section 4, “Clock Input Timing for rise/fall time of QE input pins. • Modified CLKIN, PCI_CLK rise/fall time parameters in Table 8. Modified min value of t_{MCK} in Table 19. • Modified Figure 43. • Modified formula for ce_clk calculation in Section 22.3, “System Clock Domains. • Added a note in Section 22.4, “System PLL Configuration. • Removed the signal ECID_TMODE_IN from Table 55. • Removed all references of RST signals from Table 55.
2	4/2008	• Removed Figures 2 and 3 overshoot and undershoot voltage specs from Section 2.1.2, “Power Supply Voltage Specification,” and footnotes 4 and 5 from Table 1. • Corrected QUIESCE signal to be an output signal in Table 55. • Added column for GVDD (1.8 V) - DDR2 - to Table 6 with 0.212-W typical power dissipation. • Added Figure 4 DDR input timing diagram. • Removed CE_TRB* and CE_PIO* signals from Table 55. • Added three local bus AC specifications to Table 30 (duty cycle, jitter, delay between input clock and local bus clock). • Added row in Table 2 stating junction temperature range of 0 to 105°C. • Modified Section 2.2, “Power Sequencing,” to include $\overline{\text{PORESET}}$ requirement.

Table 67. Document Revision History

Rev. No.	Date	Substantive Change(s)
1	6/2007	Correction to descriptive text in Section 2.2.
0	6/2007	Initial release.

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Document Number: MPC8323EEC
Rev. 3
02/2010



