CY7C10612DV33

16-Mbit (1 M × 16) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 175 mA at 10 ns
- Low CMOS standby power
  - I_{SB2} = 25 mA
- Operating voltages of 3.3 ± 0.3 V
- 2.0 V data retention
- Automatic Power-down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features
- Available in Pb-free 54-pin TSOP II package

Functional Description

The CY7C10612DV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

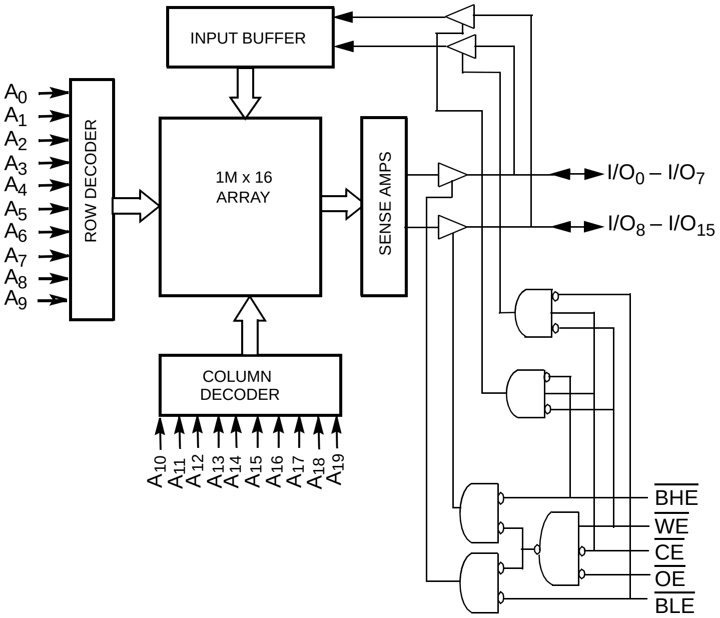
To write to the device, take Chip Enables ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) input LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins appears on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory appears on I/O$_8$ to I/O$_{15}$. See the Truth Table on page 9 for a complete description of Read and Write modes.

The input or output pins (I/O$_0$ through I/O$_{15}$) are placed in a high impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), the $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW).

The CY7C10612DV33 is available in a 54-Pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram

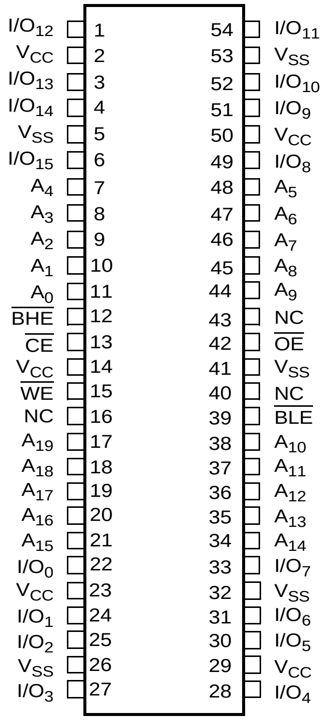


Selection Guide

Description	–10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	175	mA
Maximum CMOS Standby Current	25	mA

Pin Configuration

Figure 1. 54-Pin TSOP II (Top View) [1]



Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature with
Power Applied .... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND [2]..–0.5 V to +4.6 V

DC Voltage Applied to Outputs
in High Z State [2]................................–0.5 V to V_{CC} + 0.5 V

DC Input Voltage [2]............................–0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage...> 2001 V

(MIL-STD-883, Method 3015)

Latch Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	–10		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage [2]		–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = 1/t_{RC}, I_{OUT} = 0 mA CMOS levels		175	mA
I_{SB1}	Automatic CE power-down current — TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		30	mA
I_{SB2}	Automatic CE power-down current —CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0		25	mA

Note

2. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 2 V for pulse durations of less than 20 ns.

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
C_{IN}	Input capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 3.3$ V	6	pF
C_{OUT}	I/O capacitance		8	pF

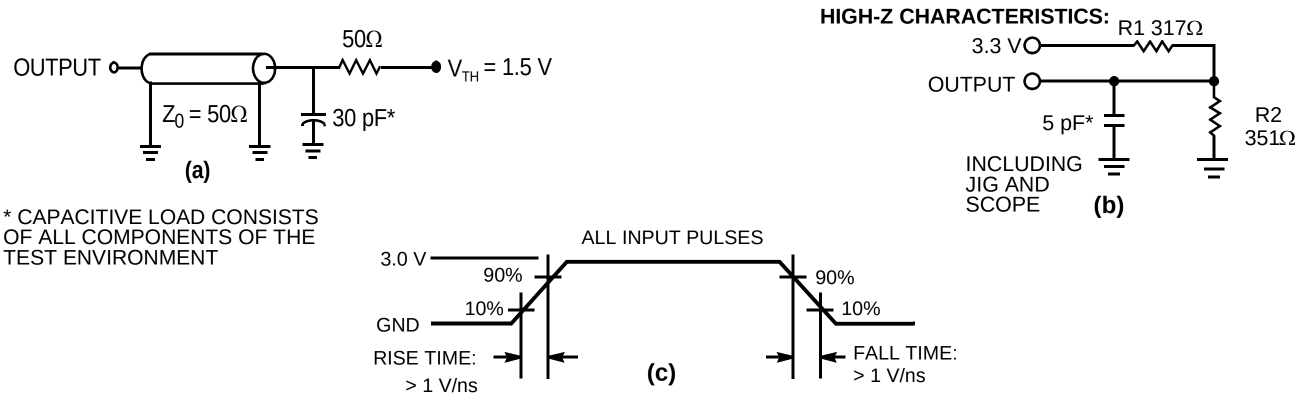
Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	24.18	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		5.40	°C/W

The AC Test Loads and Waveforms diagram follows. [3]

Figure 2. AC Test Loads and Waveforms



Note

3. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 μs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.

AC Switching Characteristics

Over the Operating Range [4]

Parameter	Description	–10		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(Typical) to the First Access [5]	100		µs
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [6]		5	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [6]	3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [6]		5	ns
t_{PU}	$\overline{CE}$ LOW to Power-up [7]	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down [7]		10	ns
t_{DBE}	Byte Enable to Data Valid		5	ns
t_{LZBE}	Byte Enable to Low Z	1		ns
t_{HZBE}	Byte Disable to High Z		5	ns
Write Cycle [8, 9]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		ns
t_{AW}	Address Setup to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		ns
t_{SD}	Data Setup to Write End	5.5		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [6]		5	ns
t_{BW}	Byte Enable to End of Write	7		ns

Notes

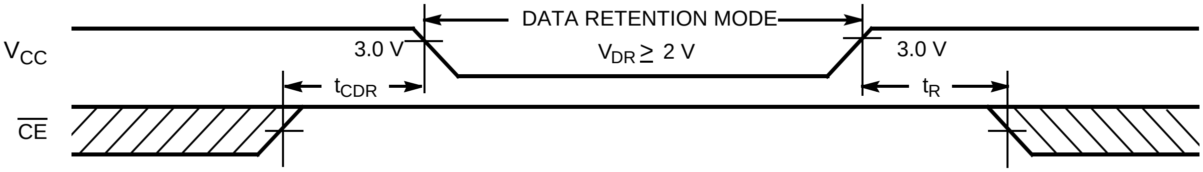
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of AC Test Loads and Waveforms, unless specified otherwise.
5. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
6. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms. Transition is measured ±200 mV from steady state voltage.
7. These parameters are guaranteed by design and are not tested.
8. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. Chip enable must be active and $\overline{WE}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics

Over the Operating Range

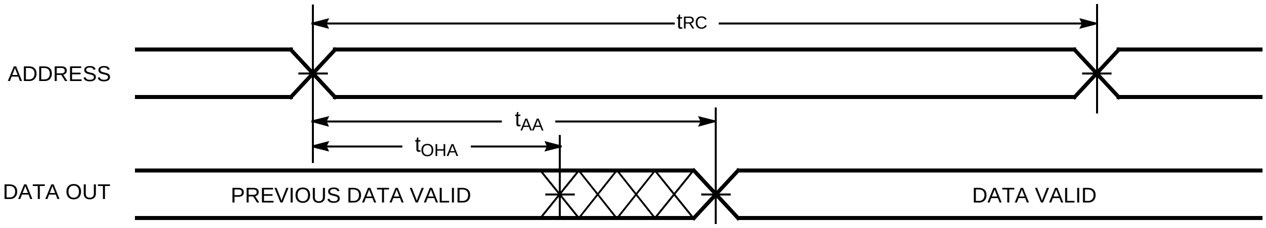
Parameter	Description	Conditions	Min	Typ[10]	Max	Unit
V_{DR}	V_{CC} for data retention		2			V
I_{CCDR}	Data retention current	$V_{CC} = 2$ V , $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V			25	mA
t_{CDR} [11]	Chip deselect to data retention time		0			ns
t_R [12]	Operation recovery time		t_{RC}			ns

Data Retention Waveform



Switching Waveforms

Figure 3. Read Cycle No. 1 [13, 14]



Notes

[10] Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$(typ), $T_A = 25$ °C

[11] Tested initially and after any design or process changes that may affect these parameters.

[12] Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ µs or stable at $V_{CC(min.)} \geq 50$ µs.

[13] The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}.

[14] $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [15, 16]

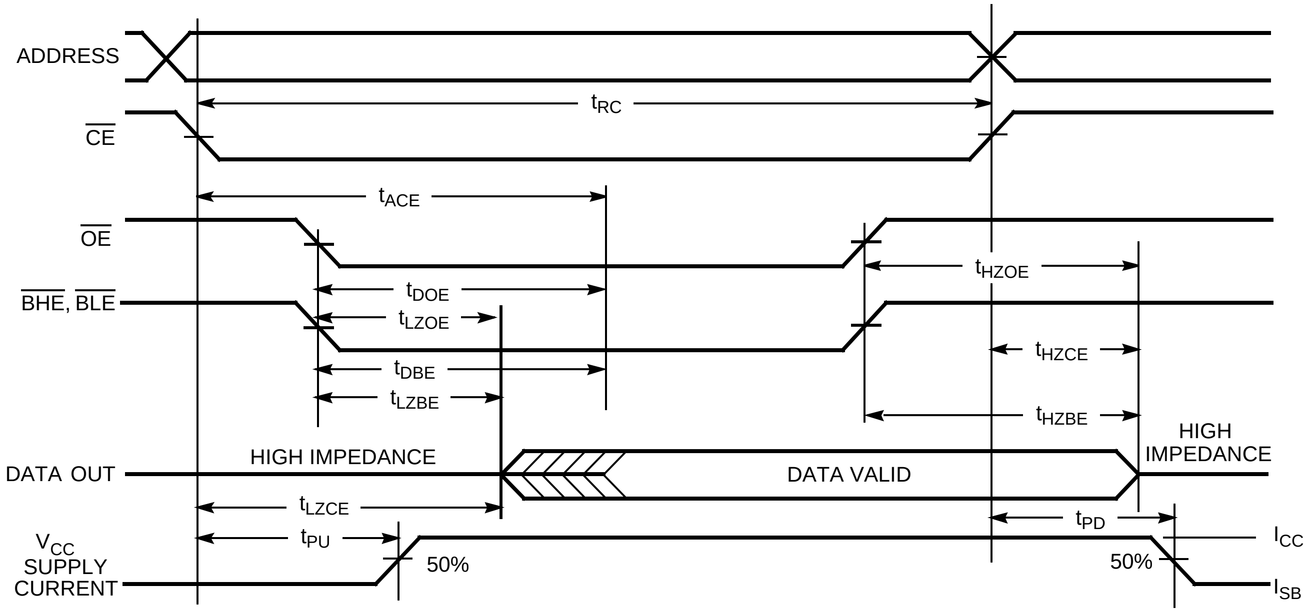
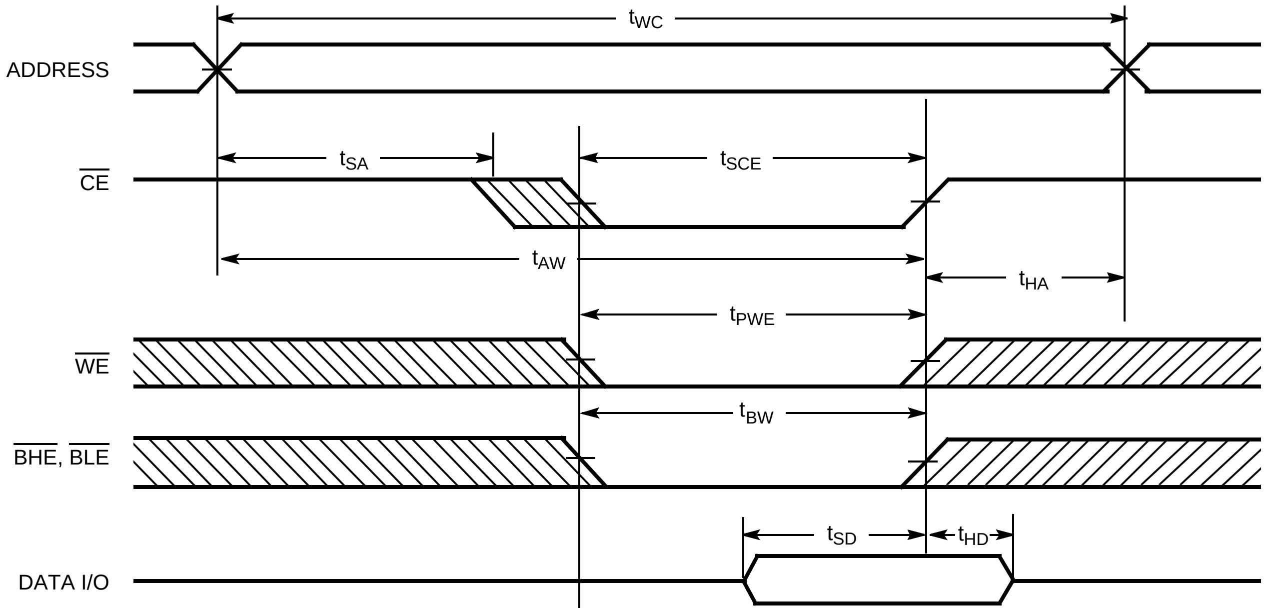


Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17, 18]



Notes

[15] $\overline{WE}$ is HIGH for read cycle.

[16] Address valid before or similar to $\overline{CE}$ transition LOW.

[17] Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.

[18] If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [19, 20]

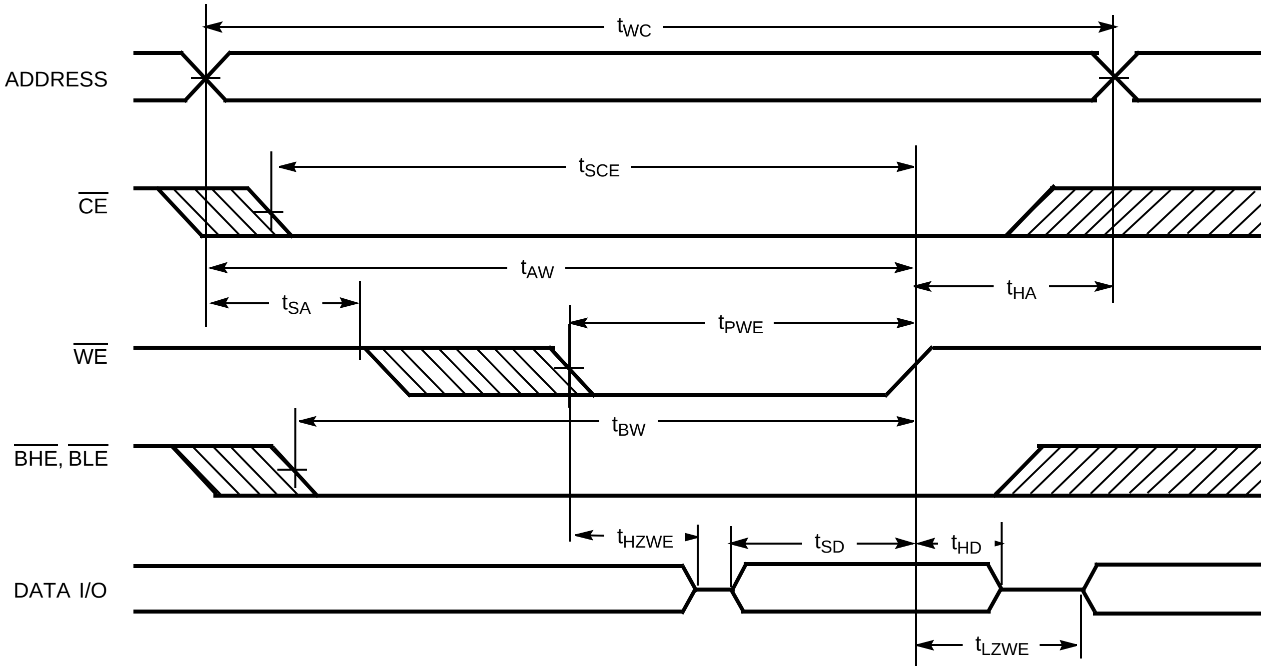
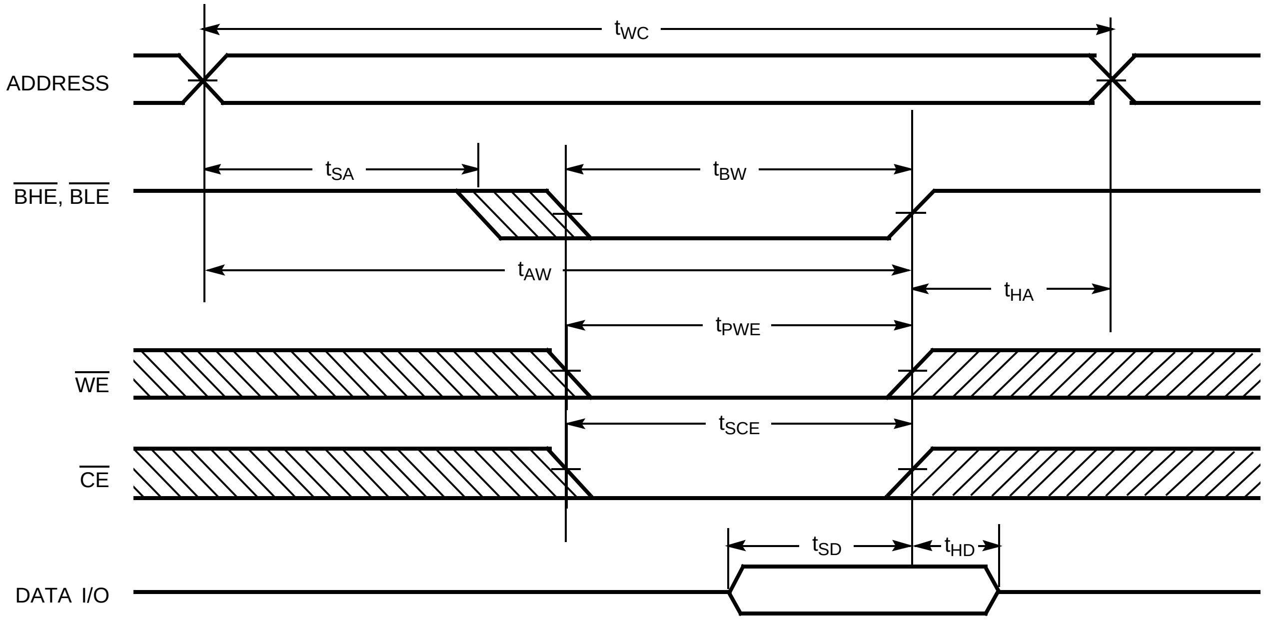


Figure 7. Write Cycle No. 3 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled) [19]



Notes

[19] Data I/O is high impedance if $\overline{\text{OE}}$, $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}}$ = V_{IH}.

[20] If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

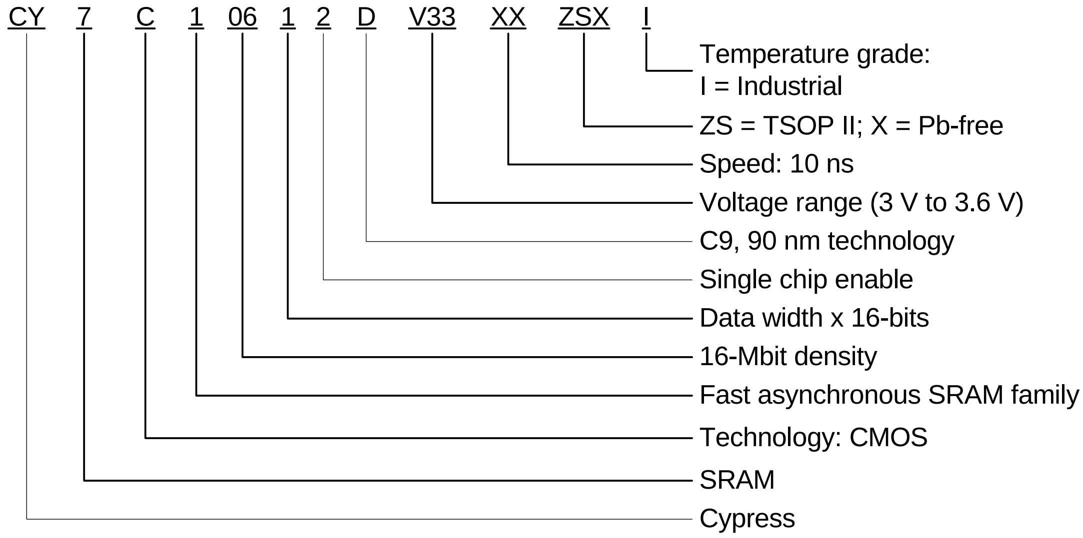
Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O$_0$–I/O$_7$	I/O$_8$–I/O$_{15}$	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I$_{SB}$)
L	L	H	L	L	Data Out	Data Out	Read all bits	Active (I$_{CC}$)
L	L	H	L	H	Data Out	High-Z	Read lower bits only	Active (I$_{CC}$)
L	L	H	H	L	High-Z	Data Out	Read upper bits only	Active (I$_{CC}$)
L	X	L	L	L	Data In	Data In	Write all bits	Active (I$_{CC}$)
L	X	L	L	H	Data In	High-Z	Write lower bits only	Active (I$_{CC}$)
L	X	L	H	L	High-Z	Data In	Write upper bits only	Active (I$_{CC}$)
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active (I$_{CC}$)

Ordering Information

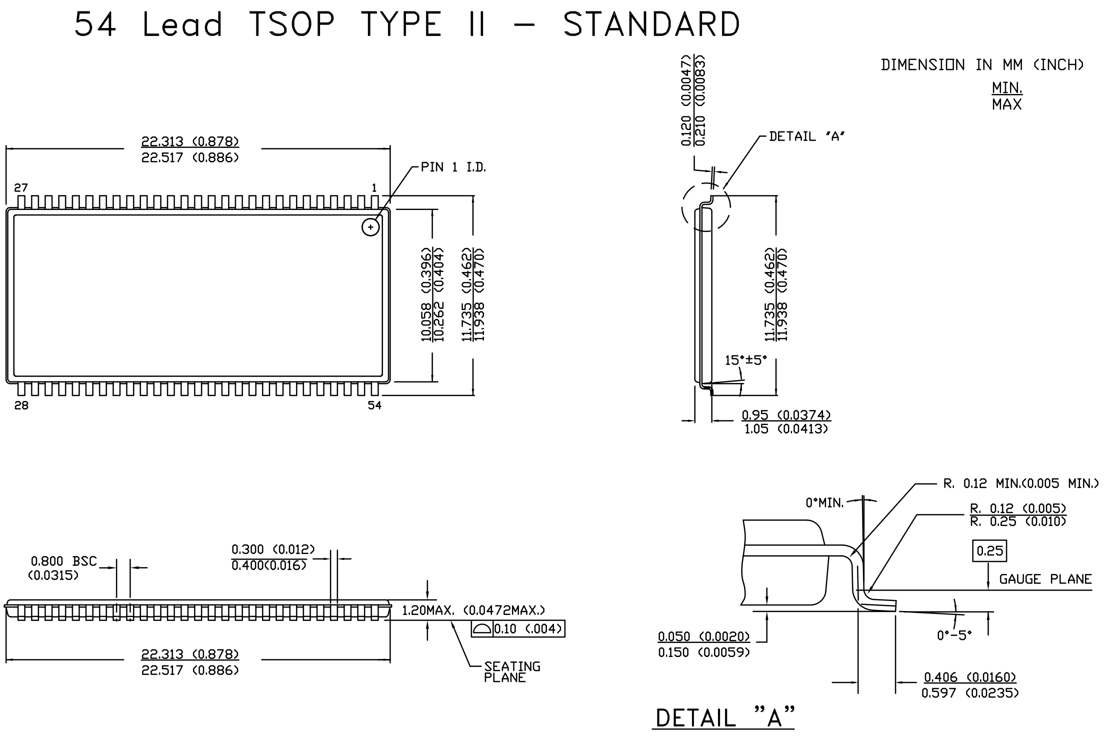
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C10612DV33-10ZSXI	51-85160	54-Pin TSOP II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagrams

Figure 8. 54-Pin TSOP Type II



51-85160 *A

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
CE	chip enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	output enable
SRAM	Static random access memory
SOJ	Small Outline J-Lead
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts

Document History Page

Document Title: CY7C10612DV33, 16-Mbit (1 M × 16) Static RAM
Document Number: 001-49315

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2589743	VKN/PYRS	10/15/08	New datasheet
*A	2718906	VKN	06/15/09	Post to external web
*B	3128718	PRAS	01/05/11	Template updates. Style changes. IO changed to I/O through out the document. Under Data Retention Characteristics on Page 6, “Typ” is associated with a new footnote # 10. Included ordering code definitions, Acronyms and units of measure tables. Updated package diagram from ** to *A.

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