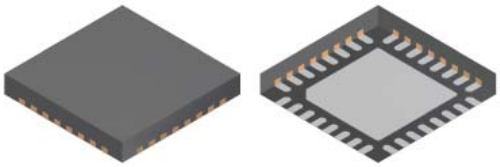
# 3-Phase Brushless DC Motor Pre-Driver

## Features and Benefits

- Drives 6 N-channel MOSFETs
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Hall element inputs
- PWM current limiting
- Dead time protection
- FG outputs
- Standby mode
- Lock detect protection
- Overvoltage protection

## Package: 32-contact QFN (suffix ET)



*Not to scale*

## Description

The A4936 is a complete 3-phase brushless DC motor pre-driver, supplying up to 28 V output for direct, high-current gate drive of an all N-channel power MOSFET 3-phase bridge. The device has three Hall-element inputs, a sequencer for commutation control, fixed off-time pulse width modulation (PWM) current control, and locked-rotor detection.

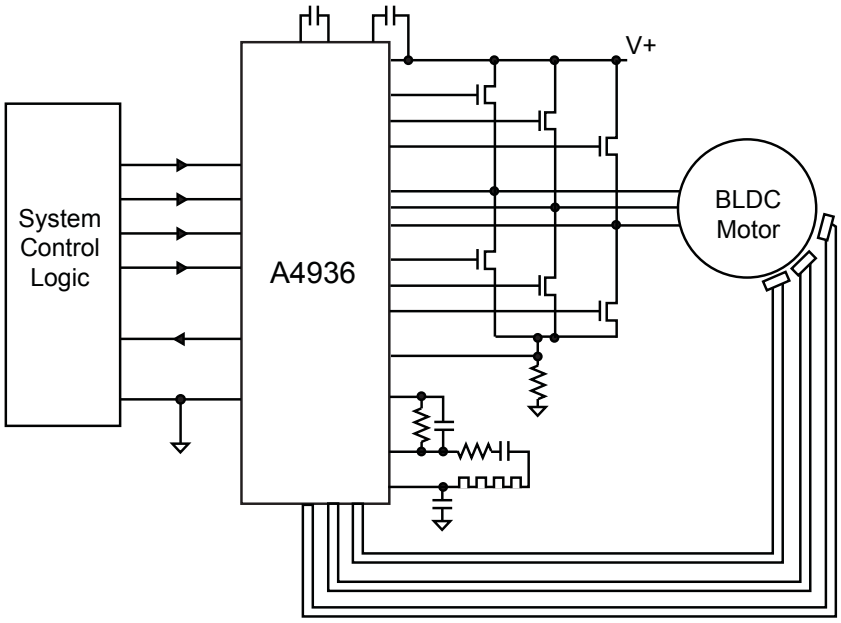
Output current is scaled by the capability of the external MOSFETs. Locked rotor detection delay is set by an external capacitor on the CLD terminal. The PWM, DIR, and BRAKE and STOP inputs can be used to control motor speed, position, and torque. Motor speed can be determined using the FG output from an FG coil amplifier and comparator.

The external MOSFETS can be PWMed using an external signal on the PWM input, or using the internal PWM current regulator. In either case, the A4936 synchronous rectification feature reduces power dissipation by turning-on the appropriate MOSFETs during current decay.

The Hall elements can be inexpensive types, when used with noise filtering to prevent false commutation signals. The A4936 provides a regulated 7.5 V supply to power the three Hall elements.

*Continued on the next page…*

## Typical Application Diagram



## Description (continued)

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage lockout, and dead time protection. Special power-up sequencing is not required. Operating temperature range is –20°C to 105°C.

The device package is a 32-contact, 5 mm × 5 mm, 0.90 mm nominal overall height QFN, with exposed pad for enhanced thermal dissipation. This small-footprint package is lead (Pb) free, with 100% matte tin leadframe plating.

## Selection Guide

| Part Number | Packing* | Package |
|---|---|---|
| A4936MET-T | 73 pieces per tube | 32-pin QFN, 5 mm × 5 mm, 0.90 mm nominal overall height |
| A4936METTR-T | 1500 pieces per reel | |

*Contact Allegro® for additional packing options

## Absolute Maximum Ratings

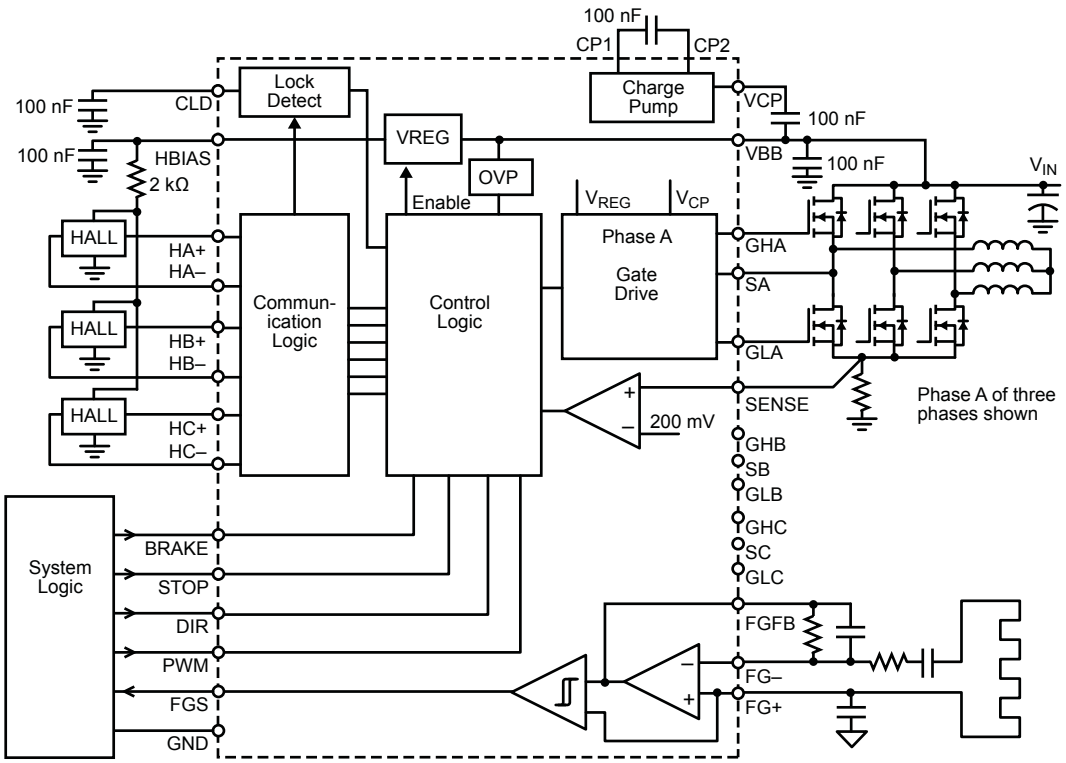
| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Load Supply Voltage | $V_{BB}$ | | 38 | V |
| Motor Phase Output | $S_x$ | $t_w$< 500 ns | –3 | V |
| Hall Input | $V_{Hx}$ | DC | –0.3 to 7 | V |
| Logic Input Voltage Range | $V_{IN}$ | | –0.3 to 7 | V |
| Ambient Operating Temperature | $T_A$ | Range M | –20 to 105 | °C |
| Maximum Junction Temperature | $T_J$(max) | | 150 | °C |
| Storage Temperature | $T_{stg}$ | | –40 to 150 | °C |

**Thermal Characteristics** may require derating at maximum conditions, see application information

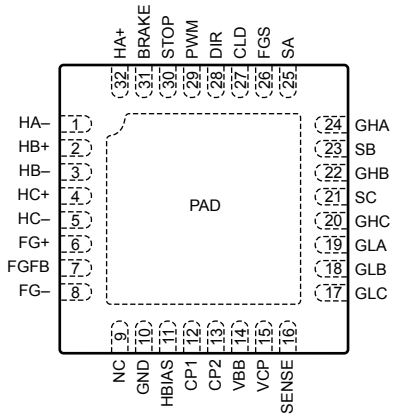
| Characteristic | Symbol | Test Conditions* | Value | Unit |
|---|---|---|---|---|
| Package Thermal Resistance (Junction to Ambient) | $R_{\theta JA}$ | On 4-layer PCB based on JEDEC standard | 32 | ºC/W |
| Package Thermal Resistance (Junction to Exposed Pad) | $R_{\theta JP}$ | | 2 | ºC/W |

*Additional thermal information available on the Allegro website

## Functional Block Diagram




## Pin-out Diagram




## Terminal List Table

| Number | Name | Function |
|---|---|---|
| 1 | HA- | Hall input A |
| 2 | HB+ | Hall input B |
| 3 | HB- | Hall input B |
| 4 | HC+ | Hall input C |
| 5 | HC- | Hall input C |
| 6 | FG+ | FG input |
| 7 | FGFB | FG amplifier feedback output |
| 8 | FG- | FG input |
| 9 | NC | No internal connection |
| 10 | GND | Ground |
| 11 | HBIAS | Hall bias power supply output |
| 12 | CP1 | Charge pump capacitor terminal |
| 13 | CP2 | Charge pump capacitor terminal |
| 14 | VBB | Supply voltage |
| 15 | VCP | Reservoir capacitor terminal |
| 16 | SENSE | Sense resistor connection |
| 17 | GLC | Low-side gate drive C |

| Number | Name | Function |
|---|---|---|
| 18 | GLB | Low-side gate drive B |
| 19 | GLA | Low-side gate drive A |
| 20 | GHC | High-side gate drive C |
| 21 | SC | High-side source connection C |
| 22 | GHB | High-side gate drive B |
| 23 | SB | High-side source connection B |
| 24 | GHA | High-side gate drive A |
| 25 | SA | High-side source connection A |
| 26 | FGS | FG output |
| 27 | CLD | Locked rotor detect timing capacitor |
| 28 | DIR | Logic input: motor direction |
| 29 | PWM | Logic input: external PWM control |
| 30 | STOP | Logic input: output disable |
| 31 | BRAKE | Logic input: motor brake |
| 32 | HA+ | Hall input A |
| – | PAD | Exposed Thermal Pad |

**ELECTRICAL CHARACTERISTICS**[1,2] Valid at $T_A$ = 25°C, $V_{IN}$ = 24 V; unless otherwise noted

| Characteristics | Symbol | Test Conditions | Min. | Typ.[3] | Max. | Unit |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| Supply Voltage Range | $V_{BB}$ | Operating | 8.5 | – | $V_{BBOV}$ | V |
| Motor Supply Current | $I_{BB}$ | $f_{PWM}$ < 30 kHz, $C_{LOAD}$ = 1000 pF | – | 5.1 | 6.5 | mA |
| | | Standby mode | – | 3 | 4 | mA |
| HBIAS | $V_{HBIAS}$ | 0 mA ≤ $I_{HBIAS}$ ≤ 24 mA | 7.2 | 7.5 | 7.8 | V |
| HBIAS Current Limit | $I_{HBIASlim}$ | | 30 | – | – | mA |
| **Control Logic** | | | | | | |
| Logic Input Voltage | $V_{IN(1)}$ | | 2 | – | – | V |
| | $V_{IN(0)}$ | | – | – | 0.8 | V |
| Logic Input Current | $I_{IN(1)}$ | $V_{IN}$ = 2 V | –1.0 | <1.0 | 1.0 | µA |
| | $I_{IN(0)}$ | $V_{IN}$ = 0.8 V | –1.0 | <–1.0 | 1.0 | µA |
| Input Pin Glitch Reject | $t_{GLITCH}$ | PWM pin | 350 | 500 | 650 | ns |
| | | DIR, BRAKE, and STOP pins | 700 | 1000 | 1300 | ns |
| HBIAS Wake-up Delay, Standby Mode | $t_{dHBIAS}$ | $C_{HBIAS}$ = 0.1 µF | – | 15 | 25 | µs |
| **Gate Drive** | | | | | | |
| High-Side Gate Drive Output | $V_{GS(H)}$ | Relative to $V_{BB}$, $I_{GATE}$ = 2 mA | 7 | – | – | V |
| Low-Side Gate Drive Output | $V_{GS(L)}$ | $I_{GATE}$ = 2 mA | 7 | – | – | V |
| Gate Drive Current (Sourcing) | $I_{GATE}$ | GHx = GLx = 4 V | 20 | 30 | – | mA |
| Gate Drive Pull-Down Resistance | $R_{GATE}$ | | 10 | 28 | 40 | Ω |
| Dead Time | $t_{DEAD}$ | | 700 | 1000 | 1300 | ns |
| Current Limit Input Threshold | $V_{REF}$ | | 180 | 200 | 220 | mV |
| Fixed Off-Time | $t_{OFF}$ | | 18 | 25 | 37 | µs |
| **Protection** | | | | | | |
| Thermal Shutdown Temperature | $T_{JTSD}$ | | 155 | 170 | 185 | °C |
| Thermal Shutdown Hysteresis | $T_{JTSDhys}$ | | – | 20 | – | °C |
| VBB UVLO Enable Threshold | $V_{BBUV}$ | Rising $V_{BB}$ | 6.2 | 7 | 7.85 | V |
| VBB UVLO Hysteresis | $V_{BBUVhys}$ | | 0.4 | 0.75 | 1 | V |
| VCP UVLO | $V_{CPUV}$ | Relative to $V_{BB}$, VCP falling | 4.6 | – | 6 | V |
| Lock Detect Duration | $t_{lock}$ | C = 0.1 µF | 1.5 | 2 | 2.5 | s |
| VBB Overvoltage Threshold | $V_{BBOV}$ | Rising $V_{BB}$ | 30 | 33 | 37.5 | V |
| **Hall Logic** | | | | | | |
| Hall Input Current | $I_{HALL}$ | $V_{IN}$ = 0.2 to 3.5 V | –1 | 0 | 1 | µA |
| Common Mode Input Range | $V_{CMR}$ | | 0.2 | – | 3.5 | V |
| AC Input Voltage Range | $V_{HALL}$ | | 60 | – | – | $mV_{p-p}$ |
| Hall Thresholds | $V_{th}$ | Difference between Hall inputs at transitions | – | +10, –10 | – | mV |
| Hall Threshold Hysteresis | $V_{HYS}$ | $T_J$ = 25°C | 10 | 20 | 30 | mV |
| | | $T_J$ = –20°C to 125°C | 5 | 20 | 40 | mV |
| Pulse Reject Filter | $t_{pulse}$ | | – | 2 | – | µs |

*Continued on the next page…*

**ELECTRICAL CHARACTERISTICS**[1,2] (continued) Valid at $T_A$ = 25°C, $V_{IN}$ = 24 V; unless otherwise noted

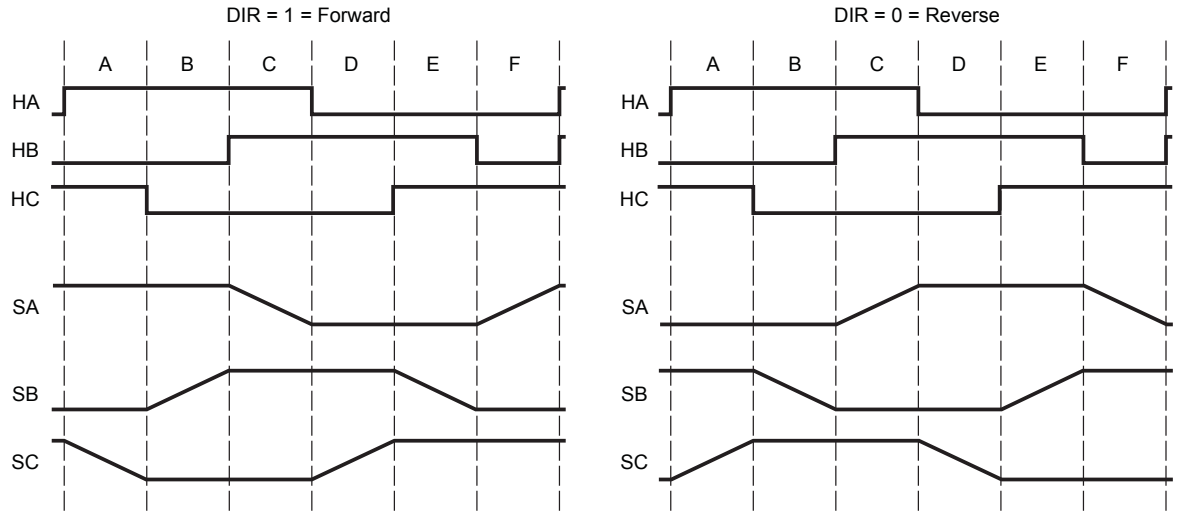
| Characteristics | Symbol | Test Conditions | Min. | Typ.[3] | Max. | Unit |
|---|---|---|---|---|---|---|
| **FG** | | | | | | |
| FG Input Bias Current | $I_{BFG}$ | | –1 | – | 1 | µA |
| FG Input Offset Voltage | $V_{OSFG}$ | | –15 | – | 15 | mV |
| FGS Output High Leakage | $I_{OH}$ | $V_{OH}$ = 5 V | –1 | – | 1 | µA |
| FGS Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 2 mA | – | 0.2 | 0.4 | V |
| FG Amp Open Loop Gain | $A_{FG}$ | | 45 | 60 | – | dB |
| FG Amp Bias Voltage | $V_{BFG}$ | | 2.2 | 2.5 | 2.8 | V |
| FG Comparator Hysteresis | $V_{FGhys}$ | | 40 | 110 | 160 | mV |

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2]Specifications throughout the allowed operating temperature range are guaranteed by design and characterization.
[3]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

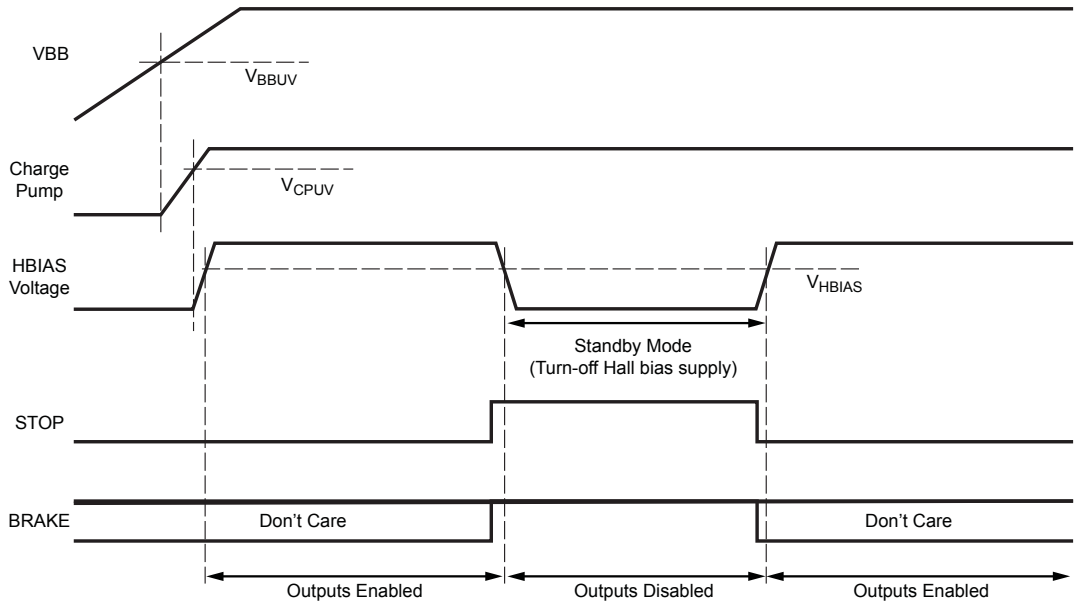
**Logic States Table*** (See timing charts, below)

| Condition | | HA | HB | HC | DIR | STOP | BRAKE | PWM | GHA | GLA | GHB | GLB | GHC | GLC | SA | SB | SC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Forward | A | + | – | + | 1 | 0 | 0 | 1 | HI | LO | LO | HI | LO | LO | HI | LO | Z |
| | B | + | – | – | 1 | 0 | 0 | 1 | HI | LO | LO | LO | LO | HI | HI | Z | LO |
| | C | + | + | – | 1 | 0 | 0 | 1 | LO | LO | HI | LO | LO | HI | Z | HI | LO |
| | D | – | + | – | 1 | 0 | 0 | 1 | LO | HI | HI | LO | LO | LO | LO | HI | Z |
| | E | – | + | + | 1 | 0 | 0 | 1 | LO | HI | LO | LO | HI | LO | LO | Z | HI |
| | F | – | – | + | 1 | 0 | 0 | 1 | LO | LO | LO | HI | HI | LO | Z | LO | HI |
| Reverse | A | + | – | + | 0 | 0 | 0 | 1 | LO | HI | HI | LO | LO | LO | LO | HI | Z |
| | B | + | – | – | 0 | 0 | 0 | 1 | LO | HI | LO | LO | HI | LO | LO | Z | HI |
| | C | + | + | – | 0 | 0 | 0 | 1 | LO | LO | LO | HI | HI | LO | Z | LO | HI |
| | D | – | + | – | 0 | 0 | 0 | 1 | HI | LO | LO | HI | LO | LO | HI | LO | Z |
| | E | – | + | + | 0 | 0 | 0 | 1 | HI | LO | LO | LO | LO | HI | HI | Z | LO |
| | F | – | – | + | 0 | 0 | 0 | 1 | LO | LO | HI | LO | LO | HI | Z | HI | LO |
| Fault | | – | – | – | X | X | X | X | LO | LO | LO | LO | LO | LO | Z | Z | Z |
| | | + | + | + | X | X | X | X | LO | LO | LO | LO | LO | LO | Z | Z | Z |
| Brake | | X | X | X | X | 0 | 1 | X | LO | HI | LO | HI | LO | HI | LO | LO | LO |
| Coast | | X | X | X | X | 1 | 0 | X | LO | LO | LO | LO | LO | LO | Z | Z | Z |
| Standby | | X | X | X | X | 1 | 1 | X | LO | LO | LO | LO | LO | LO | Z | Z | Z |

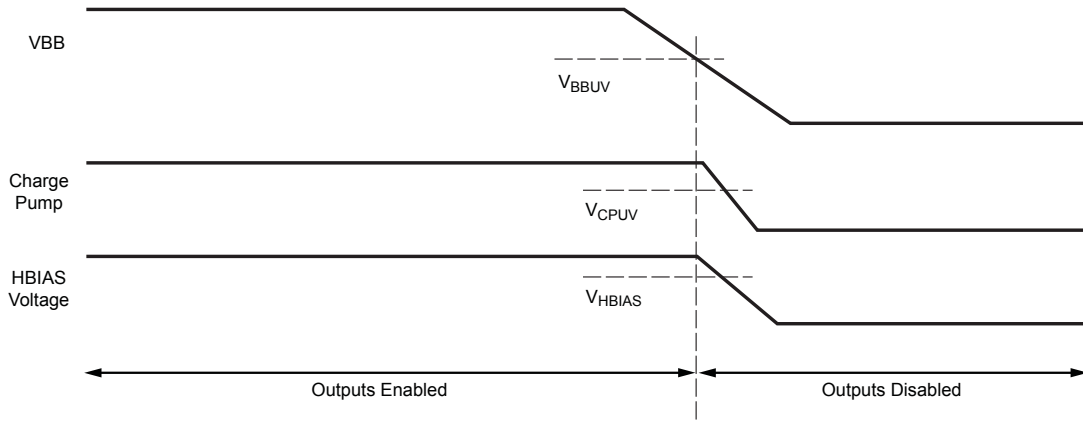
*X = Don't care (can be 1 or 0), Z = High impedance



**Power-Up and Standby Mode Timing Diagram**




**Power-Down Timing Diagram**



## Functional Description

**Current Regulation** Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the full bridge are turned on, current increases in the motor winding until it reaches a value, $I_{TRIP}$ , given by:

$$I_{TRIP} = 200 \text{ mV} / R_{SENSE}$$

When $I_{TRIP}$ is reached, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for the fixed off-time period.

**PWM Logic** The PWM input terminal allows external PWM. PWM high turns on the selected sink-source pair. PWM low switches off the appropriate drivers and the load current decays. If PWM is held high, the current will rise until it reaches the level set by the internal current control circuit. Typically PWM frequency is in the 20 to 30 kHz range. The PWM logic is summarized in the following table:

| PWM | Outputs | Outputs State |
|---|---|---|
| 1 | On | Drive |
| 0 | Source chopped | Slow decay with synchronous rectification |

**Fixed Off-Time** The A4936 fixed off-time is set to 25 µs, nominal.

**PWM Blank Timer** When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes as well as switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source enable latch, the sense comparator is blanked. The blanking timer runs after the off-time counter completes, in order to provide the blanking function. The blanking timer is reset when PWM is low or DIR is changed. With external PWM control, a DIR change or a PWM-on triggers the blanking function. The duration is fixed at 1.5 µs.

**Synchronous Rectification** When a PWM-off cycle is triggered, either by a low input on PWM or by an internal fixed off-time cycle, load current recirculates. The A4936 synchronous rectification feature turns-on the appropriate MOSFETs during the current decay, and effectively shorts-out the body diodes with the low $R_{DS(on)}$ driver. This lowers power dissipation significantly and can eliminate the need for external Schottky diodes.

**Run Mode** The motor phases are only energized when the STOP input is low. When the STOP input is high, all MOSFETs are held in the off state and the phase connections to the motor are high impedance. In this state a running motor will coast to stop. The STOP input overrides the PWM input. When STOP is high and BRAKE is high, the A4936 enters Standby mode.

**Brake Mode** A logic high on the BRAKE pin activates Brake mode. A logic low allows normal operation. Braking turns on all three sink drivers, effectively shorting out the motor-generated BEMF. The BRAKE input overrides the PWM input and also the Lock Detect function. The STOP input must be low for Brake mode to operate.

It is important to note that the internal PWM current control circuit does not limit the current when braking, because the current does not flow through the sense resistor. The maximum current can be approximated by $V_{BEMF} / R_{LOAD}$. Care should be taken to insure that the maximum ratings of the A4396 are not exceeded in the worse case braking situation of high speed and high inertial load.

**Standby Mode** The reduced power Standby mode is provided to reduce current consumption when the motor is not required to be driven. The Hall bias supply and the charge pump are disabled and all MOSFETs are turned-off. The A4936 enters Standby mode when STOP and BRAKE are held high together. All other control inputs are ignored when in Standby mode.

**HBIAS Function** This provides a power supply of 7.5 V, current-limited to 30 mA. This reference voltage is used to power the logic sections of the A4936 and also to power the external Hall elements.

**Charge Pump** The internal charge pump is used to generate a supply above VBB to drive the high-side MOSFETs. The voltage on the VCP pin is internally monitored, and in case of a fault condition, the outputs of the device are disabled.

**Fault Shutdown** In the event of a fault due to excessive junction temperature or due to low voltage on VCP or VBB, the outputs of the device are disabled until the fault condition is removed. At power-up the UVLO circuit disables the drivers.

**Overvoltage Protection** VBB is monitored to determine if a hazardous voltage is present due to the motor generator pumping up the supply bus. When the voltage exceeds $V_{BBOV}$ , the synchronous rectification feature is disabled.

**Overtemperature Protection** If die temperature exceeds approximately 165°C, the Thermal Shutdown function will disable the outputs until the internal temperature falls below the threshold, by the hysteresis.

**Lock Detect Function** The A4936 monitors the Hall inputs and the control inputs to determine if a locked rotor condition is present. A locked rotor is determined to be present under either of these two different conditions:

- The Hall inputs are not consistently changing.
- The proper commutation sequence is not being followed. The motor can be locked in a condition in which it toggles between two specific Hall device states.

If there are no Hall input changes within the lock time, $t_{lock}$ , or the Hall inputs toggle between two adjacent states for longer then $t_{lock}$ , then the outputs are disabled, and the fault is latched.

The fault remains latched until cleared by any one of the following actions:

- Rising or falling edge on the DIR pin.
- VBB UVLO threshold exceeded (during power-up cycle).
- PWM pin held low for > $t_{lock}$ / 2.

The lock time, $t_{lock}$ , is set by a capacitor connected to the CLD pin. CLD produces a triangle waveform (1.67 V peak-to-peak) with frequency linearly related to the capacitor value. $t_{lock}$ is defined as 127 cycles of this triangle waveform, or:

$$t_{lock} = CLD \times 20$$

where:

$t_{lock}$ is the lock time in µs, and

CLD is the value of the capacitor in µF.

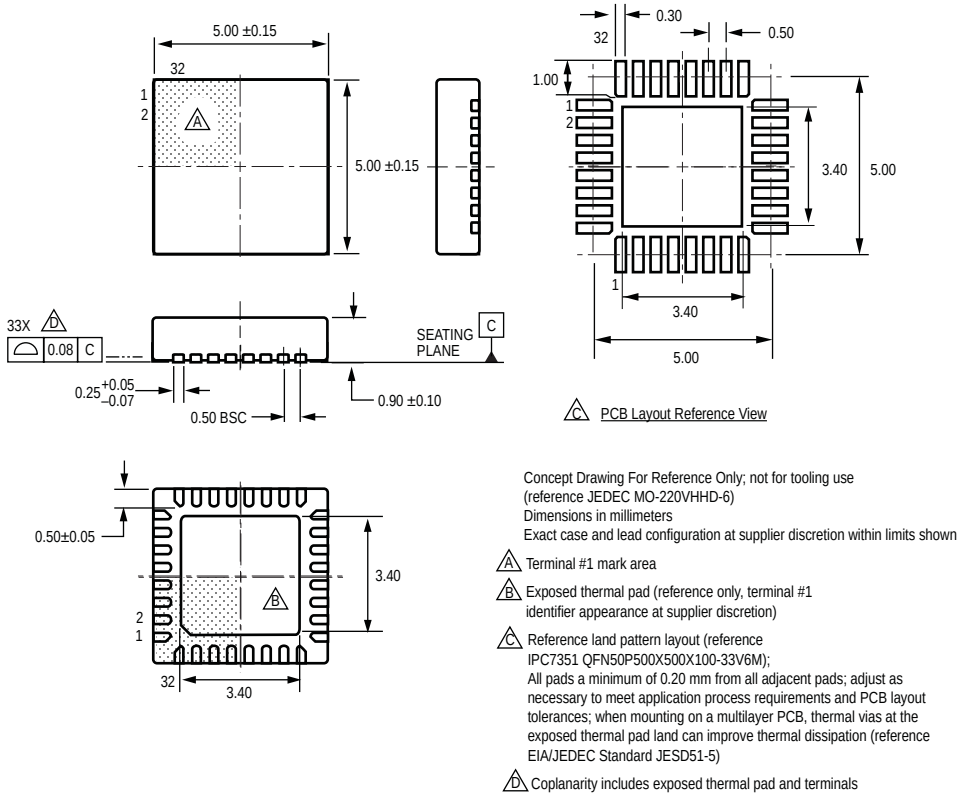
The Lock Detect function is disabled by connecting CLD to GND.

When BRAKE is high, lock detection is disabled. It also is disabled if the PWM input remains low for the duration of the Hall input lock detection.

**FG Amplifier and Comparator** A differential amplifier and a comparator are integrated into the A4936 to amplify and shape the FG signal from the FG coil underneath the motor. This coil is typically created with a copper PCB trace, and as the motor spins, the coil creates a low amplitude sinusoidal voltage with a frequency proportional to the motor speed.

The FG input differential amplifier is biased at 2.5 V, and the gain is set by the impedance between the FGFB pin and the FG– input. This amplified signal is then compared to 2.5 V to create the FGS output signal. The recommended value for the gain setting feedback resistor is 50 to 500 kΩ. The recommended value for the capacitor between FB+ and GND is 10 nF to 10 µF.

## Package ET 32-Contact QFN




Concept Drawing For Reference Only; not for tooling use
(reference JEDEC MO-220VHHD-6)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals



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