MM74HC574

3-State Octal D-Type Edge-Triggered Flip-Flop

The MM74HC574 high speed octal D−type flip−flops utilize advanced silicon−gate P−well CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS−TTL loads. Due to the large output drive capability and the 3−STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip−flops. Data at the D inputs, meeting the set−up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 18 ns
- Wide Operating Voltage Range: 2 V – 6 V
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum
- Compatible with Bus−oriented Systems
- Output Drive Capability: 15 LS−TTL Loads

MAXIMUM RATINGS (Note 1)

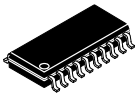
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to + 7.0 V	V
DC Input Voltage	V_{IN}	−1.5 to V_{CC} + 1.5 V	V
DC Output Voltage	V_{OUT}	−0.5 to V_{CC} + 0.5 V	V
Clamp Diode Current	I_{IK}, I_{OK}	±20	mA
DC Output Current, per pin	I_{OUT}	±35	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±70	mA
Storage Temperature Range	T_{STG}	−65 to +150	°C
Power Dissipation (Note 2) S.O. Package only	P_D	600 500	mW
Lead Temperature (Soldering 10 s)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

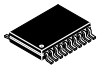
1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: − 12 mW/°C from 65°C to 85°C.

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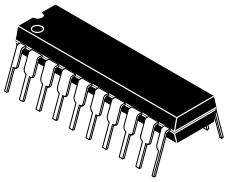
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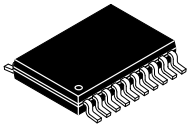
SOP20
SJ SUFFIX
CASE 565BG



TSSOP20
MTC SUFFIX
CASE 948AQ



PDIP20
N SUFFIX
CASE 646AC



SOIC20
WM SUFFIX
CASE 751BJ

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

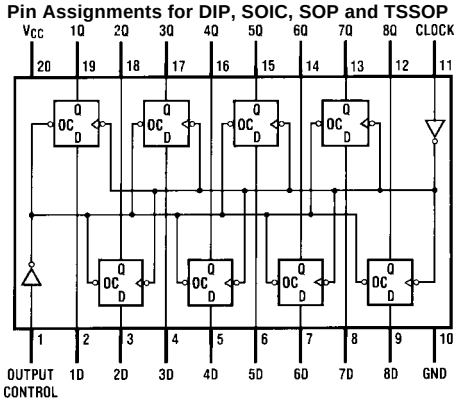
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ORDERING CODE

Order Number	Package Number	Package Description
MM74HC574WM	M20B	20−Lead Small Outline Integrated Circuit (SOIC), JEDEC MS−013, 0.300″ Wide
MM74HC574SJ	M20D	20−Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3 mm Wide
MM74HC574MTC	MTC20	20−Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO−153, 4.4 mm Wide
MM74HC574N	N20A	20−Lead Plastic Dual−In−Line Package (PDIP), JEDEC MS−001, 0.300″ Wide

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Transition from Low−to−HIGH
Z = High Impedance State
Q0 = The level of the output before steady state input conditions were established

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristic		Min	Typ	Max	Units
V_{CC}	Supply Voltage		2		6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage		0		V_{CC}	V
T_A	Operating Temperature Range		−55		+125	°C
t_r, t_f	Input Rise or Fall Times	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V			1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 3)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0 V 4.5 V 6.0 V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0 V 4.5 V 6.0 V		0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0 V 4.5 V 6.0 V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA $\|I_{OUT}\| \le 7.8$ mA	4.5 V 6.0 V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0 V 4.5 V 6.0 V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA $\|I_{OUT}\| \le 7.8$ mA	4.5 V 6.0 V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0 V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3−STATE Output Leakage Current	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0 V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0 V		8.0	80	160	μA
ΔI_{CC}	Quiescent Supply Current per Input Pin	V_{CC} = 5.5 V V_{IN} = 2.4 V or 0.4 V (Note 3)	OE	1.0	1.5	1.8	2.0	mA
			CLK	0.6	0.8	1.0	1.1	
			DATA	0.4	0.5	0.6	0.7	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. For a power supply of 5 V ±10% the worst−case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst−case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst−case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, t_r = t_f = 6 ns)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		60	33	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	C_L = 45 pF	17	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ, C_L = 45 pF	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ, C_L = 5 pF	14	25	ns
t_S	Minimum Setup Time, Data to Clock		10	12	ns
t_H	Minimum Hold Time, Clock to Data		−3	5	ns
t_W	Minimum Pulse Clock Width		8	15	ns

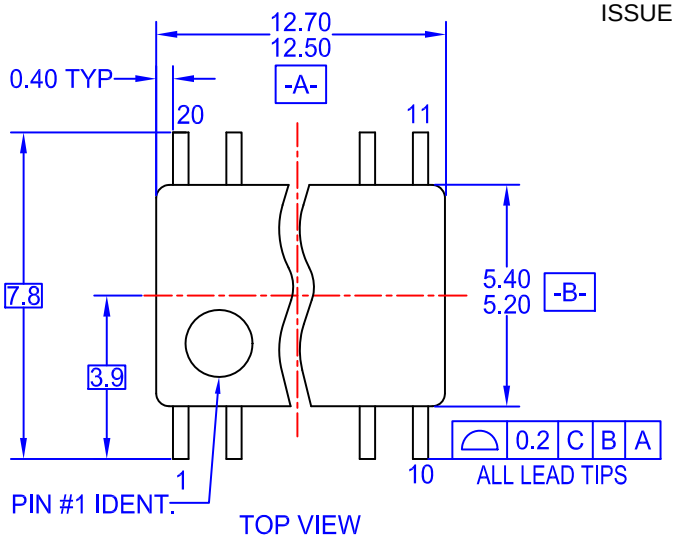
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.0 − 6.0 V, C_L = 50 pF, $t_r = t_f$ = 6 ns unless otherwise specified)

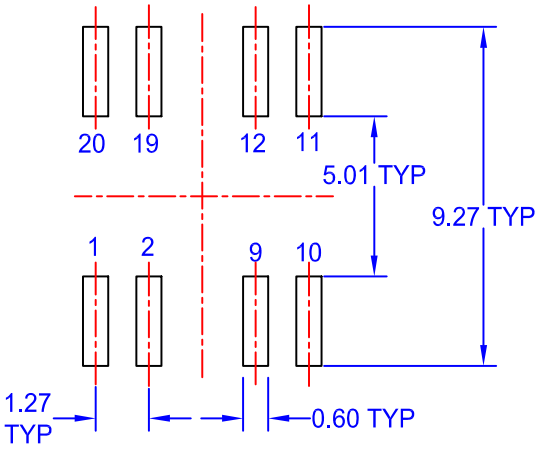
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	C_L = 50 pF	2.0 V 4.5 V 6.0 V		33 30 35	28 24 28	23 20 23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	C_L = 50 pF C_L = 150 pF	2.0 V 2.0 V	18 51	30 155	38 194	45 233	ns
		C_L = 50 pF C_L = 150 pF	4.5 V 4.5 V	13 19	23 31	29 47	35 47	ns
		C_L = 50 pF C_L = 150 pF	6.0 V 6.0 V	12 18	20 27	25 34	30 41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 50 pF C_L = 150 pF	 2.0 V 2.0 V	 22 59	 30 180	 38 225	 45 270	ns
		C_L = 50 pF C_L = 150 pF	4.5 V 4.5 V	14 20	28 36	35 45	42 54	ns
		C_L = 50 pF C_L = 150 pF	6.0 V 6.0 V	12 18	24 31	30 39	36 47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0 V 4.5 V 6.0 V	15 12 10	30 25 21	38 31 27	45 38 32	ns
t_S	Minimum Setup Time Data to Clock		2.0 V 4.5 V 6.0 V	6	12 20 17	15 25 21	18 30 25	ns
t_H	Minimum Hold Time Clock to Data		2.0 V 4.5 V 6.0 V	−1	5 0 0	6 0 0	8 0 0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0 V 4.5 V 6.0 V	6 7 6	12 12 10	15 15 13	18 18 15	ns
t_W	Minimum Clock Pulse Width		2.0 V 4.5 V 6.0 V	30 9 8	15 16 14	20 20 18	24 24 20	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time		2.0 V 4.5 V 6.0 V		1000 500 400	1000 500 400	1000 500 400	ns
C_{PD}		OC = V_{CC} OC = GND		5 58				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

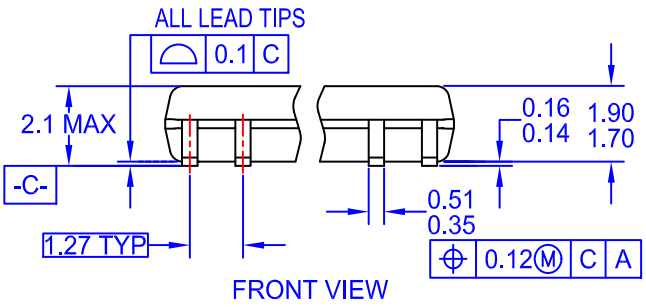
4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

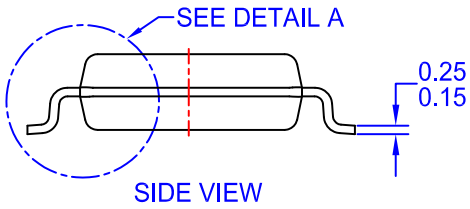
PACKAGE DIMENSIONS

SOP20
CASE 565BG
ISSUE O



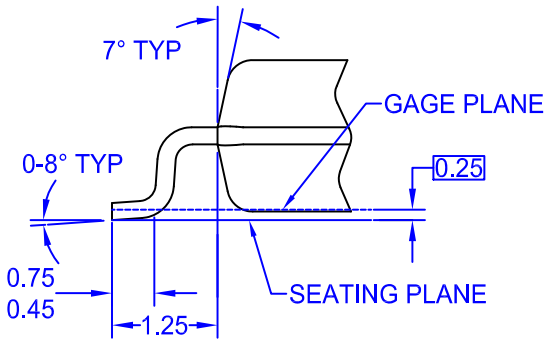






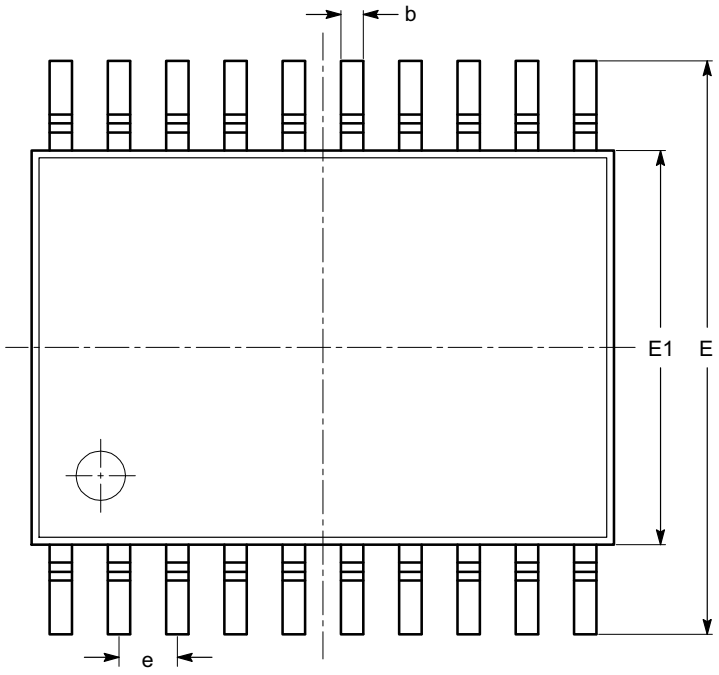
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



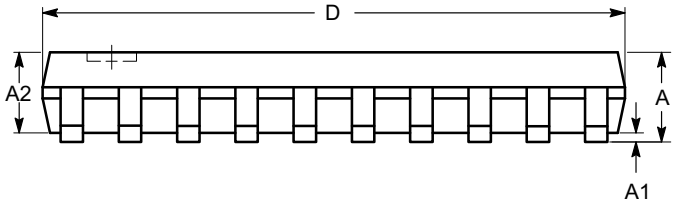
PACKAGE DIMENSIONS

TSSOP20, 4.4x6.5
CASE 948AQ−01
ISSUE A

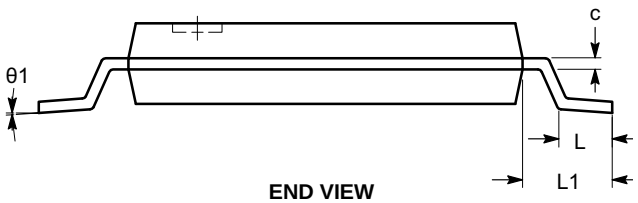


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW

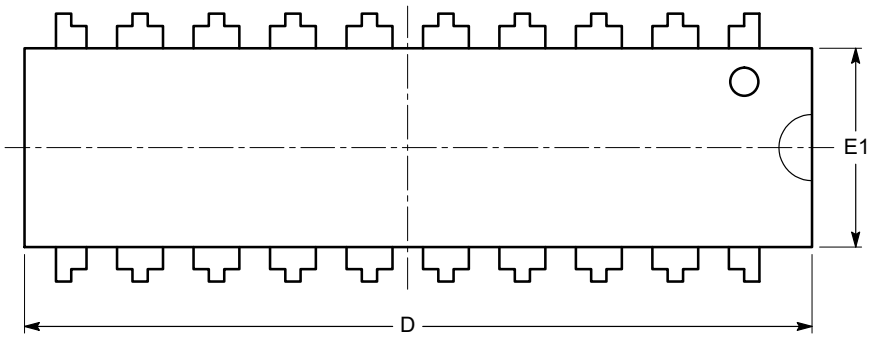


END VIEW

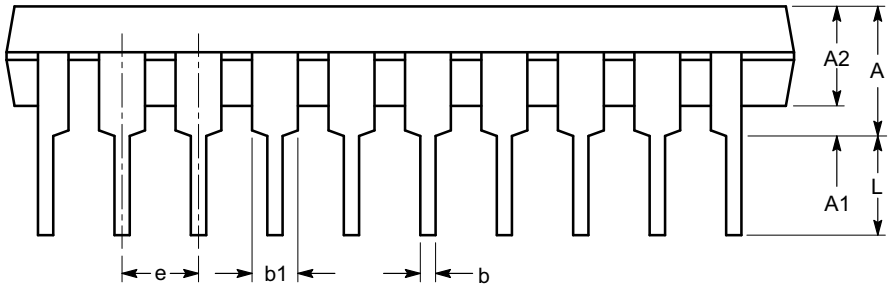
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

PACKAGE DIMENSIONS

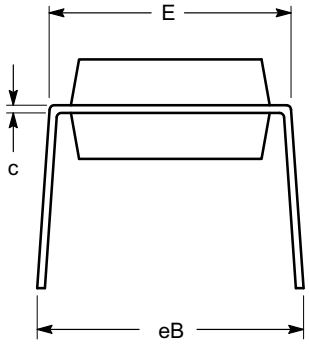
PDIP−20, 300 mils
CASE 646AC−01
ISSUE A



TOP VIEW



SIDE VIEW



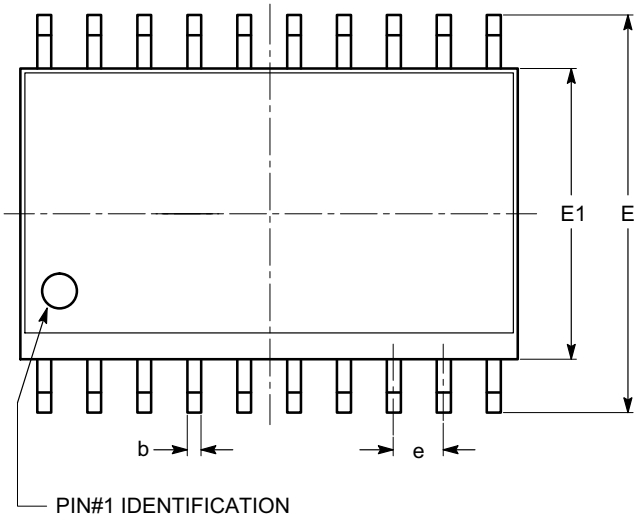
END VIEW

SYMBOL	MIN	NOM	MAX
A	3.56		5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.45	0.55
b1	1.15	1.52	1.77
c	0.21	0.26	0.35
D	24.89	26.16	26.92
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.88		10.92
L	2.99	3.30	3.81

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

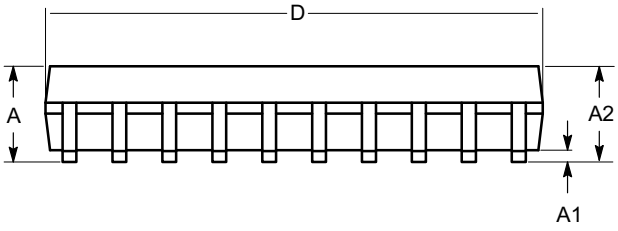
PACKAGE DIMENSIONS

SOIC−20, 300 mils
CASE 751BJ−01
ISSUE O

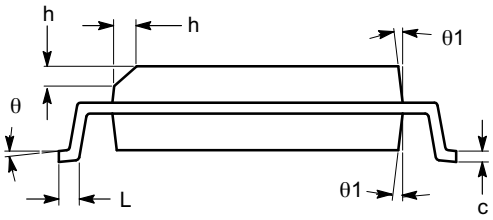


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.36	2.49	2.64
A1	0.10		0.30
A2	2.05		2.55
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	12.60	12.80	13.00
E	10.01	10.30	10.64
E1	7.40	7.50	7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40	0.81	1.27
θ	0º		8º
θ1	5º		15º



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

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