RDA012M4MS

12 Bit 1.3 GS/s Master-Slave 4:1 MUXDAC

Features

- 12 Bit Resolution
- 1.3 GS/s Sampling Rate
- 4:1 Input Multiplexer
- Master-Slave Operation for Synchronous Operation of Multiple Devices
- Differential Analog Output
- Input Code Format: Offset Binary
- Output Swing: 600 mV with 50 Ω Termination
- 3.3V NMOS-Compatible Data Inputs
- Differential ECL or Sinusoidal Clock Input
- LVDS Compatible Clock Output
- 10 Bit Static Linearity
- Reference Output/Input Pin for Accurate Full-Scale Adjustment.
- 3.3V and -5.2V Power Supply
- 77 Lead HSD Package

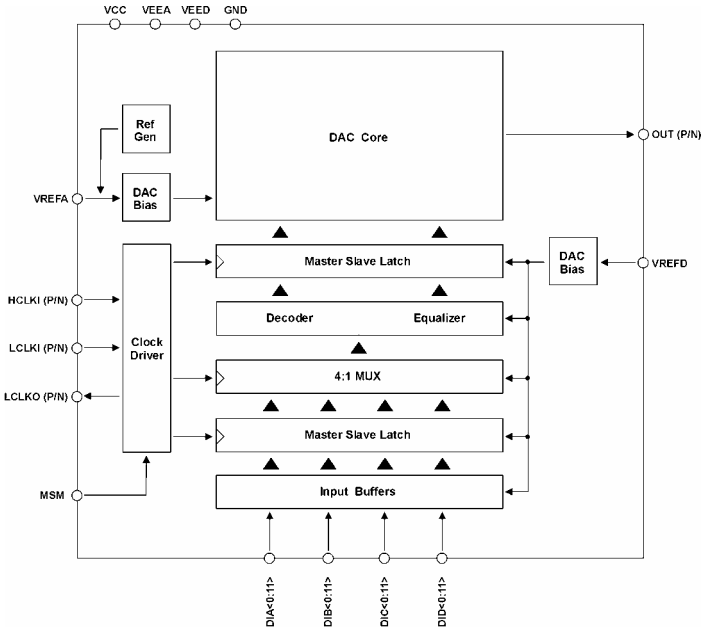

Figure 1 - Functional Block Diagram

Product Description

The RDA012M4MS is a digital-to-analog converter (DAC) with a 4:1 input multiplexer and a maximum update rate of 1.3GS/s. The RDA012M4MS features master-slave operation that simplifies synchronization when multiple devices are required, such as in an I-Q modulation scheme. The integrated DAC utilizes a segmented current source to reduce the glitch energy and achieve high linearity performance. For best dynamic performance, the DAC outputs are internally terminated with 50Ω resistance, and outputs a nominal full-scale current of 12mA when terminated with external 50Ω resistors. For a convenient interface with most CMOS ICs, the digital data inputs are low voltage NMOS compatible.

Ordering information

PART NUMBER	DESCRIPTION
RDA012M4MS-DI	12 BIT 4:1 MUX 1.3GS/s DAC, DIE
RDA012M4MS-HD	12 BIT 4:1 MUX 1.3GS/s DAC, HSD Package
EVRDA012M4MS-HD	RDA012M4MS-HD Evaluation Board

Absolute Maximum Ratings

Supply Voltages

Between GNDs ..... -0.3V to +0.3V
Between VCCs ..... -0.3V to +0.3V
VCCs to GND ..... 0V to +3.8V

RF Input Voltages

CLKIP, CLKIN to GND ..... 0V to VCC

HS Digital Input Voltages

DI<0:11> ..... 0V to VCC

Output Termination Voltages

DOUTP, DOUTN to GND .....0V to VCC

Temperature

Operating Temperature.....-30 to +100 °C
Case Temperature..... -15 to +85 °C
Junction Temperature..... +120 °C
Lead, Soldering (10 Seconds) ..... +220 °C
Storage..... -40 to 125 °C

Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
ACCURACY							
Differential Nonlinearity	DNL		2		±2		LSB
Integral Nonlinearity	INL		2		±2.5		LSB
DYNAMIC PERFORMANCE							
Spurious Free Dynamic Range	SFDR1	F_{clk} = 800MHz , F_{out} = 267MHz	1		56		dBc
	SFDR2	F_{clk} = 1000MHz , F_{out} = 333MHz	1		53		dBc
	SFDR3	F_{clk} = 1300MHz , F_{out} = 400MHz	1		50		dBc
Signal Noise Ratio	SNDR						dB
Clock Feedthrough	FD						dB
ANALOG SIGNAL OUTPUT (OUTP, OUTN)							
Full-scale Output Range	V_{FSS}	Single Ended, 50Ω Termination to Ground	2	570	600	630	mV_{p-p}
Full-scale Output Range	V_{FSRS}	Single Ended, 50Ω Termination to Ground (MIN=000h, MAX=FFFh)		-650		0	mV
Full-scale output swing	V_{FSD}	Differential with 50Ω Termination to Ground on each output	2	1140	1200	1260	mV_{p-p}
Output current	I_{OUT}		3		12		mA
Rise Time	$T_{R,OUT}$	20%-80% with FSR output					ps
Fall Time	$T_{F,OUT}$	20%-80% with FSR output					ps
Settling Time	T_{SETTL}						ps
CORE CLOCK INPUT (HCLKIP, HCLKIN)							
Amplitude	$V_{CPP,HCLKI}$	Differential ECL	1	400	600	800	mVpp
Common Mode Voltage	$V_{CM,HCLKI}$		1	-0.8	-1.5	-2.0	V
Input Resistance	R_{HCLKI}		3	45	50	55	Ω
Input Capacitance	C_{HCLKI}						fF
Maximum Frequency	$F_{MAX,HCLKI}$		3	1300			MHz
Minimum Frequency	$F_{MIN,HCLKI}$		3			1	MHz
CLOCK INPUT (LCLKIP, LCLKIN)							
Amplitude	$V_{CPP,LCLKI}$	Differential LVDS	2	250	350	450	mVpp
Common Mode Voltage	$V_{CM,LCLKI}$		2	0.9	1.2	1.5	mV
Input Resistance	R_{LCLKI}		3		100		Ω
Maximum Frequency	$F_{MAX,LCLKI}$		3	325			MHz
Minimum Frequency	$F_{MIN,LCLKI}$		3			0.25	MHz
CLOCK OUPUT (LCLKOP, LCLKON)							
Amplitude	$V_{CPP,LCLKO}$		2	250	350	450	mVpp
Common Mode Voltage	$V_{CM,LCLKO}$		2	0.9	1.2	1.5	mV
Maximum Frequency	$F_{MAX,LCLKO}$		3	325			MHz
Minimum Frequency	$F_{MIN,LCLKO}$		3			0.25	MHz
DIGITAL INPUTS (A<0:11>, B<0:11>, C<0:11>, D<0:11>)							
Input High Voltage	V_{IH}		2	0.9		VCC	V
Input Low Voltage	V_{IL}		2	-0.4		0.4	V
Input Resistance	R_{DIN}						Ω
Setup Time	$t_{ST,DTHCK}$	From data input to LCLKO	3	300			ps
Hold Time	$t_{HL,DTHCK}$	From LCLKO to data input	3	-50			ps

Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
TERMINATION (VTT)							
HCLKI Termination Voltage	VTT				-2.0		V
REFERENCE (VREFA, VREFD)							
Analog Reference	VREFA	Internally generated	3	-1.9	-2.0	-2.1	V
Digital Reference	VREFD	Internally generated	3	-1.9	-2.0	-2.1	V
Input Resistance	R_{VREF}	For externally driven VREFA, VREFD	3	500	560	620	Ω
POWER SUPPLY							
Positive Supply	VCC			3.1	3.3	3.5	V
Negative Supply, Analog	VEEA			-5.4	-5.2	-5.0	V
Negative Supply, Digital	VEED			-5.4	-5.2	-5.0	V
Power Dissipation	P	Total dissipation			3300		mW
Power Dissipation	P_{VCC}	Positive supply			500		mW
Power Dissipation	P_{VEEA}	Negative supply, analog			500		mW
Power Dissipation	P_{VEED}	Negative supply, digital			2300		mW
OPERATING RANGE							
Ambient Temperature	T_A						°C
Junction Temperature	T_J				120		°C

Test Levels

TEST LEVEL	TEST PROCEDURE
1	100% production tested at T_A = 25C[1,2]
2	Sample tested at T_A = 25C unless other temperature is specified[1]
3	Guaranteed by design and/or characterization testing

[1] All tests are continuous, not pulsed. Therefore, Tj (junction temperature) > Tc (case temperature) > Ta (ambient temperature). This is the normal operating condition and is more stressful than a pulsed test condition.

[2] The tests are conducted with the power set to VCC_{MIN} and to VCC_{MAX}.

Pin Description

P/I/O	PIN	NUM.	NAME	FUNCTION
P	7, 14, 39, 62	4	VCC	+3.3V Digital Power Supply
P	68, 71, 72, 73, 74, 75, 76	7	VEEA	-5.2V Analog Power Supply
P	8, 12, 26, 52, 64, 67	6	VEED	-5.2V Digital Power Supply
P	Bottom Plate	-	GND	Ground
I	77	1	VREFA	-2V Reference Voltage
I	10	1	VREFD	Digital Circuitry Bias Reference. Bypass to Ground
I	4	1	VTT	HCLKI Clock Termination Voltage
I	6	1	MSM	Master-Slave Mode Selection: Float - Master GND - Slave
I	5	1	HCLKIP	Clock Input
I	3	1	HCLKIN	
I	24	1	LCLKIP	Low Clock Input
I	25	1	LCLKIN	
I	2	1	LCLKOP	Low Clock Output
I	1	1	LCLKON	
I	9, 16, 20, 27, 31, 35, 40, 44, 48, 53, 57, 61	12	DIA<0:11>	DIA<i> Is Channel A Digital Bit i Input. MSB is bit 11
I	11, 17, 21, 28, 32, 36, 41, 45, 49, 54, 58, 63	12	DIB<0:11>	DIB<i> Is Channel B Digital Bit i Input. MSB is bit 11
I	13, 18, 22, 29, 33, 37, 42, 46, 50, 55, 59, 65	12	DIC<0:11>	DIC<i> Is Channel C Digital Bit i Input. MSB is bit 11
I	15, 19, 23, 30, 34, 38, 43, 47, 51, 56, 60, 66	12	DID<0:11>	DID<i> Is Channel D Digital Bit i Input. MSB is bit 11
O	70	1	OUTP	Differential Output
O	69	1	OUTN	

Pin Layout (TOP view)

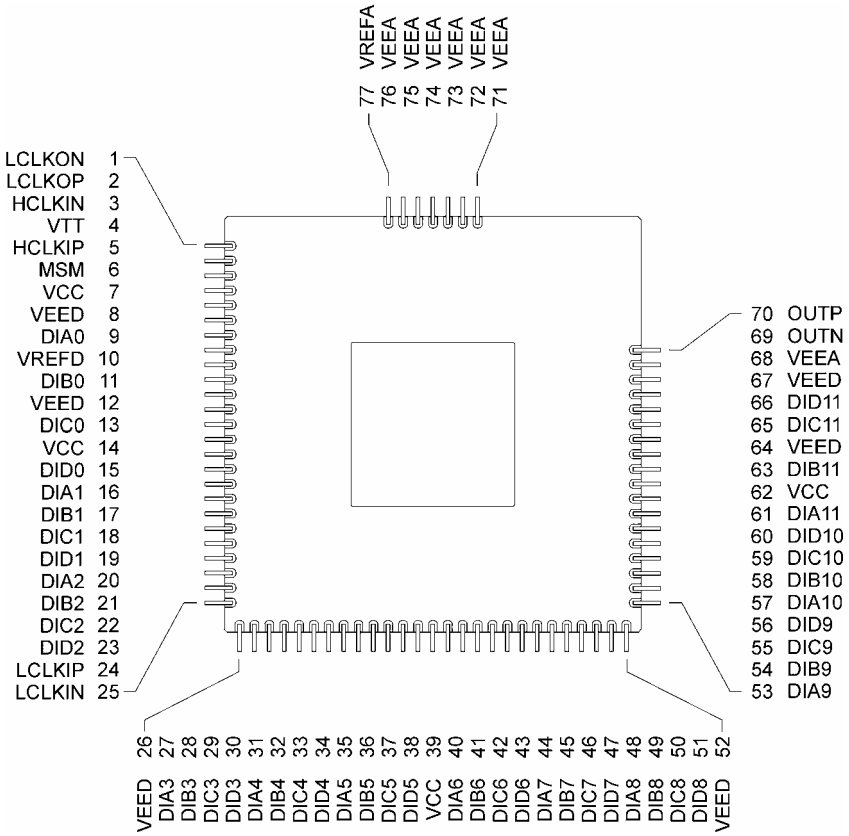

Figure 2 - RDA012M4MS-HD pinout (top view).

Pad Layout

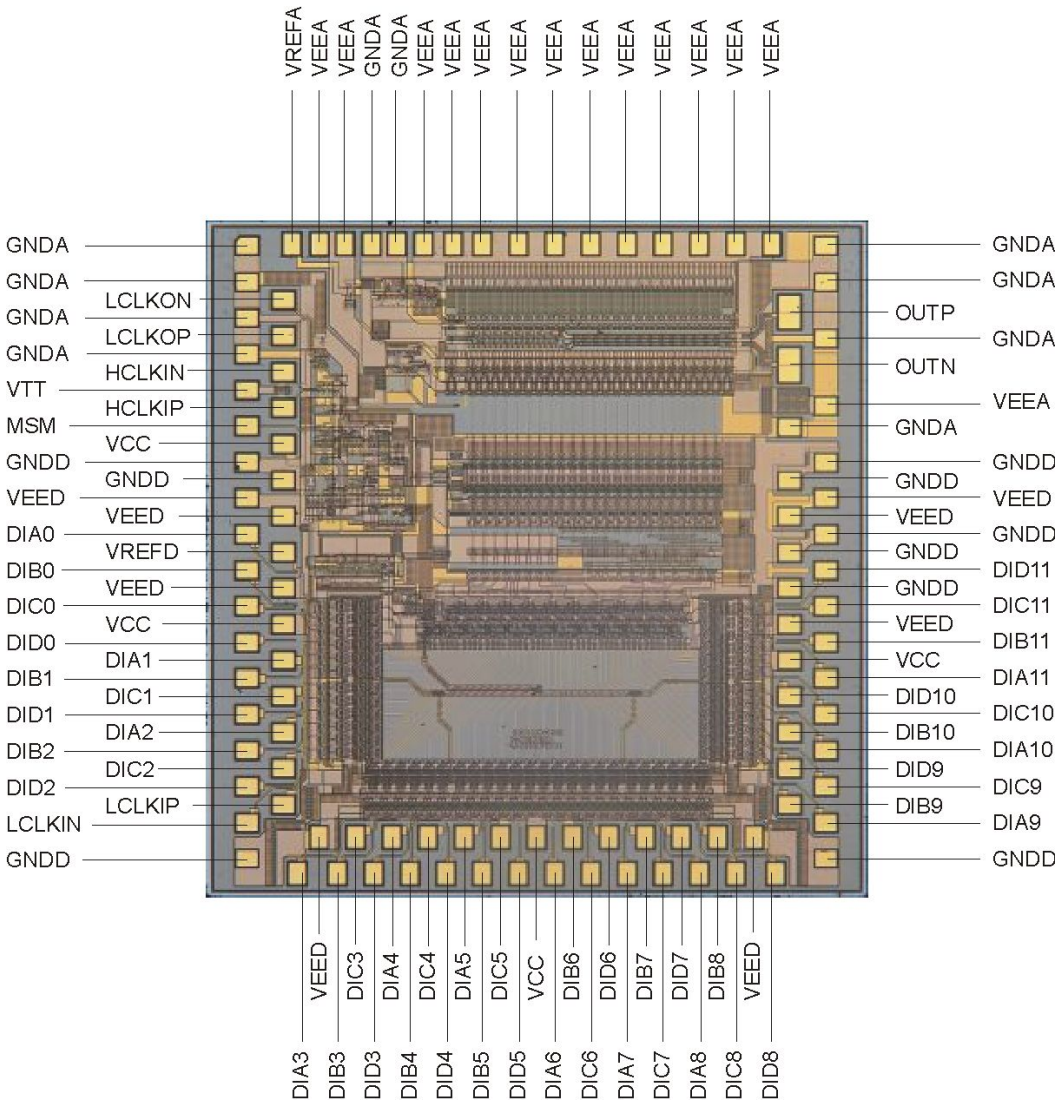

Figure 3 - RDA012M4MS pad layout.

Theory of Operation

For best dynamic and static performance, the DAC employs 6-bit segmentation. The 3.3V NMOS compatible 12-bit digital data inputs are latched by a master-slave flip-flop immediately after the input buffer to reduce the data skew. The four-channel data are combined together by the 48:12 MUX and latched again. The 6 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 6 LSB data bits are transported through the delay equalizer block. The digital data are synchronized again by a second master slave flip-flop to reduce the switching glitch. The decoded 6 MSB data drive 63 identical current switches, and the 6 LSB data drive 6 current switches. The output nodes from the LSB current switches are connected to the analog output through an R-2R ladder to generate the binary output.

The DAC output full-scale voltage follows the relationship $V_{FS} = 0.3xV_{REF.}$ An internal reference circuit with approximately -10dB supply rejection is integrated on chip for application convenience. The reference pin is provided for monitoring and for bypass purposes. To band-limit the noise on the reference voltage, the reference pin should be bypassed to the GNDA node with capacitance > 100pF. The VREF pin can also be used to override the internal reference with an accurate, temperature-compensated external voltage reference.

The timing diagram is shown in figure 3. The 1.3GHz external clock (HCLK) is divided by 2 and 4 resulting in the MUX internal selection signals S0 and S1. A low-speed clock (LCLK) is provided to drive the external digital. The four-channel data input are latched with an internal clock that is synchronized with the LCLK. Controlled by S0 and S1, input data are fed to the 1.3GS/s DAC in the order shown.

For applications requiring two MUXDACs, such as quadrature modulation, the RDA012M4MS offers master and slave mode operation. This provides synchronization between the two MUXDACs in a straightforward manner. Figure 4 illustrates two MUXDACs in an I-Q configuration and 1 GS/s conversion rate. The I-MUXDAC is in master mode and the Q-MUXDAC is in slave mode. The master MUXDAC generates an LVDS compatible 250MHz clock signal that is input to the slave MUXDAC were it is used to synchronize the generation of the select signal for the input muxes. The slave device then feeds this clock to the FPGA clock driver. For proper synchronization, the delay associated with the LVDS clock signal from master to slave MUXDAC must not exceed one clock period of the high-speed clock.

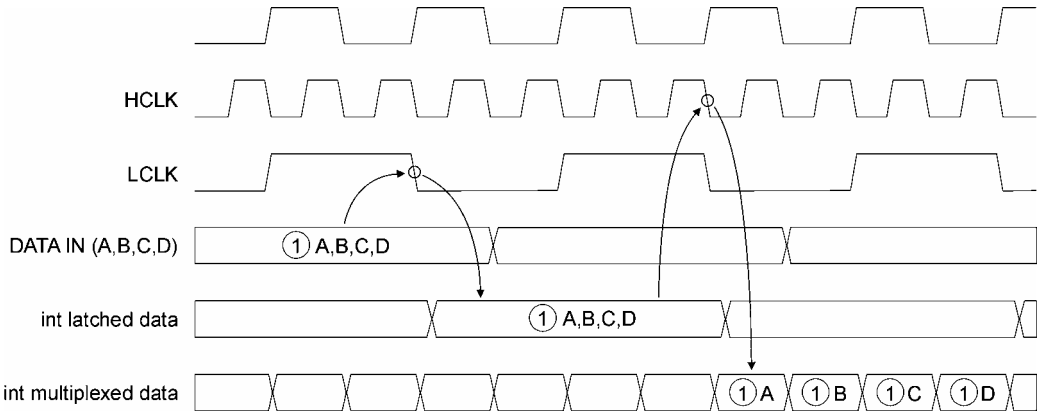

Figure 4 - Input Timing Diagram.

Signal Description

HIGH SPEED INPUT CLOCK.

The RDA012M4MS high-speed clock input is differential and can be driven from typical ECL circuits. Also a differential sinusoidal clock can be used. The HCLKIP and HCLKIN inputs, are internally terminated with 50 Ω to VTT which should be connected to a well decoupled –2.0 volt supply. Since the MUXDAC's output phase noise is directly related to the input clock noise and jitter, a low-jitter clock source is ideal. The internal clock driver generates very little added jitter (~100fs). A 500MHz MUXDAC output demands a white noise induced clock jitter of less than 250fs for a 10-bit equivalent, 62dB SNDR.

DATA INPUT.

The data inputs are 3.3V NMOS-compatible. The data is interleaved according to significant bit. For example, consecutive data pins will occur as A0, B0, C0, D0, A1, B1, etc.

OUTPUT CLOCK.

Output clock LCLKOP and LCLKON are supplied for the DSP/FPGA/ASIC in slave mode, or connected to another MUXDAC if in master mode. They are LVDS compliant and needs to be terminated with a100Ω resistor in front of the clock driver for the ASIC/DSP.

For application convenience, the data input's setup and hold time is specified with respect to the LCLKO. It should be noted that LCLKOP and LCLKON are driven by the MUXDAC and the waveforms of these signals are better defined at the receiver end; that is, near the ASIC/DSP chip that provides the input data for the MUXDAC. The system designer should consider the delay associated with the signal routing in the system's timing budget.

In figure 6, the setup and hold time of the LCLK to data transition are defined at the MUXDAC side. Data transitions of the data input have to occur during the "Valid Data Transition Window." The timing margin seen from the MUXDAC is T_P-T_S where T_P is the LCLKO period and T_S is the setup time, assuming that the ASIC chip takes LCLKO as the clock input and its outputs are latched at the falling edge of the clock. From the ASIC/DSP end, however, the timing margin is decreased by the amount equal to the sum of the data delay and clock delay between the two chips, as noted in the lower part of the diagram.

ANALOG OUTPUT.

The outputs DACOUTP and DACOUTN should both be connected though a 50 Ω resistor to ground. This will give a full-scale amplitude of 0.6 volt (both outputs must be terminated), 1.2 volt differentially. The output common mode can be changed by terminating the load resistors to a different voltage. The device is optimized to perform best when connected to a voltage between 0 and 1 volt, however. For reliable operation, the output termination voltage should not exceed 3 volts.

REFERENCE.

VREFA is provided for added control of the full-scale amplitude output. The internal reference circuit is designed to provide -2.0 volts, which can change up to ±5% as the supply voltage and/or operating temperature changes. If the user prefers accurate absolute full-scale, use an external voltage reference with low output impedance to override the internal reference. The output full-scale voltage follows the relationship V_{FS} = 0.3xV_{REF}. Note that the MUXDAC is optimized to have the best performance with a reference voltage of -2.0 volts. The output resistance of the reference node is 560 Ω ±10%. VREFD allows adjusting of the digital circuitry bias point for varying input voltage swings. In most cases, VREFD should be bypassed to GND.

Typical Operating Circuit

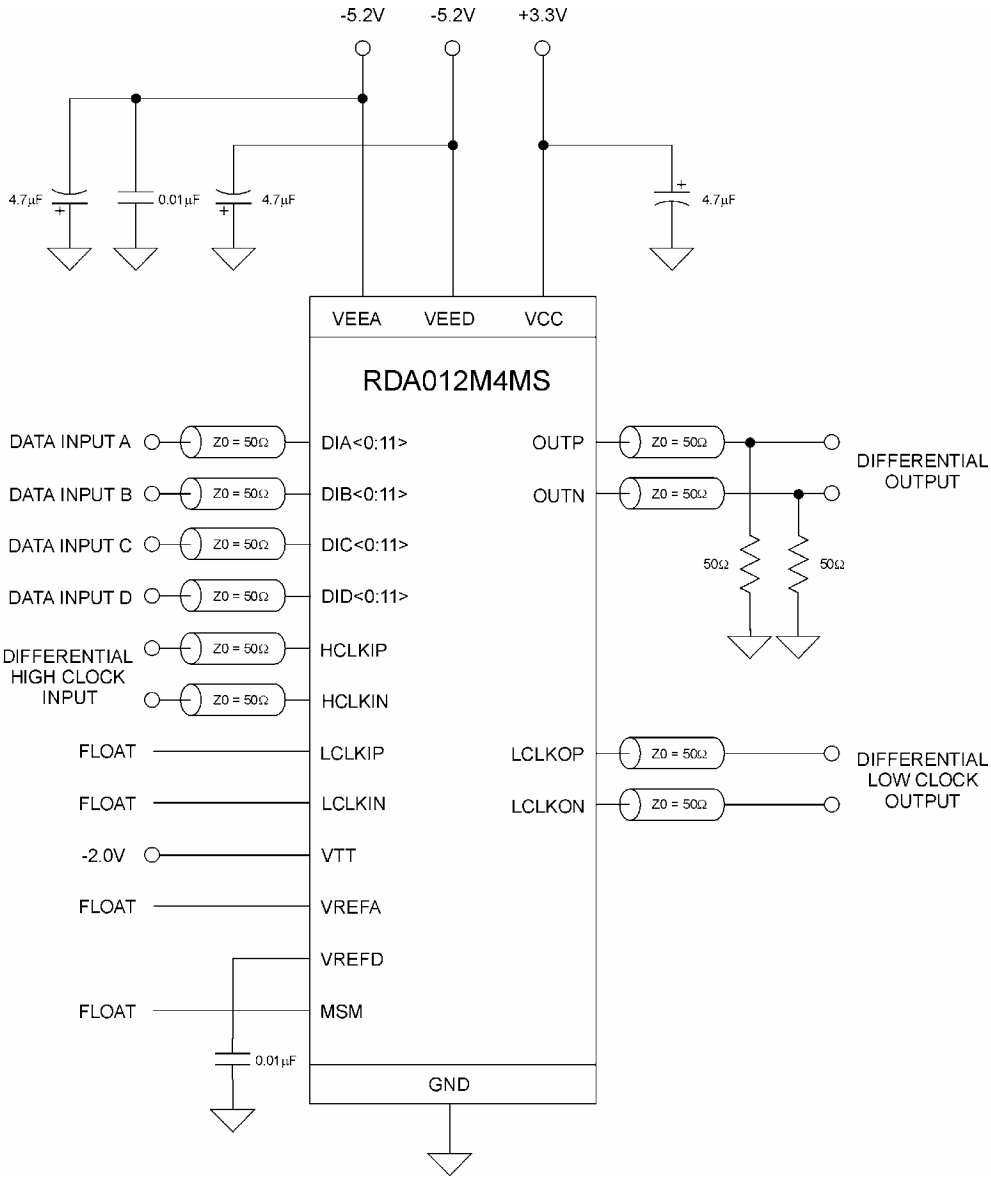

Figure 5 - RDA012M4MS typical operating circuit using the internal voltage reference.

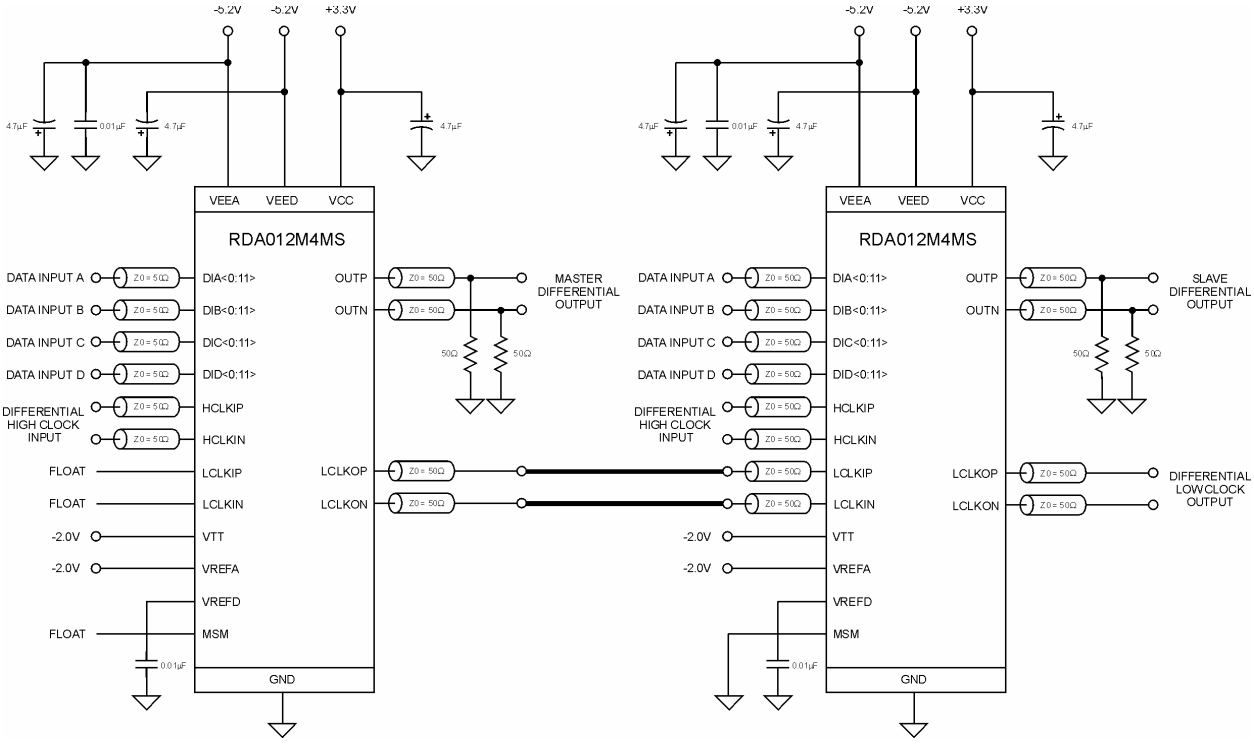

Figure 6 - RDA012M4MS typical operating circuit in master-slave mode using external voltage reference.

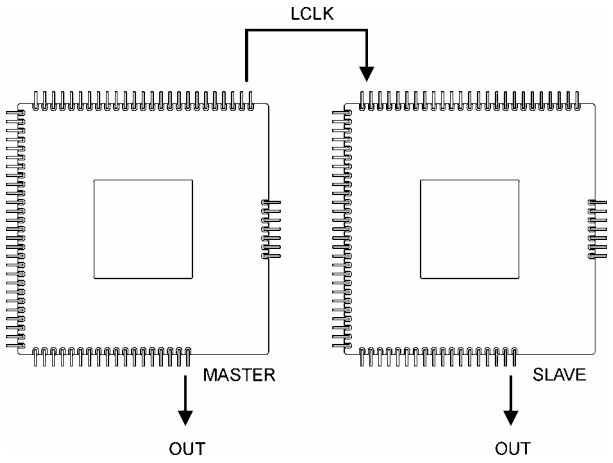

Figure 7 - RDA012M4MS recommended placement in master-slave mode to minimize LCLK routing.

Typical Performance

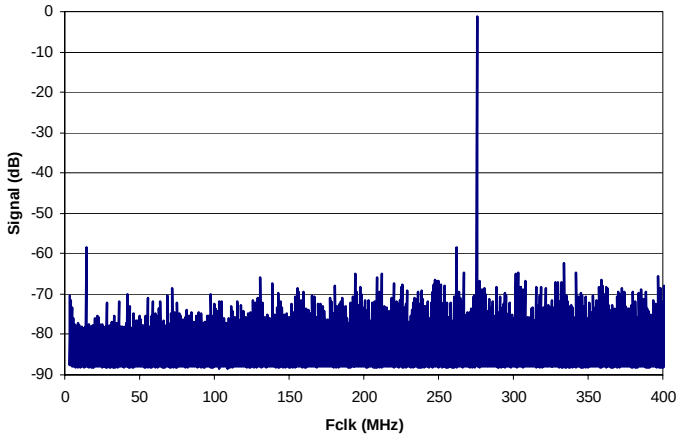

Figure 8 - Output spectrum at Fclk=800MHz, Fout=270MHz

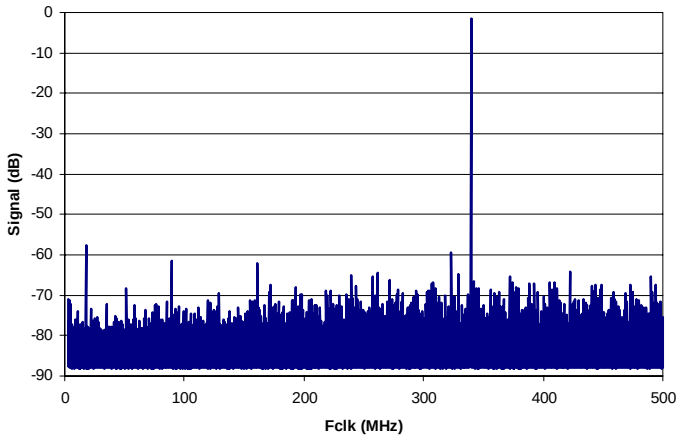

Figure 9 - Output spectrum at Fclk=1000MHz, Fout=340MHz

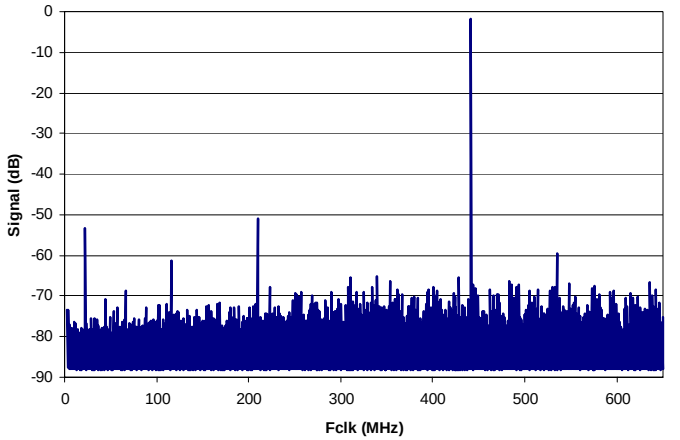

Figure 10 - Output spectrum at Fclk=1300MHz, Fout=340MHz

Package Information

The package is a 77 pin HSD with a heat sink slug on the package's bottom. The leads are gull-winged formed and trimmed to 0.053 inch (1.35 mm) in lenght.

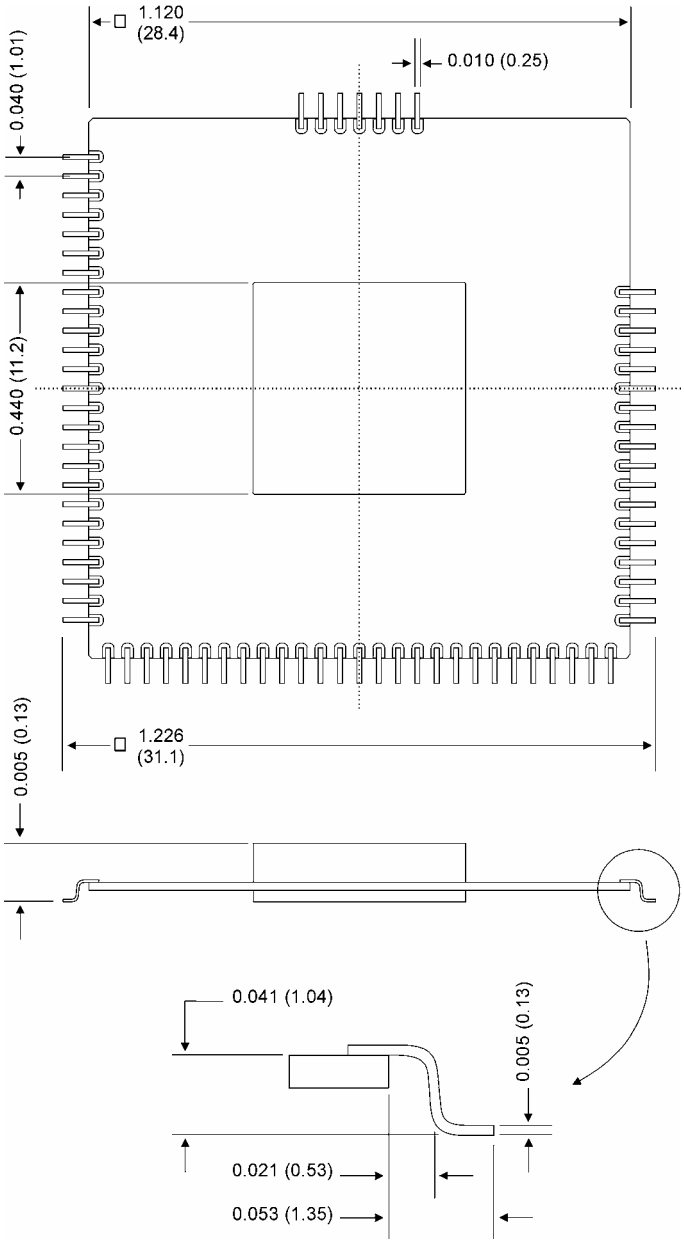

Figure 11 - RDA012M4MS-HD package, dimensions shown in inches (mm).

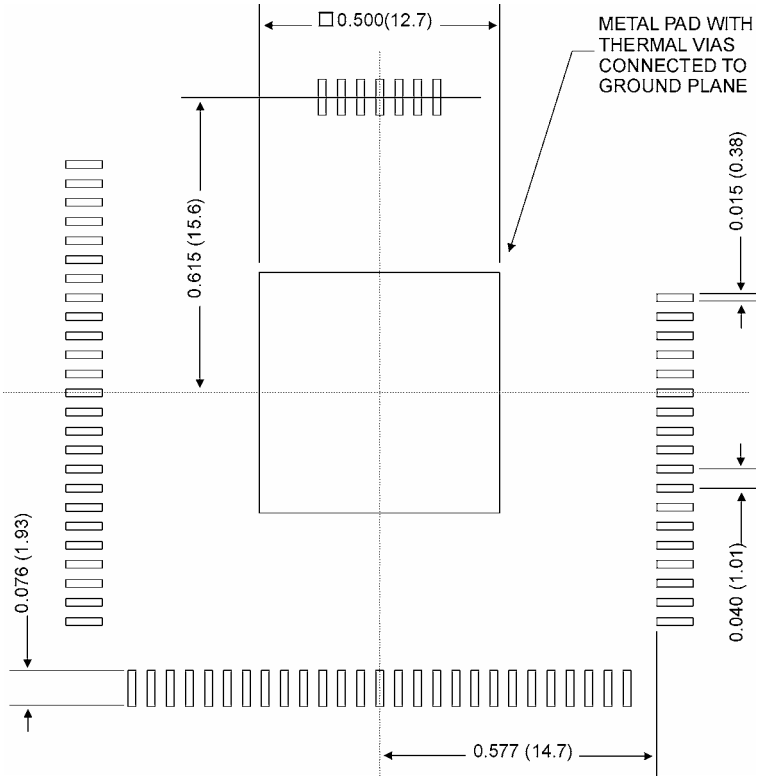

Figure 12 - RDA012M4MS-HD footprint, dimensions shown in inches (mm).