SYSTEM CAMERA DEVICE

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1. GENERAL DESCRIPTION

W99685FS is a high performance and highly-integrated system camera device that it can preview, capture, compress, store, and display the digital still images or playback a short period of live video.

This chip provide 8 or 16 Bits Host interface and easy for base band chip(Host) to develop Camera function through Command set protocol that allow the development of products without knowing any W99685FS chip programming.

W99685FS Built-in 8-bit 8032 compatible uC with internal 16KB program RAM and 4K data RAM.

Program can be down load from Host bus interface. This chip also Built-in 2M byte frame buffer for real-time video clip (MJPG) and burst snapshot. Support CCIR-656 8-bit YUV CMOS or CCD capture sensor interface.

W99685FS Support up to dual LCD Panels interface with MCU type interface. Support TFT-LCD, CSTN-LCD, STN-LCD Panel Types, If camera function is active, The host CPU can use W99685FS as the bridge (display controller) to LCM. And it can provide multiple display buffers.

If camera function is disabled, the host CPU can use bypass mode to control the LCM directly for maximum power saving.

W99685FS Support dual video pipes and double buffering for real-time motion JPEG, Support smooth digital zoom of video pipes, different kinds of raw data formats for display, some popular image color effects (Black & White, Sepia, Negative, Solarize or Oil Painting), Video Rotation / Mirror / Flip for capture and playback, Sticker maker, Comic Photo maker and smart frame rate control.

2. FEATURES

- **General**
  - 0.18um logic process
  - Core 1.8V
  - I/O 2.6V - 3.6V
  - Power consumption
    - < 23mA for 160x120 @ 15 fps, 2.8V preview mode
    - < 35mA for 160x120 @ 30fps, 2.8V preview mode
  - Support power-down mode
  - Support LCD bypass mode
  - Support GPIO pins for flash light control or else
  - Built-in smart processor to allow the development of products without knowing any W99685 chip programming. Minimum product design cycle time for fast time-to-market
  - Built-in 8-bit 8032 compatible uC with internal 16KB program RAM and 4K data RAM
  - Program can be down load from host interface.
  - Built-in 2M bytes frame buffer for real-time video clip (M-JPEG) and burst snapshot.
  - Support VGA/ Mega image resolution

- **Sensor Interface**
  - Support CCIR-656 8-bit YUV interface
  - Supports fast serial interface to program image sensor.
- **Host Interface**
  - 8/16 bits parallel Bus (Indirect access)
- **Easy for base band chip(Host) to develop Camera function through Command set protocol.**
- **LCD Display Interface**
  - Support up to dual LCD Panels interface
  - Supports **MCU type interface** LCD module
  - Supports 8/16/18-bit display data output to LCD Penal
  - Support 4 kinds of display data format out to LCD Penal
    - 256 colors (RGB-332)
    - 4096 colors (RGB-444)
    - 64k colors (RGB-565)
    - 256k colors (RGB-666)
  - Support LCD interface bypass mode
  - Support TFT-LCD, CSTN-LCD, STN-LCD Panel Types
  - If camera function is active, the host CPU can use W99685FS as the bridge (display controller) to LCM. And it can provide multiple display buffers.
  - If camera function is disabled, the host CPU can use bypass mode to control the LCM directly for maximum power saving.
- **JPEG CODEC for Image Compression and Decompression**
  - Fully compliant with ISO/IEC 10918-1 international JPEG standard
  - JPEG compression and decompression for still images
  - Real-time motion JPEG (M-JPEG) compression with advanced bit rate control for live video
  - JPEG baseline sequential mode in interleaved scan YcbCr(4:2:2) or YcbCr(4:2:0) format
  - Support adjustable quantization table for different compression ratio
  - Support smooth digital zoom
  - Support JPEG re-sizing and re-encoding
- **Operation Modes**
  - Preview ModeFrame rate up to 30 fps
  - Single Snapshot Mode
  - Burst Snapshot Mode
    - Support up to 10 frames burst snapshot at 1/30 sec interval
  - Movie Mode (Motion JPEG)
    - About 15 seconds recording time with 800K bytes vedio buffer at 160x120 size @ 15 fps

- Playback Mode
- Comic Photo Mode
- Transfer Mode
- Still Image Size
  - 1280 x 960
  - 640 x 480 (VGA)
  - 320 x 240 (QVGA)
  - 160 x 120 (QQVGA)
  - Subject to change by request
- Video Clip Size
  - 160 x 120 (QQVGA)
  - Subject to change by request

❑ **Video Display Function**

- Support high-color / OSD Video overlay function
- Support graphics/video blending
- Support image Rotation / Flip / Mirror
  - Left 90 degree rotation
  - Right 90 degree rotation
  - 180 degree rotation
  - Horizontal mirror
  - Vertical flip
- Support image color effects
  - Normal
  - Black & white
  - Sepia
  - Negative
  - Solarize / oil painting
- Support image sticker maker
- Support imprint of message photo
- Support comic photo maker
- Support OSD Video overlay function
- Support dual video pipes and double buffering for real-time Motion JPEG
- Support arbitrary N/M (=[0..255]) scaling-down of video pipes
- Support different kinds of raw data formats for display
- Support some popular image color effects
- Support smart frame rate control

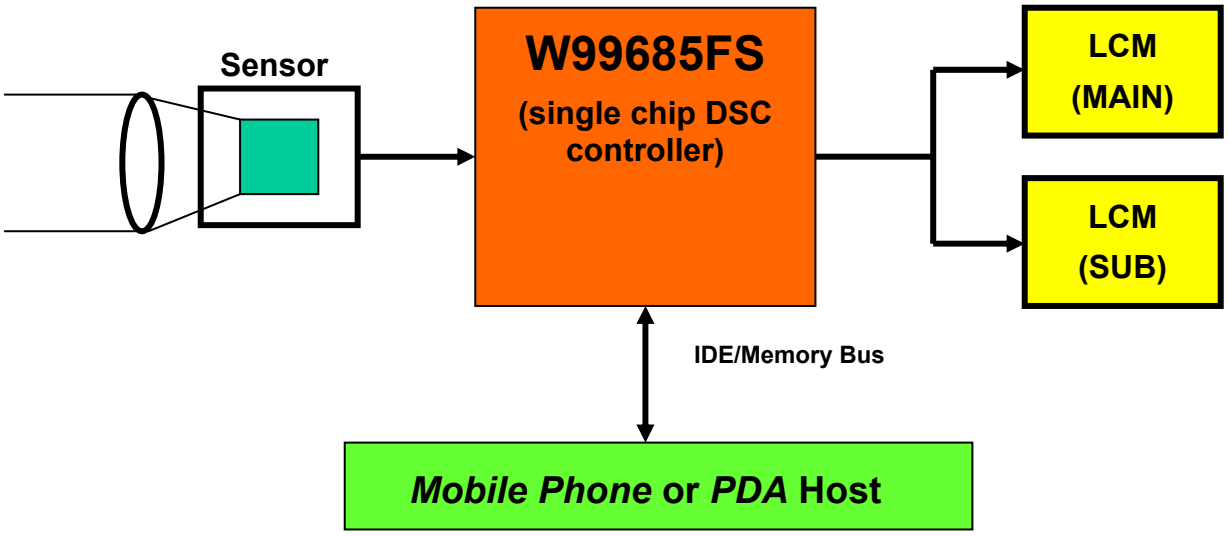
- **USB Interface**Compliant with USB Spec. Rev. 1.1 specification
  - Supports three USB pipes including:
    - Control pipe
    - Bulk-in pipe
    - Bulk-out pipe

- **Power Management**
  - Advanced power management including:
    - Power-down mode
    - Stand-by mode
    - Operating mode

- **Package:**
  - **W99685FS**/ BGA 108-Balls package (8mm x 8mm)

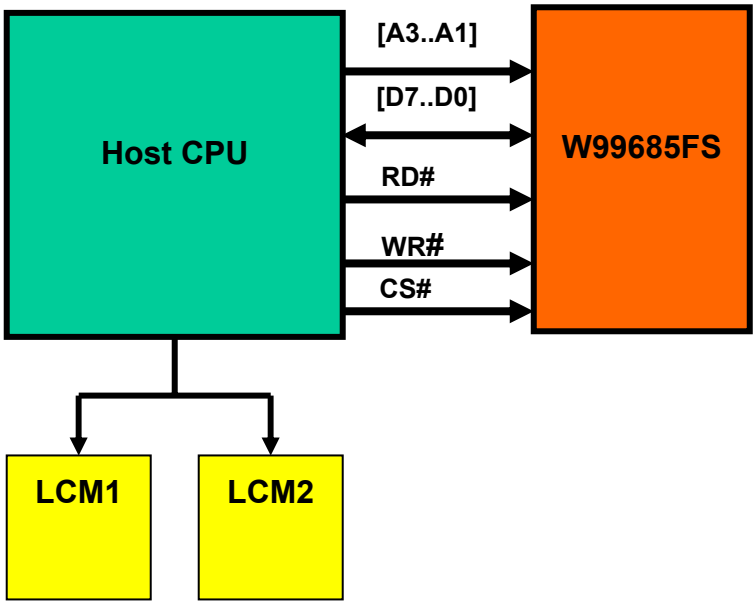
3. APPLICATION

3.1 System Overview

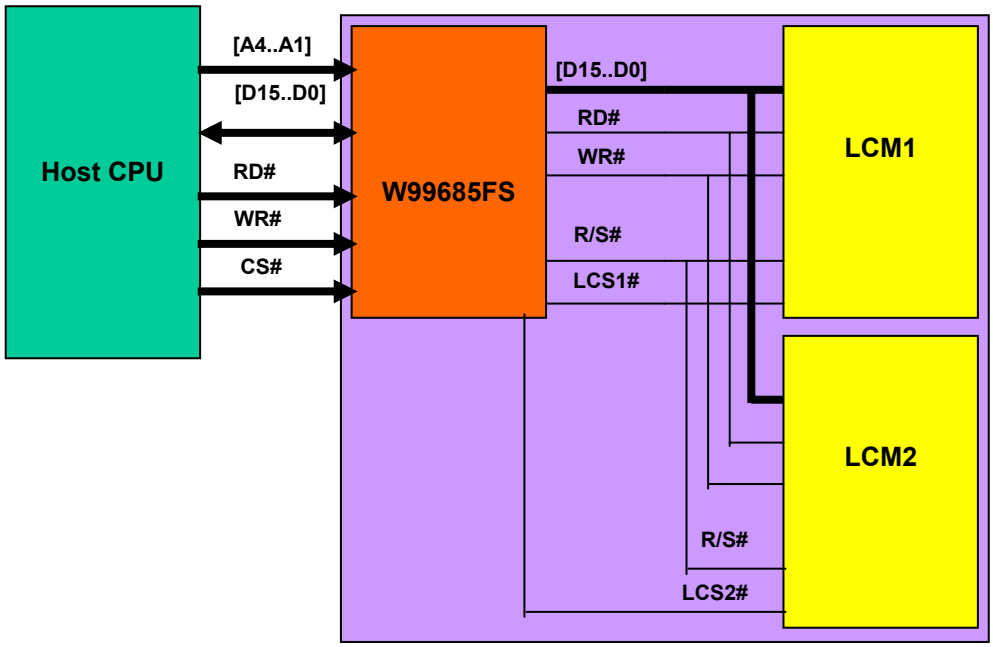


3.2 Host Interface

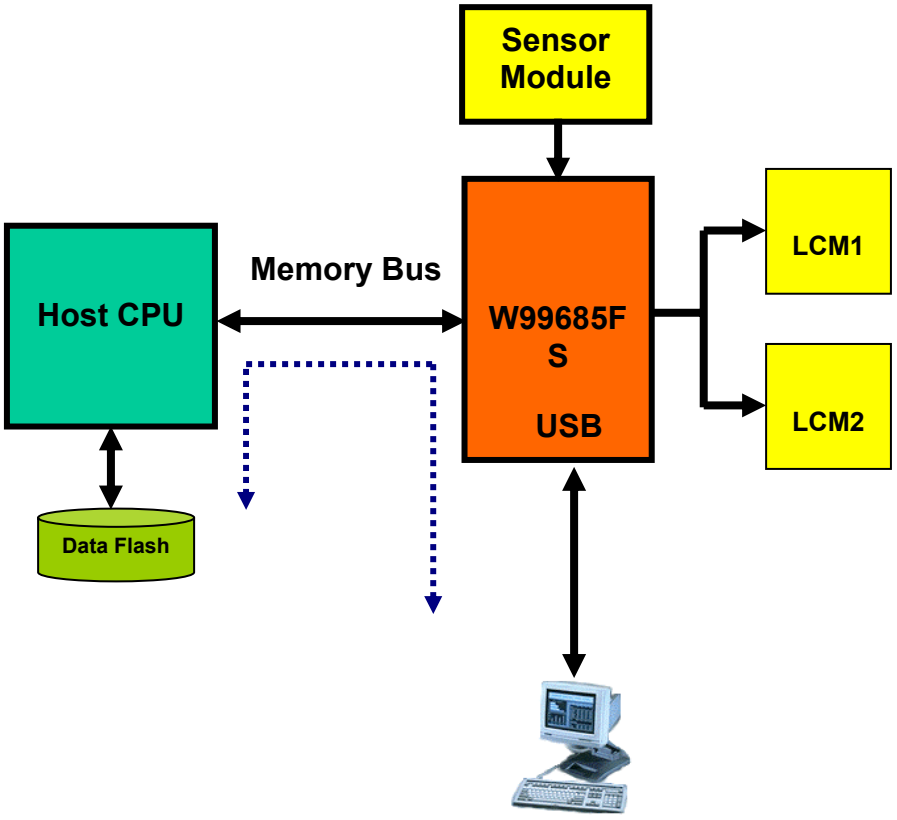
- **Host Interface IDE**
  - High speed parallel bus (8-bit or 16-bit)
  - Ideal attachable CF camera solution especially for PDA with CF slot
  - Ideal built-in camera solution
- **Host Interface IDE-1**



- **Host Interface IDE-2**



3.3 USB Interface with PC



3.4 Camera Implementation

- **Preview Mode Features**
  - Support raw data preview or JPEG preview
  - Support video preview directly to LCM
  - Support video rotation/flip/mirror
  - Support live color effect and sticker display
  - Support up to 30 fps preview depending on the sensor frame rate
  - Support digital zoom
- **Snapshot Mode Features**
  - Support encoding of different size of images
  - Support image rotation/flip/mirror
  - Support color effect and sticker functions
- **Burst Snapshot Mode Features**
  - Extension to snapshot (single capture) mode
  - Support up to 10 frames burst snapshot at 1/30 sec interval
  - The encoded pictures are stored in W99685 frame buffer, the host can select the favorite ones for storage.
- **Movie Mode Features**
  - Support real-time video clip encoding
  - The video clip (dumb video) is stored in W99685 frame buffer, the duration depends on the frame rate and resolution
  - Support up to 800KB video clip in frame buffer
  - Dumb Video Implementation
  - Motion JPEG Movie Implementation
- **Playback Mode Features**
  - Support still JPEG playback directly to LCD or raw data
  - Support motion JPEG video playback direct to LCD or raw data
  - Support image rotation/flip/mirror
  - Support playback mode digital zoom in for 1.0x~2.0x to raw data or 1.0x~7.999x to LCD at small steps
  - Support playback mode digital zoom out to LCD or raw data at N/M (=[0..255])
  - Support pan/tilt control for LCD output at zoom in
  - Support JPEG re-sizing and re-encoding
- **Comic Photo Mode Features**Support MxN grids of comic photo
  - Each grid of comic photo can come either from a stored JPEG file or a captured video frame.

4. PIN DESCRIPTION

4.1 W99685FS Pin Definition (108 balls, LFBGA Package)

The following signal types are used in these descriptions.

I Input pin
IS Input pin with Schmitt trigger
B Bi-directional input/output pin
BR Bi-directional input/output pin with repeater
BU Bi-directional input/output pin with internal pull-up
O Output pin
A Analog input/output pin
P Power supply pin
G Ground pin
Active low

USB Interface (2 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DP	P6	A	Data Plus line of differential USB upstream port. Note: provide an external 1.5 KΩ pull-up resistor at DP so the device indicates to the host that it is a full-speed device.
DM	P7	A	Data Minus line of differential USB upstream port.

UART Interface (2 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
TXD / P3[1]	P10	B	Serial Transmit Data Port-3 Bit-1
RXD / P3[0]	P9	B	Serial Receive Data Port-3 Bit-0

Sensor or Video Input Interface (14 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SVID[9:0]	A7, B8, M14, A8, B9, A9, A10, B10, A11, B11	I	Sensor or Video Data Input SVID[9:0].
SPCLK	B7	I	Clock for Sensor or Video Data Input
SVS	F13	B	Vertical Sync Input. Programmable polarity.
SHS	A6	B	Horizontal Sync Input. Programmable polarity.
SCLK	E7	O	Clock Output to Sensor

LCD Digital Display Interface (22 pins) & POWER ON SETTING (8 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
LA0	P13	O	M-LCD: Address-0, for LCD Controller RS signal (CMD/DAT#)
LCD_CS0#	P12	O	M-LCD: LCD Chip Select 0 enable
LCD_WR#/	E10	O	M-LCD: Write Enable/ M-68 mode data RW# control
LCD_RD#	H13	O	M-LCD: Read Enable/ M-68 mode data enable
LDAT [7:0]/ Setting [7:0]	K14, E13, L14, F14, J14, G13, K13, H14	BU	Digital Display Output Data 8 bits Power On Setting [7:0]
LDAT [17:8]	P14, J13, A13, N14, A14, B14, D14, C14, H10, E14	BU	Digital Display Output Data [17:8]bits

SD Interface (6 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SD_CLK	P2	O	HCLK for SD Card CLK
SD_CMD	P1	O	Host SD_CMD for SD Card CMD signal
SD[3:0]	P5, P4, N2, P3	BU	Host Data for SD Card signal

Host Interface (24 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
FA0	C1	BR	Address-0
FA1	D1	BR	Address-1
FA2	D2	BR	Address-2
NC	G5	-	No define
FIORD#	E5	BU	I/O Read Strobe
FIOWR#	D13	BU	I/O Write Strobe
FCE2# / LCD_CS#	E2	BR	Chip Select Signal – 2 LCD Function Selected
FCE1#	F2	BR	Chip Select Signal – 1
FD [15:0]	A2, A1, N10, B1, B2, N9, B5, A3, H1, K5, H2, G1, G2, N8, N6, H5	BR	Data Bus FD[15:0]

GPIO (14 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
GPIO0/ SD_WP#	N5	BU	General Purpose I/O [0] Write protect for SD Card
GPIO1/ LCD_CS1#	L2	BU	General Purpose I/O [1] M-LCD: LCD Chip Select 1 enable
GPIO2/ VBUS	B6	BU	General Purpose I/O [2] 20mA power supply output
GPIO3/ SCK	K10	BU	General Purpose I/O [3] Serial Interface Clock
GPIO4/ SDI/SDA	A5	BU	General Purpose I/O [4] Serial Interface Data Input/ Serial Data Acknowledge
GPIO5/ SDO/SDE	N11	BU	General Purpose I/O [5] Serial Interface Data Output / Serial Data Enable
GPIO7	A4	BU	General Purpose I/O [7]
NC	P11	-	No define
NC	B4	-	No define
GPIO10 SD_CD#	A12	BU	General Purpose I/O [10] SD Card Inserted Detect
GPIO12	F1	BU	General Purpose I/O [12]
GPIO13	N4	BU	General Purpose I/O [13]
GPIO14	L13	BU	General Purpose I/O [14]
GPIO15	G14	BU	General Purpose I/O [15]

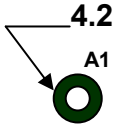
Miscellaneous (4 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
XIN	J2	I	Reference frequency input from ext. crystal or a clock source.
XOUT	J1	O	Oscillator output to a crystal. This pin is left unconnected if an external clock source is employed.
RESET	M1	IS	Reset In. This pin is active high to reset W99685FS chip.
TME	N1	I	Test Mode Enable. Only for test, this pin must be connected to GND for normal operation.

Power and Ground (20 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VDDB	B13, E1, K2, N13	P	I/O Pad Buffer Power Supply. Provide isolated power to the I/O buffers for improved noise immunity. 2.6V ~ 3.6V
GND	E6, E9, F10, F5, K9, J10, J5, K6	G	Ground.
VDDI	E8, G10, K8	P	Internal Core Logic Power Supply. 1.8V
AVDDP	L1	P	PLL Power Supply. 1.8 V
AVSSP	K1	G	PLL Ground.
USBVDD	N7	P	USB Power Supply. 3.0V ~ 3.6V
USBVSS	P8	G	USB Ground.
VDDFB	K7	P	Embedded FRAME BUFFER Power Supply. 2.6V ~ 3.6V

4.2 W99685FS-108b Pin Assignment – (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	FD14	FD15	FD8	GPIO7	GPIO 4/SDA	SHS	SVID9	SVID6	SVID4	SVID3	SVID1	GPIO 10/SD _CD#	LDAT15	LDAT13
B	FD12	FD11		NC	FD9	GPIO2/ VBUS	SPCLK	SVID8	SVID5	SVID2	SVID0		VDDB	LDAT12
C	FA0													LDAT10
D	FA1	FA2											FIOW R#	LDAT11
E	VDDB	FCE2 #/ LCD_ CS#			FIORD#	GND	SCLK	VDDI (1.8V)	GND	LCD_ WR#			LDAT6	LDAT8
F	GPIO 12	FCE1#			GND					GND			SVS	LDAT4
G	FD4	FD3			NC					VDDI (1.8V)			LDAT2	GPIO15
H	FD7	FD5			FD0					LDAT9			LCD_ RD#	LDAT 0
J	XOUT	XIN			GND					GND			LDAT16	LDAT3
K	AVSSP (GND)	VDDB			FD6	GND	VDDFB	VDDI (1.8V)	GND	GPIO 3/SCK			LDAT1	LDAT7
L	AVDDP (1.8V)	GPIO1/ LCD_C S1#											GPIO14	LDAT5
M	RESET													SVID7
N	TME	SD1		GPIO13	GPIO0/ SD_WP #	FD1	USBVDD	FD2	FD10	FD13	GPIO5/ SDO		VDDB	LDAT14
P	SD_ CMD	SD_ CLK	SD0	SD2	SD3	DP	DM	USBVSS	P30 / RXD	P31 / TXD	NC	LCD_ CS0#	LA0	LDAT17

W99685FS 108 Ball Location List

LOCATION/ NUMBER	PIN NAME	LOCATION/ NUMBER	PIN NAME
B13/ (1)	VDDB(2.6V~3.6V)	F14/ (55)	LDAT4 / SET4
B6/ (2)	GPIO2 / VBUS	L14/ (56)	LDAT5 / SET5
E5/ (3)	FIORD#	E13/ (57)	LDAT6 / SET6
D13/ (4)	FIOWR#	K14/ (58)	LDAT7 / SET7
E2/ (5)	FCE2# / LCD_CS#	E14/ (59)	LDAT8
F2/ (6)	FCE1#	H10/ (60)	LDAT9
F1/ (7)	GPIO12	C14/ (61)	LDAT10
E6/ (8)	GND	D14/ (62)	LDAT11
H5/ (9)	FD0	B14/ (63)	LDAT12
N6/ (10)	FD1	A14/ (64)	LDAT13
N8/ (11)	FD2	N14/ (65)	LDAT14
G2/ (12)	FD3	A13/ (66)	LDAT15
G1/ (13)	FD4	J13/ (67)	LDAT16
H2/ (14)	FD5	P14/ (68)	LDAT17
K5/ (15)	FD6	P13/ (69)	LA0
H1/ (16)	FD7	A12/ (70)	GPIO10 / SD_CD#
N5/ (17)	GPIO0 / SD_WP#	P12/ (71)	LCD_CS0#
E1/ (18)	VDDB(2.6V~3.6V)	E10/ (72)	LCD_WR#
J2/ (19)	XIN	H13/ (73)	LCD_RD#
J1/ (20)	XOUT	B11/ (74)	SVID0
E9/ (21)	GND	A11/ (75)	SVID1
L2/ (22)	GPIO1 / LCD_CS1#	B10/ (76)	SVID2
K1/ (23)	AVSSP(GND)	A10/ (77)	SVID3
L1/ (24)	AVDDP(1.8V)	K6/ (78)	GND
N4/ (25)	GPIO13	A9/ (79)	SVID4
N1/ (26)	TME	B9/ (80)	SVID5
M1/ (27)	RESET	K8/ (81)	VDDI(1.8V)
P2/ (28)	SD_CLK	A8/ (82)	SVID6
P1/ (29)	SD_CMD	M14/ (83)	SVID7
P3/ (30)	SD0	B8/ (84)	SVID8
N2/ (31)	SD1	A7/ (85)	SVID9

W99685FS 108 Ball Location List, continued

LOCATION/ NUMBER	PIN NAME	LOCATION/ NUMBER	PIN NAME
P4/ (32)	SD2	B7/ (86)	SPCLK
P5/ (33)	SD3	F13/ (87)	SVS
K2/ (34)	VDDB(2.6V~3.6V)	A6/ (88)	SHS
F10/ (35)	GND	E7/ (89)	SCLK
P8/ (36)	USBVSS	K10/ (90)	SCK / GPIO3
P6/ (37)	DP	A5/ (91)	SDA / GPIO4
P7/ (38)	DM	N11/ (92)	SDO / GPIO5
N7/ (39)	USBVDD	A4/ (93)	GPIO7
P9/ (40)	P30 / RXD	P11/ (94)	NC
P10/ (41)	P31 / TXD	B4/ (95)	NC
N13/ (42)	VDDB(2.6V~3.6V)	A3/ (96)	FD8
J10/ (43)	GND	B5/ (97)	FD9
E8/ (44)	VDDI(1.8V)	N9/ (98)	FD10
F5/ (45)	GND	B2/ (99)	FD11
G5/ (46)	NC	B1/ (100)	FD12
J5/ (47)	GND	N10/ (101)	FD13
H14/ (48)	LDAT0 / SET0	A1/ (102)	FD14
G10/ (49)	VDDI(1.8V)	A2/ (103)	FD15
L13/ (50)	GPIO14	C1/ (104)	FA0
G14/ (51)	GPIO15	D1/ (105)	FA1
K13/ (52)	LDAT1 / SET1	D2/ (106)	FA2
G13/ (53)	LDAT2 / SET2	K9/ (107)	GND
J14/ (54)	LDAT3 / SET3	K7/ (108)	VDDFB(2.6V ~ 3.6V)

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNIT
Ambient temperature	-20	70	°C
Storage temperature	-40	125	°C
DC supply voltage for core (1.8V) V_{DDI}	0	2.0	V
DC supply voltage for I/O (2.8V) V_{DDB}	0	3.6	V
I/O pin voltage with respect to V_{SS}	– 0.3	V_{DDB} +0.4	V

Table 5-1

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 D.C. Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDB}	Power Supply for I/O Pads		2.6	2.8	3.6	V
A_{VDDP}	Power Supply for PLL Analog		1.70	1.8	1.90	V
V_{DDI}	Power Supply for Core		1.70	1.8	1.90	V
V_{IL}	Input Low Voltage		0		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DDB}	V
V_{OL}	Output Low Voltage	I_{OUT} = 2mA			V_{SS} +0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -2mA	V_{DDB}* 0.8			V
V_{OH} (P30/P31)	Output High Voltage **(Open Drain with Internal Pull-Up)**	I_{OUT} = -2mA			2.0	V
I_{IL}	Input Low Leakage Current	V_{IN} = 0.4V			10	μA
I_{IH}	Input High Leakage Current	V_{IN} = 2.4V			-10	μA
I_{UP}	Pull-up Current	V_{IN} = 0V			-500	μA
I_{PD}	Power Down Current (XIN=0, No Load)	Core V_{DDI}= 1.8V		20		μA
		I/O V_{DDB}= 2.8V		120		
I_{DD}	Active Current	160x120 preview at 15 fps CPU clock at 12 MHz Engine clock at 24 MHz		20	30	mA

Table 5-2

5.3 A.C. Characteristics

5.3.1 RESET A.C. Characteristics

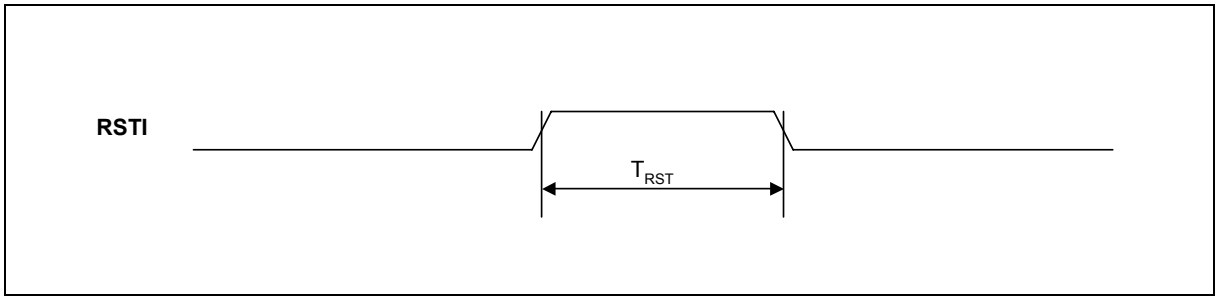


Figure 5.1 RESET Timing Diagram

RESET Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{RST}	Reset Pulse Width		1.0		mS

Table 5-3

5.3.2 Video Input A.C. Characteristics

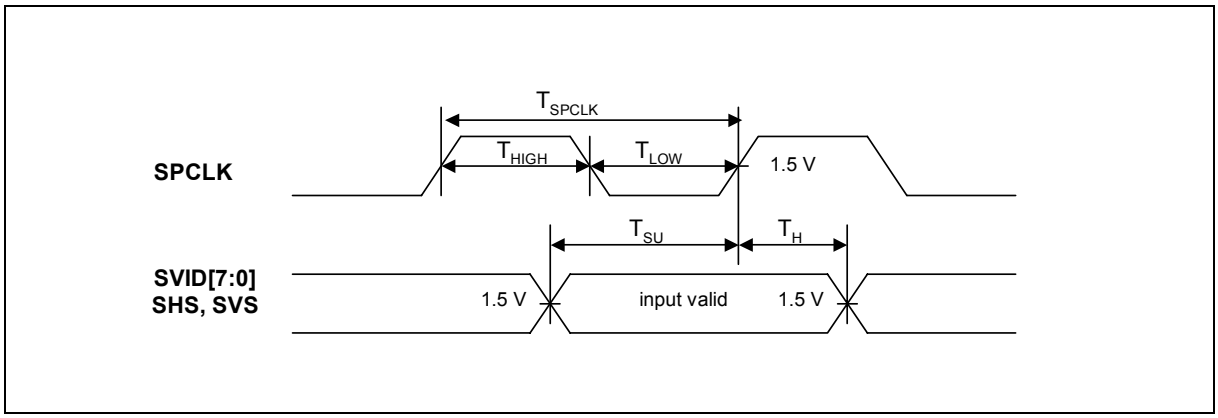


Figure 5.2 Input Video Timing Diagram

Input Video Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
F_{SPCLK}	SPCLK Frequency = 1 / T_{SPCLK}		5	48	MHz
T_{HIGH}	SPCLK Clock High Time		5		nS
T_{LOW}	SPCLK Clock Low Time		5		nS
T_{SU}	SVID[9:0], SHS, SVS Setup Time		6		nS
T_H	SVID[9:0], SHS, SVS Hold Time		4		nS

Table 5-4

5.3.3 Host Interface: CF-IDE Slave (Memory Bus) A.C. Characteristics

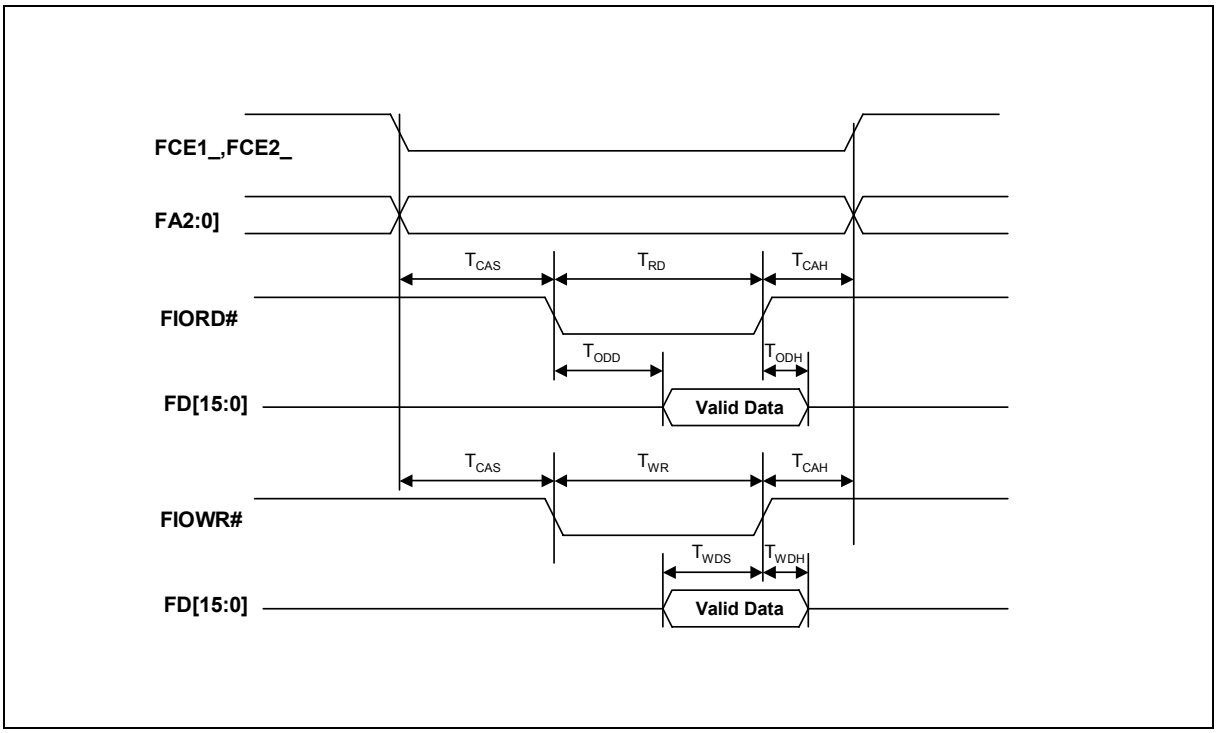


Figure 5.3 Host Interface: CF-IDE Slave (Memory Bus) Timing Diagram

Host Interface : CF_IDE Slave (Memory Bus) Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{CAS}	Chip Select & Address Set-up Time		65	---	nS
T_{CAH}	Chip Select & Address Hold Time		5	---	nS
T_{ODD}	FIORD# Low to Data Valid Delay		---	$2T_{MCLK}$	nS
T_{ODH}	Read Data Output Hold Time		0	---	nS
T_{RD}	FIORD# Pulse Width		$*165/4T_{MCLK}$	---	nS
T_{WDS}	Write Data Input Setup Time		60	---	nS
T_{WDH}	Write Data Input Hold Time		2	---	nS
T_{WR}	WR# Pulse Width		$*165/4T_{MCLK}$	---	nS

Table 5-5

$165/4T_{MCLK}$: 165ns or 4 internal engine clock cycles

5.3.4 LCD Interface A.C. Characteristics

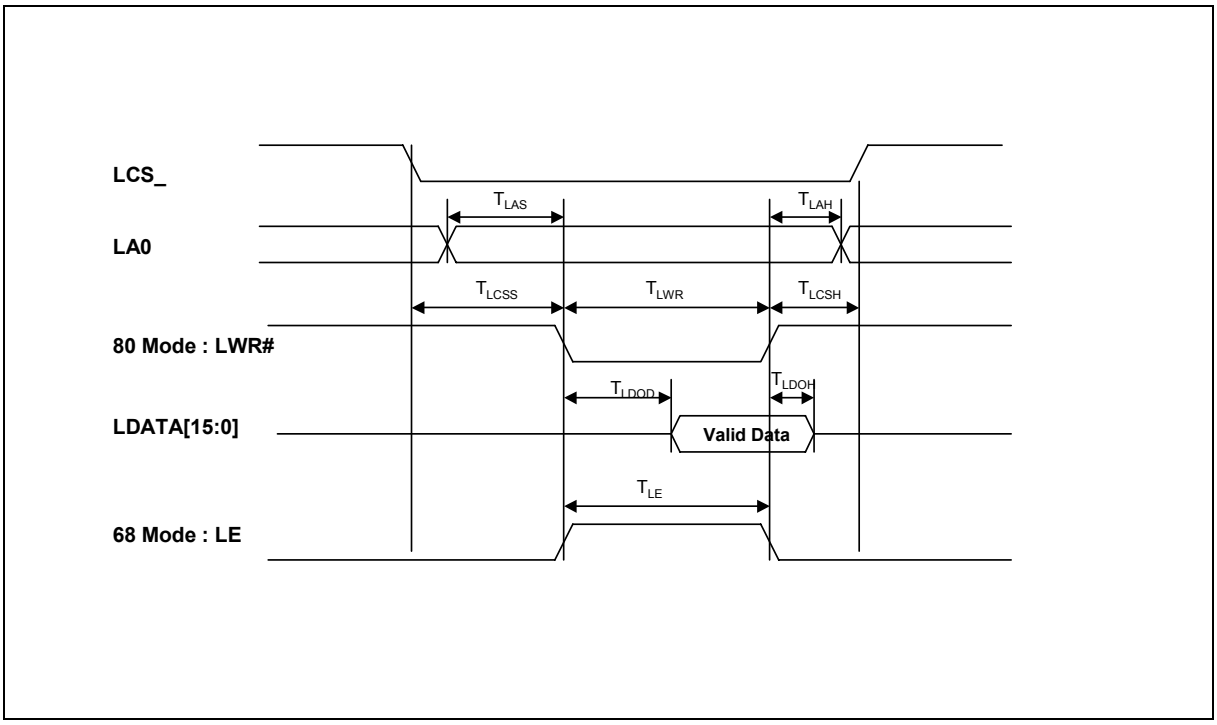


Figure 5.4 LCD Interface Timing Diagram

LCD Interface Timing

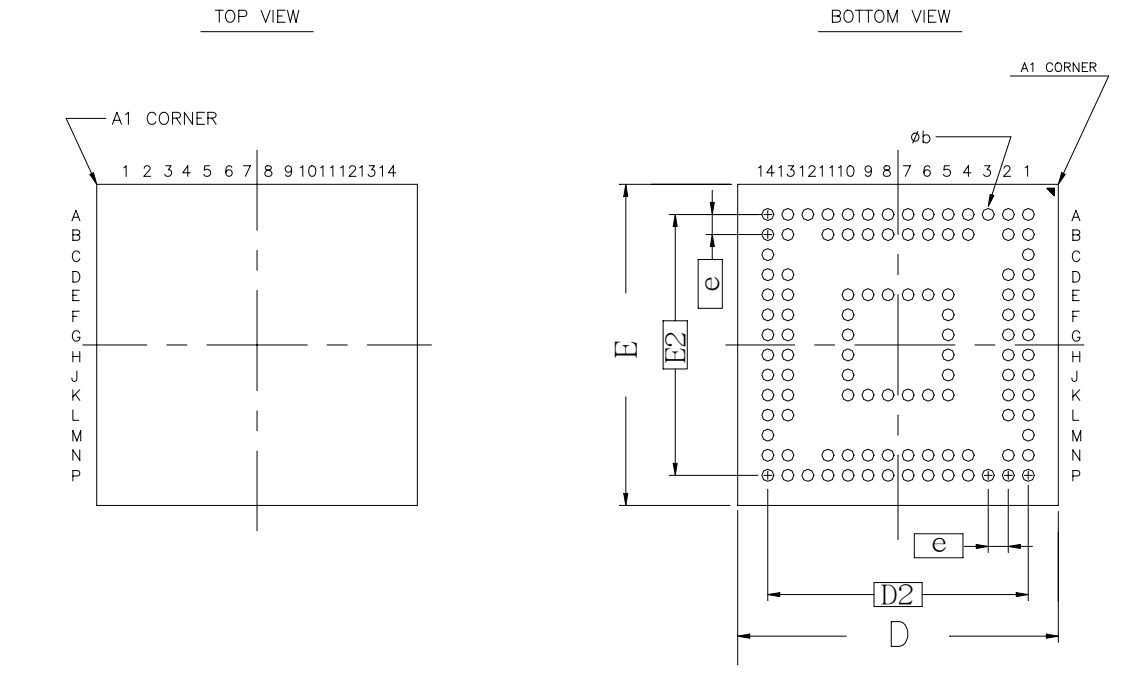
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{LCSS}	Chip Select Set-up Time		0.5	---	PCLK
T_{LCSH}	Chip Select Hold Time		0.5	---	PCLK
T_{LAS}	Address Set-up Time		1	---	PCLK
T_{LAH}	Address Hold Time		1	---	PCLK
T_{LDOD}	Write Data Active Delay		5	---	nS
T_{LDOH}	Write Data Hold Time		0.5	---	PCLK
T_{LWR}	LWR# Pulse Width	80 Mode	0.5		PCLK
T_{LE}	LE Pulse Width	68 Mode	0.5		PCLK

Table 5-6

Note: PCLK => Engine Clock / 32

6. PACKAGE DIMENSION

6.1 108L LFBGA (8 x 8 mm, Ball pitch: 0.5 mm, Ø = 0.3 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.50	–	–	0.059
A1	0.17	–	0.27	0.007	–	0.011
D	7.95	8.00	8.05	0.313	0.315	0.317
D2	6.50 BASIC			0.256 BASIC		
E	7.95	8.00	8.05	0.313	0.315	0.317
E2	6.50 BASIC			0.256 BASIC		
y	0.08 BASIC			0.003 BASIC		
øb	0.27	–	0.37	0.011	–	0.015
e	0.50 BASIC			0.020 BASIC		

7. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 28, 2004		Initial Issue
A2	Dec. 15, 2004	18	Revise Fspclk to 48 Mhz
A3	Feb. 24, 2005	2, 3, 9, 13	Revised USBVDD 3.0V ~ 3.6V, LCD I/F.
A4	April 13, 2005	17	Update I_{PD}

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