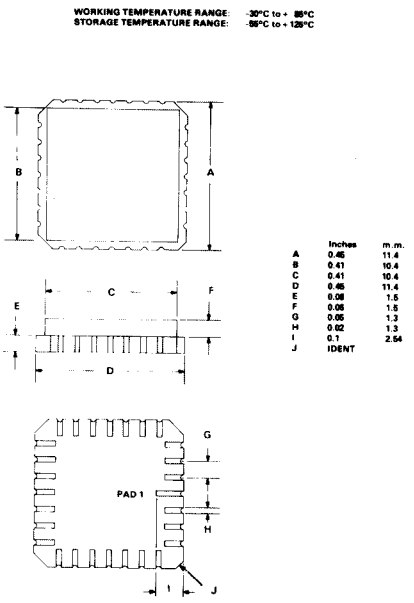
CONSUMER MICROCIRCUITS LTD

FX202 is an Obsolete Product
- For Information Only -

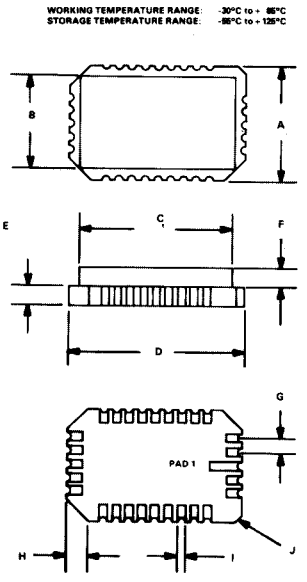
PRODUCT INFORMATION

PUBLICATION - D/FX '03-K/1 JANUARY 1982

FX102·K
FX202C·K
FX202Z·K
FX103·K
FX313·K
FX403·K
FX503C·K
FX503Z·K



	Inches	m.m.
A	0.45	11.4
B	0.41	10.4
C	0.41	10.4
D	0.45	11.4
E	0.06	1.5
F	0.06	1.5
G	0.05	1.3
H	0.02	1.3
I	0.1	2.54
J	IDENT	



	Inches	m.m.
A	0.35	8.9
B	0.3	7.6
C	0.5	12.7
D	0.55	14.0
E	0.06	1.5
F	0.06	1.5
G	0.05	1.3
H	0.02	0.5
I	0.1	2.54
J	IDENT	

FEATURES

* SMALL PHYSICAL SIZE
* C SUFFIX DEVICES TUNED TO CCIR TONESET
* Z SUFFIX DEVICES TUNED TO ZVEI TONESET
* WIDE TEMPERATURE RANGE
* HERMETICALLY SEALED PACKAGE
* LOW POWER CMOS PROCESS

GENERAL DESCRIPTION

FX003 PRODUCTS PACKAGED IN LEADLESS CHIP CARRIERS.

Products from the FX'03 range are available packaged in leadless chip carriers. This form of packaging can result in a greatly increased packing density.

The ceramic leadless chip carrier provides a high level of package hermeticity and wide operating and storage temperature ranges.

DESCRIPTION

The circuit function and electrical specification of leadless chip carrier products are identical to the dual-in-line product information with the following exceptions:

a) The FX003 tone decoder comprises two discrete LSI chips which are each packaged in a chip carrier. Both packages are required for a complete tone decoder, and are available to decode the CCIR or the ZVEI range of signalling tones. The product codes for a CCIR decoder are an FX102-K together with an FX202QC-K and for a ZVEI device are FX102-K and FX202QZ-K. The interconnection and external components of the two chip carriers are given in diagram 2.

The supply current taken by the FX102 and FX202 combined is typically 1200μA at 5 volts supply.

b) All chip carrier products are specified for operation over supply voltage range 4.5V to 6V.

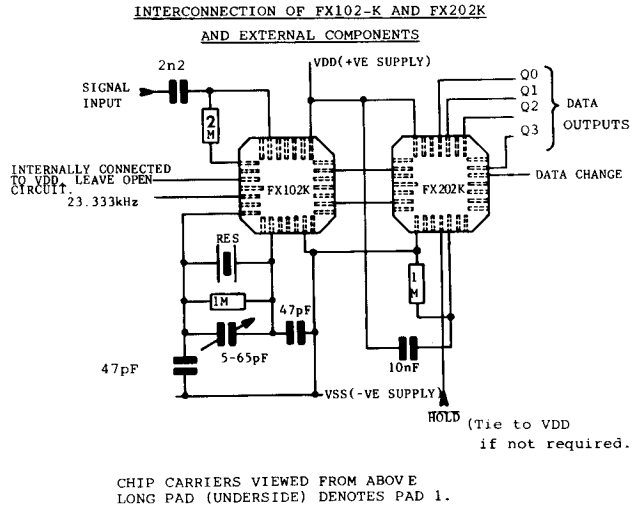


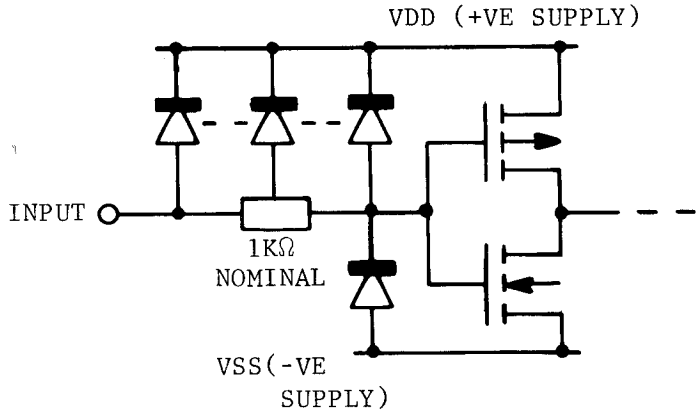
FIG.2

Methods of Attachment.

Leadless chip carriers may be attached by reflow soldering techniques. A typical reflow temperature would be 210°C and the molten solder tends to align the chip carrier over the solder pads on the substrate. The ideal substrate material is ceramic because it has a coefficient of linear expansion very closely matched to that of the carrier. Epoxy glass printed circuit boards can be used but the unmatched expansion coefficients lead to strain on the solder joints during cooling.

Handling Considerations.

Care should be taken when handling any CMOS product to minimise the possibility of the static electrical discharge into the input pins.



During storage the devices should be protected from static charges by packaging in conductive foam or storage in metal trays.

PIN DATA

PAD	FX102-K	FX202QC-K FX202QZ-K	FX103-K	FX313-K	FX403-K	FX503C-K FX503Z-K
1	N/C	N/C	Data Chng.I/P	VDD (+)	Data Chng.I/P	Tone O/P
2	23.333kHz I/P	N/C	PUR I/P	D0 I/P	PUR I/P	Tp O/P
3	N/C	93.333kHz I/P	Vss (-)	D1 I/P	Vss (-)	O/P Bias I/P
4	Osc. Bias	N/C	Alert R/S I/P	D2 I/P	Audio R/S I/P	N/C
5	N/C	Vss(-)	$\overline{\text{Dec.Abort}}$ I/P	D3 I/P	$\overline{\text{Decode}}$ I/P	Enable I/P
6	Osc. I/P	N/C	Preamble I/P	Data Chng.I/P	Tp. mode I/P	N/C
7	N/C	N/C	Alert O/P	23.333kHz I/P	Audio O/P	N/C
8	N/C	$\overline{\text{Hold}}$ I/P	23.333kHz I/P	PUR I/P	23.333kHz I/P	Data Chng.I/P
9	N/C	PUR I/P	$\overline{\text{Qp}}$ O/P	Load En. I/P	Inc.Add. I/P	Auto R I/P
10	Vss (-)	N/C	$\overline{\text{Q1}}$ O/P	$\overline{\text{Display}}$ I/P	Load O/P	N/C
11	N/C	N/C	$\overline{\text{Q2}}$ O/P	New Data O/P	Q0 O/P	N/C
12	N/C	N/C	$\overline{\text{Q3}}$ O/P	B Invalid I/P	Q1 O/P	N/C
13	93.333kHz O/P	N/C	$\overline{\text{Q4}}$ O/P	Overflow O/P	Q2 O/P	N/C
14	N/C	N/C	$\overline{\text{Q5}}$ O/P	Vss (-)	Q3 O/P	XTC/$\overline{\text{QTC}}$ I/P
15	N/C	N/C	D10 I/P	Digit 1 O/P	Dp0 I/P	Vss (-)
16	N/C	Data Chng.O/P	D11 I/P	Digit 2 O/P	Dp1 I/P	N/C
17	Logic sig.O/P	Q3 O/P	D12 I/P	Digit 3 O/P	Dp2 I/P	D0 I/P
18	N/C	N/C	D13 I/P	Digit 4 O/P	Dp3 I/P	D1 I/P
19	Vdd (+)	Q2 O/P	Group 'O'I/P	Digit 5 O/P	Tx Relay O/P	D2 I/P
20	N/C	N/C	A.C.I. I/P	Digit 6 O/P	Tx Enable I/P	D3 I/P
21	N/C	Q1 O/P	Mute O/P	Digit 7 O/P	Mute O/P	N/C
22	N/C	Q0 O/P	Mute R/S I/P	Segment g O/P	Mute R/S I/P	N/C
23	N/C	N/C	Vdd (+)	Segment f O/P	Vdd (+)	N/C
24	Signal I/P	N/C	Data Flag O/P	Segment e O/P	Data Flag O/P	$\overline{\text{Character}}$ I/P
25	N/C	Vdd (+)	D0 I/P	Segment d O/P	D0 I/P	N/C
26	Signal Bias	N/C	D1 I/P	Segment c O/P	D1 I/P	Clock I/P
27	N/C	Logic sig.I/P	D2 I/P	Segment b O/P	D2 I/P	$\overline{\text{Clock}}$ O/P
28	Internal Vdd	N/C	D3 I/P	Segment a O/P	D3 I/P	Vdd (+)

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