High Voltage Ring Generator IC

Features

- 220V maximum operating voltage
- Integrated high voltage transistors
- Up to $70V_{RMS}$ ring signal
- Pulse by pulse output over current protection
- 5 REN output capability
- External MOSFETs enhance output rating to 20 REN

Applications

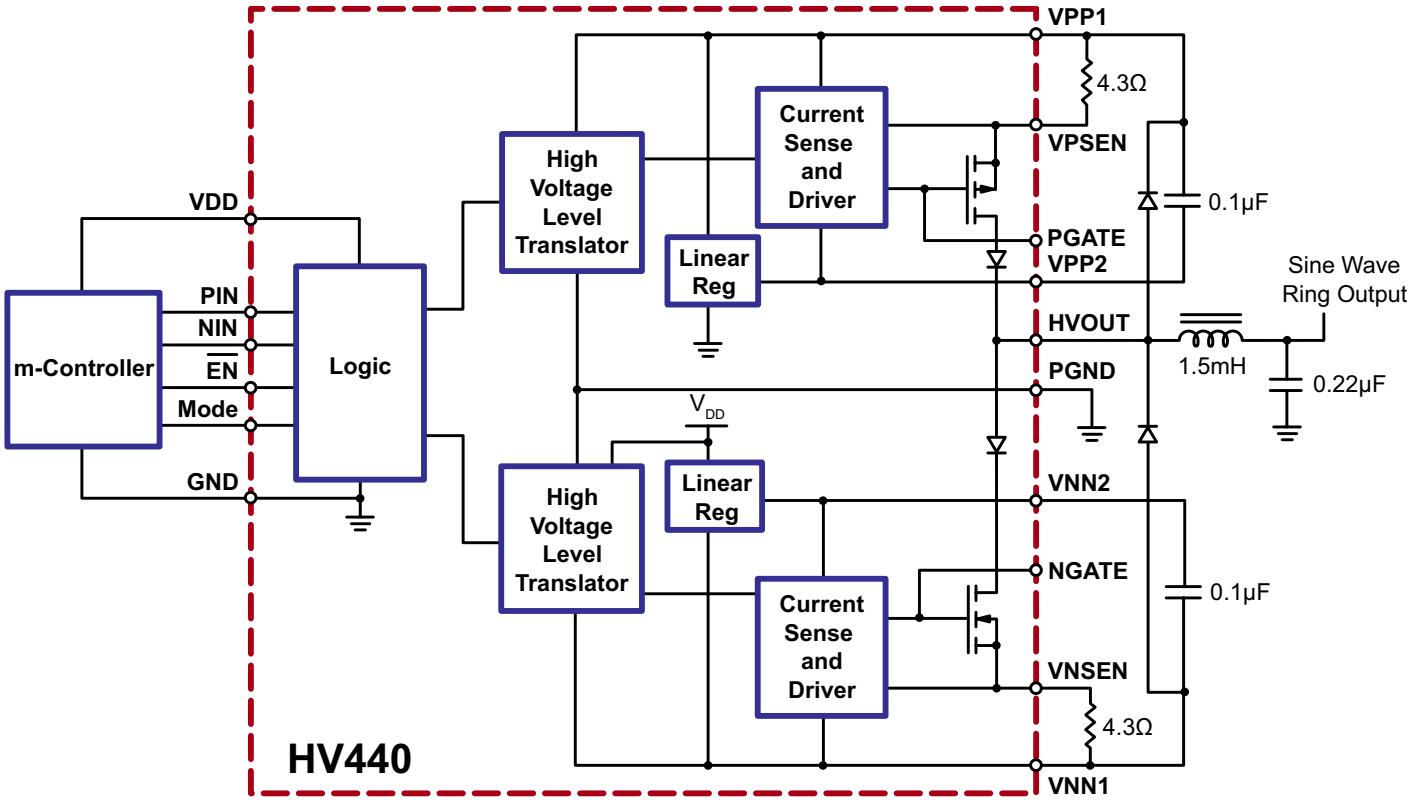
- Microcontroller or microprocessor controlled high voltage ring generator
- Set-top/street box ring generator
- Pair gain ring generator
- Wireless local loops
- Fibre in the loop/to the curb
- Coax cable loop

General Description

The Supertex HV440 is a monolithic integrated circuit capable of generating up to 70V RMS sine wave output at frequencies of 15 to 60Hz with a load of 5 North American RENs. Its out putrating can be enhanced to 20 North American RENs with the addition of two Supertex MOSFETs: one N-Channel MOSFET, the TN2524N8, and one P-Channel MOSFET, the TP2522N8.

The high voltage output P- and N-Channel transistors are controlled independently by the logic inputs PIN and NIN. Connecting the mode pin to ground will enable the device to be controlled with a single input, NIN. This adds a 200ns deadband on the control logic to avoid cross conduction on the high voltage output. A logic high on NIN will turn the high voltage P-Channel on and the N-Channel off. The high voltage outputs have pulse by pulse overcurrent protection set by two external sense resistors. Nominal PWM logic input frequency is 100KHz.

Typical Application Circuit

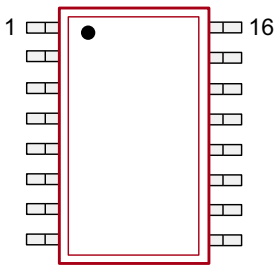


Ordering Information

Part Number	Package Option	Packing
HV440WG-G	16-Lead SOW	1000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Pin Configuration



16-Lead SOW (WG)
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{PP1} - V_{NN1}, power supply voltage	+240V
V_{PP1}, positive high supply voltage	+120V
V_{PP2}, positive gate supply voltage	+120V
V_{NN1}, negative high voltage	-170V
V_{NN2}, negative gate voltage	-170V
V_{DD}, logic supply voltage	+7.5V
Storage temperature	-65°C to +150°C
Power dissipation	800mW

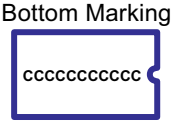
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

Top Marking



Bottom Marking



YY = Year Sealed
WW = Week Sealed
A = Assembler ID
L = Lot Number
C = Country of Origin*
——— = "Green" Packaging

** May be part of top marking*

Package may or may not include the following marks: Si or 

16-Lead SOW (WG)

Typical Thermal Resistance

Package	θ_{ja}
16-Lead SOW	66°C/W

Electrical Characteristics *(over operating supply voltage unless otherwise specified. T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PP1}	High voltage positive supply	15	-	110	V	T_A = -40°C to +85°C
V_{PP2}	Positive linear regulator output	V_{PP1} -9.9	-	V_{PP1} -19.1		
V_{NN1}	High voltage negative supply	V_{PP1} -220	-	-110		
V_{NN2}	Negative linear regulator output	V_{PP1} +5.6	-	V_{NN1} +10.5		
V_{DD}	Logic supply	4.5	-	5.5		
I_{PP1Q}	V_{PP1} quiescent current	-	250	400	µA	P_{IN} = N_{IN} = 0V, T_A = -40°C to +85°C
I_{NN1Q}	V_{NN1} quiescent current	-	250	550		
I_{DDQ}	V_{DD1} quiescent current	-	-	150	µA	P_{IN} = N_{IN} = 0V, MODE = 0
		-	-	60		P_{IN} = N_{IN} = 0V, MODE = 1
I_{PP1}	V_{PP1} operating current	-	-	1.7	mA	No load, V_{OUTP} and V_{OUTN} switching at 100KHz, T_A = -40°C to +85°C

Electrical Characteristics *(cont.)* *(over operating supply voltage unless otherwise specified. T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{NN1}	V_{NN1} operating current	-	-	1.9	mA	No load, V_{OUTP} and V_{OUTN} switching at 100KHz, T_A = -40°C to +85°C
I_{DD}	V_{DD} operating current	-	-	1.0	mA	---
I_{IL}	Mode logic input low current	-	25	-	µA	MODE = 0V
V_{IL}	Logic input low voltage	0	-	1.0	V	V_{DD} = 5.0V
V_{IH}	Logic input high voltage	4.0	-	5.0	V	V_{DD} = 5.0V

High Voltage Output

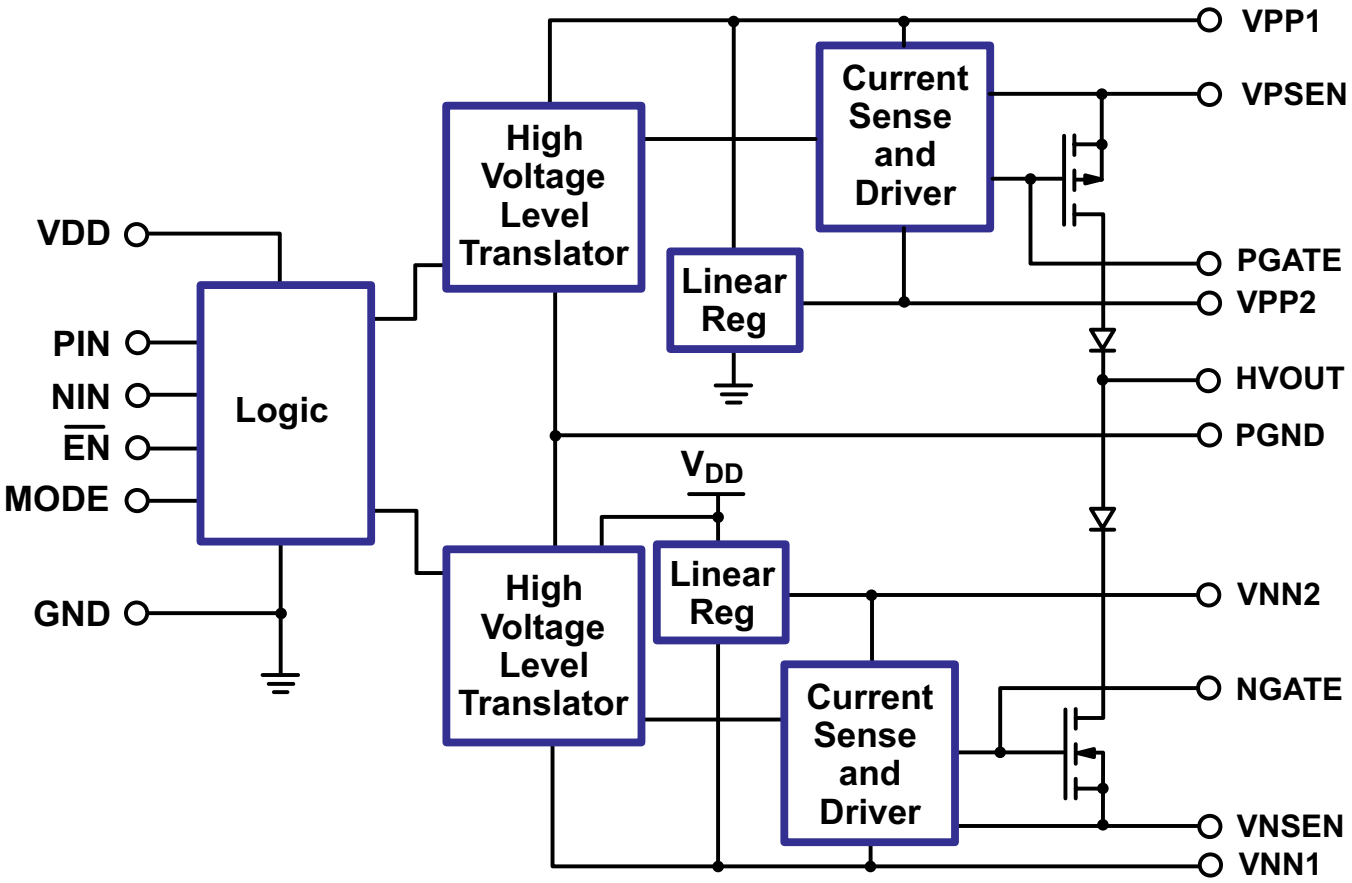
R_{SOURCE}	V_{OUT}P source resistance	-	60	80	Ω	I_{OUT} = 100mA
R_{SINK}	V_{OUT}P sink resistance	-	60	80	Ω	I_{OUT} = -100mA
ΔR/ΔT	Change in source/sink resistance over temperature	-	0.33	-	Ω/°C	T_A = -40°C to +85°C
$t_{D(ON)}$	HV_{OUT} delay time	-	150	-	ns	P_{IN} = high to low, Mode = high
t_{RISE}	HV_{OUT} rise time	-	-	50	ns	P_{IN} = high to low
$t_{D(OFF)}$	HV_{OUT} delay time	-	200	-	ns	N_{IN} = low to high, Mode = high
t_{FALL}	HV_{OUT} fall time	-	-	50	ns	N_{IN} = low to high
t_{DB}	Logic deadband time	-	-	200	ns	Mode = low
V_{PSEN}	HV_{OUT} current source sense voltage	V_{PP1} -0.75	V_{PP1} -1.00	V_{PP1} -1.25	V	T_A = -40°C to +85°C
		V_{PP1} -0.67	-	V_{PP1} -1.31		
V_{NSEN}	HV_{OUT} current sink sense voltage	V_{NN1} +0.75	V_{NN1} +1.00	V_{NN1} +1.25	V	T_A = -40°C to +85°C
		V_{NN1} +0.65	-	V_{NN1} +1.33		
t_{SHORTP}	HV_{OUT} off time when current source sense is activated	-	-	100	ns	---
t_{SHORTN}	HV_{OUT} off time when current sink sense is activated	-	-	100	ns	---
t_{WHOUT}	Minimum pulse width for HV_{OUT} at V_{PP1}	-	-	500	ns	T_A = -40°C to +85°C
t_{WLOUT}	Minimum pulse width for HV_{OUT} at V_{NN1}	-	-	500	ns	T_A = -40°C to +85°C

Truth Table

N_{IN}	P_{IN}	Mode	$\overline{EN}$	HV_{OUT}
L	L	H	L	VPP1
L	H	H	L	High Z
H	L*	H	L	–
H	H	H	L	VNN1
L	X	L	L	VNN1
H	X	L	L	VPP1
X	X	X	H	High Z

* *This state will short V_{PP1} to V_{NN1} and should therefore be avoided.*

Block Diagram

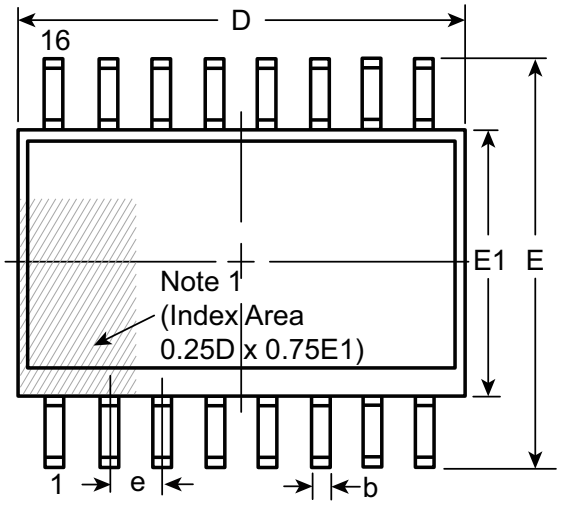


Pin Description

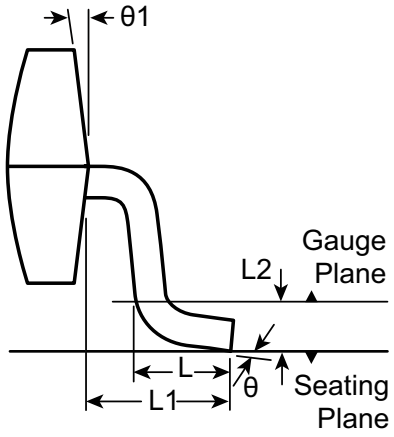
Pin	Name	Description
1	VPP1	Positive high voltage supply.
2	PGND	High voltage power ground.
3	GND	Low voltage ground.
4	MODE	Logic mode input. Logic low activates 200nsec deadband. When mode is low, NIN turns on and off the high voltage N- and P-Channels. Pin is not used and should be connected to VDD or ground.
5	PIN	Logic control input. When mode is high, logic input high turns off output high voltage P-Channel.
6	NIN	Logic control input. When mode is high, logic input high turns on output high voltage N-Channel.
7	$\overline{EN}$	Active low enable input.
8	VDD	Logic supply voltage.
9	VNN1	Negative high voltage supply.
10	VNN2	Negative gate voltage supply. Generated by an internal linear regulator. A 0.1µF capacitor should be connected between VNN2 and VNN1.
11	NGATE	Gate drive for external N-channel MOSFET.
12	VNSEN	Pulse by pulse over current sensing for internal N-Channel MOSFET.
13	HVOUT	High voltage output. Voltage swings from VPP1 to VNN1.
14	VPSEN	Pulse by pulse over current sensing for internal P-Channel MOSFET.
15	PGATE	Gate drive for external P-channel MOSFET.
16	VPP2	Positive gate voltage supply. Generated by an internal linear regulator. A 0.1µF capacitor should be connected between VPP2 and VPP1.

16-Lead SOW (Wide Body) Package Outline (WG)

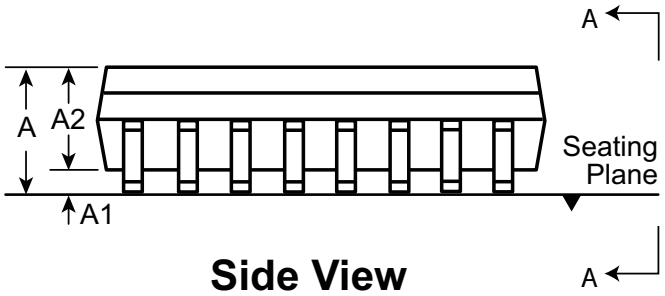
10.30x7.50mm body, 2.65mm height (max), 1.27mm pitch



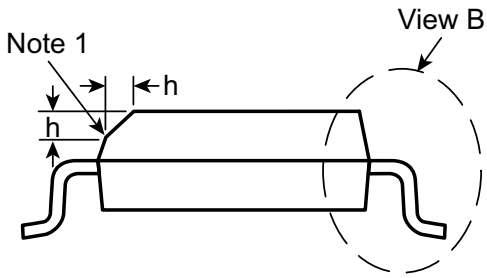
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	10.10*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	10.30	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	10.50*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AA, Issue E, Sep. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: DSPD-16SOWWG, Version E041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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