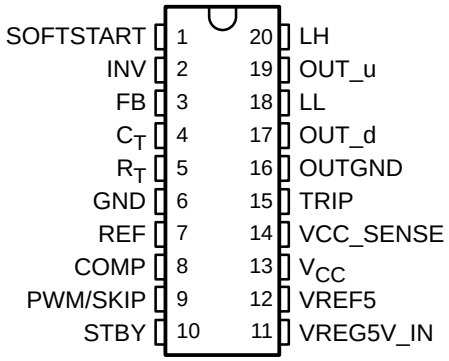
- **Step-Down DC-DC Converter**
- **Three Operation-Modes**
  - **Heavy Load:**
    - **Fixed Frequency PWM**
    - **Hysteretic (User Selectable)**
  - **Light Load:**
    - **Skip Mode**
- **4.5-V to 25-V Input Voltage Range**
- **Adjustable Output Voltage Down to 1.2 V**
- **95% Efficiency**
- **Standby Control**
- **Overcurrent Protection**
- **UVLO for Internal 5-V Regulation**
- **Low-Standby Current . . . 0.5 mA Typical**
- **T_A = –40°C to 85°C**

DB PACKAGE
(TOP VIEW)



description

The TPS5103 is a synchronous buck dc/dc controller, designed for notebook PC system power. The controller has three user-selectable operation modes available: hysteretic mode, fixed-frequency PWM control, or SKIP control.

In high-current applications, where fast transient response is advantageous for reducing bulk capacitance, the hysteretic mode is selected by connecting the R_T pin to VREF5. Selecting the PWM/SKIP modes for less demanding transient applications is ideal for conserving notebook battery life under light load conditions. The device includes high-side and low-side MOSFET drivers capable of driving low $r_{ds(on)}$ N-channel MOSFETs.

The user-selectable overcurrent protection (OCP) threshold is set by an external TRIP-pin resistor in order to protect the system. The TPS5103 is configured so that a current-sense resistor is not required, improving the operating efficiency.

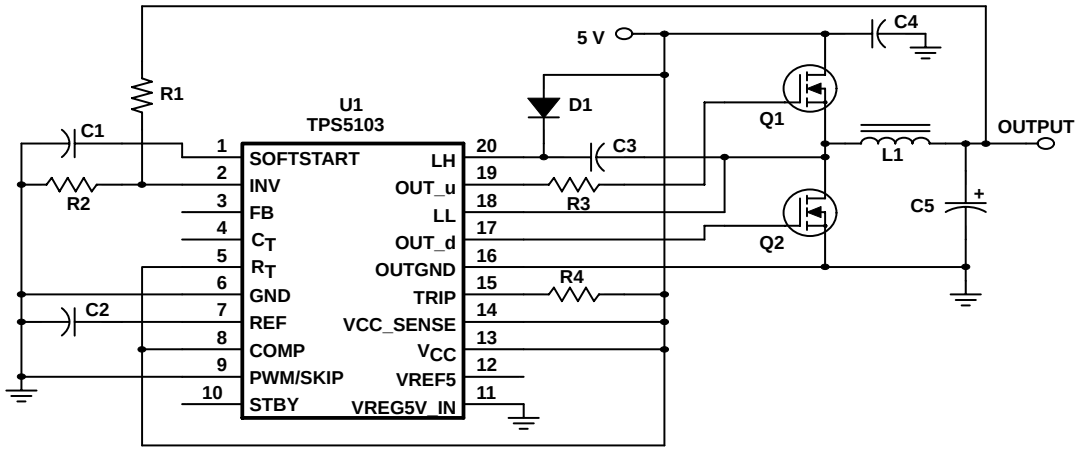


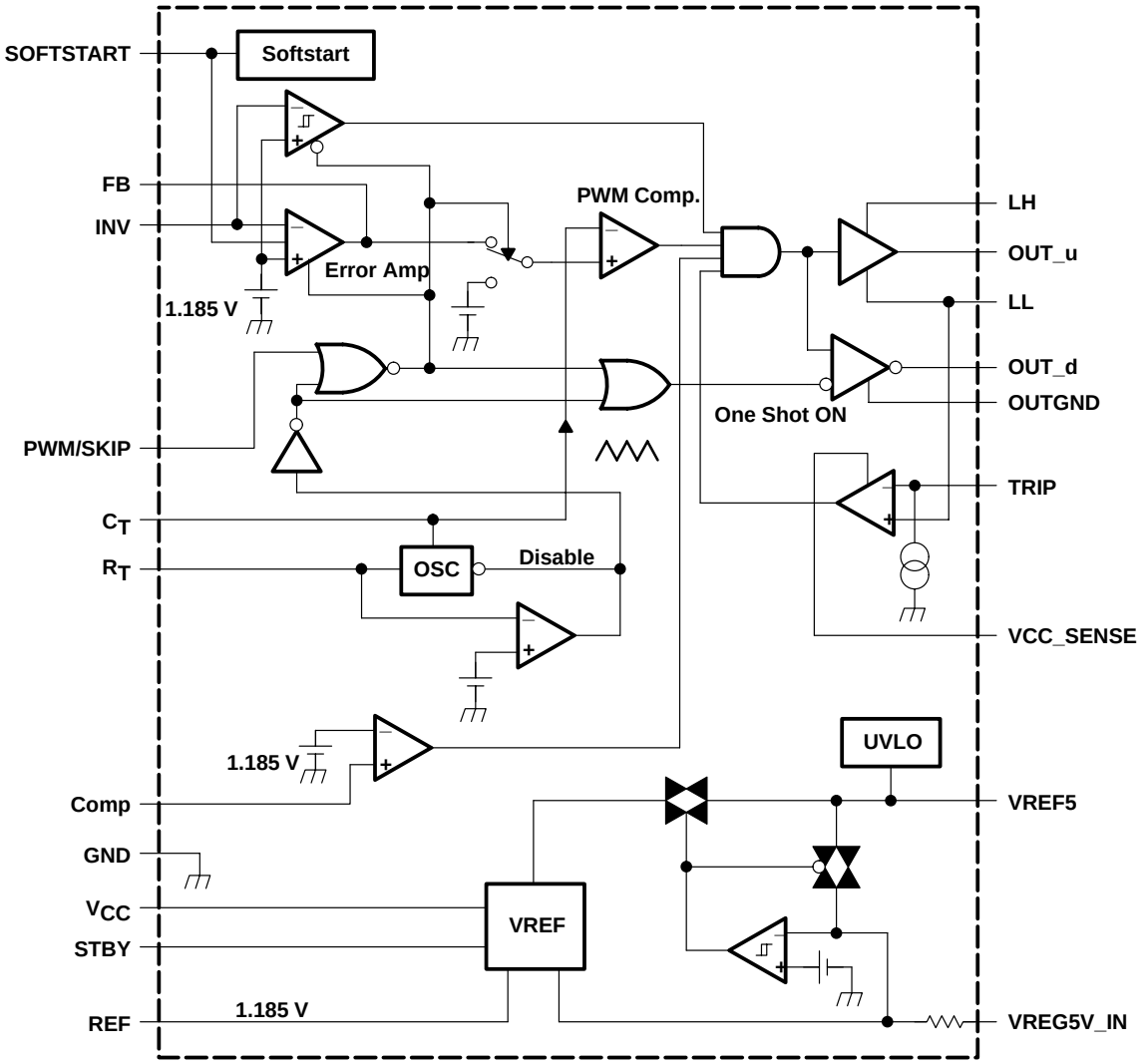
Figure 1. Typical Design

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE	
	SSOP(DB)	EVM
–40°C to 85°C	TPS5103IDB	TPS5103EVM–136
	TPS5103IDBR	

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
COMP	8	I	Comparator input for voltage monitor
C_T	4	I/O	External capacitor from C_T to GND for adjusting the triangle oscillator and decreasing the current-limiting voltage
FB	3	O	Feedback output of error amp
GND	6		Control GND
INV	2	I	Inverting input of both error amp and hysteretic comparator
LH	20	I/O	Bootstrap. Connect a 1 μF, low-ESR capacitor from LH to LL.
LL	18	I/O	Bootstrap low. High-side gate driving return and output-current protection. Connect to the junction of the high-side and low-side FETs for a floating drive configuration.
OUT_d	17	I/O	Gate-drive output for low-side power switching FETs
OUTGND	16		Ground for FET drivers
OUT_u	19	O	Gate-drive output for high-side power switching FETs
PWM/SKIP	9	I	PWM/SKIP mode select L:PWM mode H:SKIP mode
REF	7	O	1.185-V reference voltage output
R_T	5	I/O	External resistor connection for adjusting the triangle oscillator.
SOFTSTART	1	I	External capacitor from SOFTSTART to GND for soft-start control
STBY	10	I	Standby control
TRIP	15	I	External resistor connection for output-current control
V_{CC}	13	I	Supply-voltage input
VCC_SENSE	14	I	Supply voltage sense for current protection
VREF5	12	O	5-V internal regulator output
VREG5V_IN	11	I	External 5-V input (input voltage range = 4.5 V to 25 V)

detailed description

REF

The reference voltage is used for the output voltage setting and the voltage protection(COMP). The tolerance is 1.5% typically.

VREF5

An internal linear voltage regulator is used for the high-side driver bootstrap voltage. Since the input voltage range is from 4.5 V to 25 V, this voltage offers a fixed voltage for the bootstrap voltage so that the design for the bootstrap is much easier. The tolerance is 6%.

hysteretic comparator

The hysteretic comparator is used to regulate the output voltage of the synchronous-buck converter. The hysteresis is set internally and is typically 9.7 mV. The total delay time from the comparator input to the driver output is typically 400 ns for going both high and low.

error amplifier

The error amplifier is used to sense the output voltage of the synchronous buck converter. The negative input of the error amplifier is connected to the VREF (1.185 V) with a resistive divider network. The output of the error amplifier is brought out to the FB terminal to be used for loop-gain compensation.

low-side driver

The low-side driver is designed to drive low-$r_{ds(on)}$ n-channel MOSFETs. The maximum drive voltage is 5 V from VREF5. The current rating of the driver is typically 1.2 A at sink current, and –1.5 A at source current.

high-side driver

The high-side driver is designed to drive low-$r_{ds(on)}$ n-channel MOSFETs. The current rating of the driver is 1.2 A at sink current, and –1.7 A at source current. When configured as a floating driver, the bias voltage to the driver is developed from VREF5, limiting the maximum drive voltage between OUT_u and LL to 5 V. The maximum voltage that can be applied between LH and OUTGND is 30 V.

driver deadtime control

The deadtime control prevents shoot-through current from flowing through the main power FETs. During switching transitions the deadtime control actively controls the turnon time of the MOSFET drivers. The typical deadtime from the low-side-driver-off to the high-side-driver-on is 90 ns, and 110 ns from high-side-driver-off to low-side-driver-on.

COMP

COMP is designed for use with a regulation-output monitor. COMP also functions as an internal comparator used for any voltage protection such as the input under voltage protection. If the input voltage is lower than the setpoint, the comparator turns off and prevents external parts from being damaged. The investing terminal of the comparator is internally connected to REF (1.185 V).

current protection

Current protection is achieved by sensing the high-side power MOSFET drain-to-source voltage drop during on-time through VCC_SENSE and LL terminals. An external resistor between VREG5V_IN and TRIP, with the an internal current source connected to the current comparator negative input, adjusts the current limit. The typical internal current source value is 15 μA in PWM mode, and 5 μA in SKIP mode. When the voltage on the positive terminal is lower than the negative terminal, the current comparator turns on the trigger, and then activates the oscillator. This oscillator repeatedly resets the trigger until the overcurrent condition is removed. The capacitor on the C_T terminal can be open or added to adjust the reset frequency.

detailed description (continued)

softstart

SOFTSTART sets the sequencing of the output for any possibility. The capacitor value for a start-up time can be calculated by the following equation:

$C = 2 \times T\ (\mu F)$

Where C is the external capacitor value, and T is the required start-up time in (ms).

standby

The controller can be switched into the standby mode by grounding the STBY terminal. When it is in standby mode, the quiescent current is less than 1.0 μA.

UVLO

The under-voltage lockout (ULVO) threshold is approximately 3.8 V. The typical hysteresis is 55 mV.

5-V switch

If the internal 5-V switch senses a 5-V input from REG5V, the internal 5-V linear regulator will be disconnected from the MOSFET drivers. The external 5 V will be used for both the low-side driver and the high-side bootstrap, thus, increasing the efficiency.

PWM/SKIP switch

The PWM/SKIP switch selects the output operating mode. This controller has three operational modes, PWM, SKIP, and hysteretic. The PWM and SKIP mode control should be used for slower-transient applications.

oscillator

The oscillator gives a triangle wave by connecting an external resistor to R_T and an external capacitor to C_T. The voltage amplitude is 0.43 V ~ 1.17 V. This wave is connected to the noninverting input of the PWM comparator.

Table 1. Comparison Table Between PWM Mode and Hysteretic Mode

MODE	PWM	HYSTERETIC
Frequency	Fixed	Not fixed
Transient response	Normal	Very fast
Feed back compensation	Need	Needless

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . –0.3 V to 27 V
Input voltage, V_I, INV, C_T, R_T, PWM/SKIP, SOFTSTART, COMP . . . . . –0.3 V to 7 V
Input voltage, VREG5V_IN . . . . . –0.3 V to 6 V
Input voltage, STBY . . . . . –0.3 V to 15 V
Input voltage, TRIP, VCC_SENSE . . . . . –0.3 V to 27 V
Output current, I_O . . . . . 3 A
Low-level output voltage, V_{OL} . . . . . –0.3 V to 27 V
High-level output voltage, V_{OH} . . . . . –0.3 V to 32 V
Reference voltage, V_{ref} . . . . . –0.3 V to 3 V
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating virtual junction temperature range, T_J . . . . . –125°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. See Dissipation Rating Table for free-air temperature range above 25°C.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DB	801 mW	6.408mW/°C	416 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		25	V
V_I	Input voltage	INV, C_T, R_T, COMP, PWM/SKIP, SOFTSTART			6	V
		VREG5V_IN			5.5	
		STBY			12	
		TRIP, VCC_SENSE			25	
$R_{(T)}$	Oscillator frequency	Timing register		82		kΩ
$C_{(T)}$		Timing capacitor		100		pF
f		Frequency		200		kHz
T_A	Operating temperature range		–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted)

reference voltage

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage	T_A = 25°C,	I_{vref} = 50 µA	1.167	1.185	1.203	V
		I_{vref} = 50 µA		1.155		1.215	
Regin†	Line regulation	V_{CC} = 4.5 V to 25 V,	I = 50 µA		0.2	12	mV
Regl†	Load regulation	I = 1 µA to 1 mA			0.5	10	mV

† Not a JEDEC symbol.

oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Frequency	PWM mode			500	kHz
$R_{(T)}$	Timing resistor		47			kΩ
fdv†	Frequency change	V_{CC} = 4.5 V to 25 V		0.1%		
fdt†		T_A = –40°C to 85°C		2%		
V_{OH}	High-level output voltage‡	DC includes internal comparator error	1	1.1	1.2	V
		f = 200 kHz, includes internal comparator error		1.17		
V_{OL}	Low-level output voltage‡	DC includes internal comparator error	0.4	0.5	0.6	V
		f = 200 kHz, includes internal comparator error		0.43		

† Not a JEDEC symbol.
‡ The output voltages of oscillator (f = 200 kHz) are ensured by design.

error amp

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	T_A = 25°C		2	10	mV
Av†	Open-loop voltage gain		50			dB
GB†	Unity-gain bandwidth			0.8		MHz
I_O	Output sink current	V_O = 0.4 V	30	45		µA
I_S	Output source current	V_O = 1 V		300		µA

† Not a JEDEC symbol.

hysteresis comparator§

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Hysteresis window	Hysteretic mode	6	9.7	13	mV
Vp-V_S	Offset voltage			2		mV
I	Bias current			10		pA
t_{PHL}	Propagation delay from INV to OUT_U	TTL input signal		230		ns
t_{PLH}	Propagation delay time, low-to-high	10-mV overdrive on hysteresis band signal		400		ns

§ The numbers in the table include the driver delay. All numbers are ensured by design.

control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IHA}	High-level input voltage	STBY	2.5			V
		PWM/SKIP	2			
V_{ILA}	Low-level input voltage	STBY			0.5	V
		PWM/SKIP			0.5	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

5-V regulator

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	I = 10 mA		4.7		5.3	V
Regin†	Line regulation	V_{CC} = 5.5 V to 25 V,	I = 10 mA			20	mV
Regl†	Load regulation	I = 1 mA to 10 mA,	V_{CC} = 5.5 V			40	mV
I_{OS}	Short-circuit output current	V_{ref} = 0 V			70		mA

† Not a JEDEC symbol.

5-V switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(high)}$	Threshold voltage		4.2		4.9	V
$V_{IT(low)}$			4.1		4.8	
V_{hys}	Hysteresis		50	150	250	mV

UVLO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(high)}$	Threshold voltage		3.6		4.2	V
$V_{IT(low)}$			3.5		4.1	
V_{hys}	Hysteresis		10		150	mV

output

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	OUT_u sink current	V_O = 3 V		0.5	1.2		A
I_S	OUT_u source current	V_O = 2 V		–1	–1.7		A
I_O	OUT_d sink current	V_O = 3 V		0.5	1.2		A
I_S	OUT_d source current	V_O = 2 V		–1	–1.5		A
I	TRIP terminal current	PWM mode,	$V_{(TRIP)}$ = 7 V	10	15	20	µA
		SKIP mode,	$V_{(TRIP)}$ = 7 V	3	5	7	
t_r	Rise time	High-side driver is GND referenced.					ns
		Input: INV = 0 – 3V					
		t_r/t_f = 10 ns,	Frequency = 200 kHz				
		C_L = 2200 pF			28		
		C_L = 3300 pF			39		
t_f	Fall time	High-side driver is GND referenced.					ns
		Input: INV = 0 – 3 V					
		t_r/t_f = 10 ns,	Frequency = 200 kHz				
		C_L = 2200 pF			30		
		C_L = 3300 pF			38		

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

softstart

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(CTRL)}$	Softstart current		1.9	2.5	3	μA
$V_{IT(high)}$	Threshold voltage (SKIP mode)			3.9		V
$V_{IT(low)}$				2.6		

output voltage monitor

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT}	Threshold voltage		1.08	1.18	1.28	V

driver deadtime section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(DRVLH)}$	Low side to high side			90		ns
$T_{(DRVHL)}$	High side to low side			110		ns

whole device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current			0.5	1.2	mA
$I_{O(sd)}$	Shutdown current	STBY = 0 V		0.01	10	μA

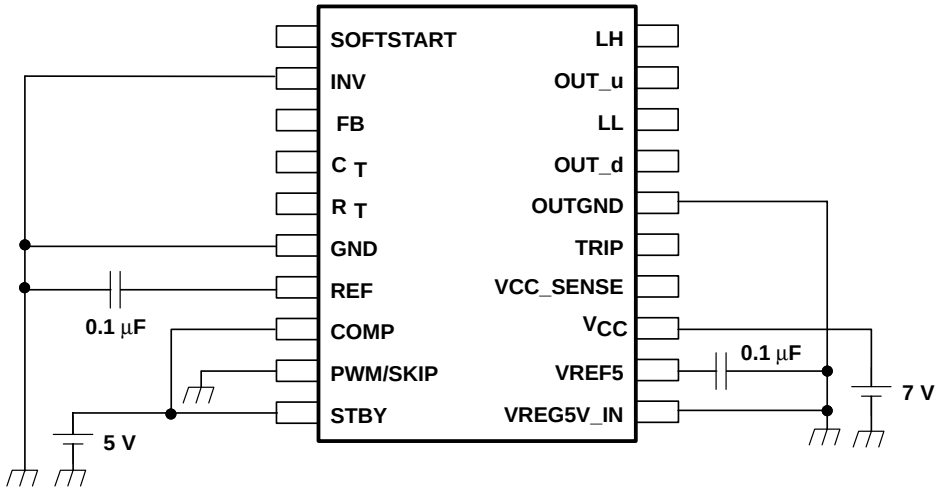


Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT vs JUNCTION TEMPERATURE

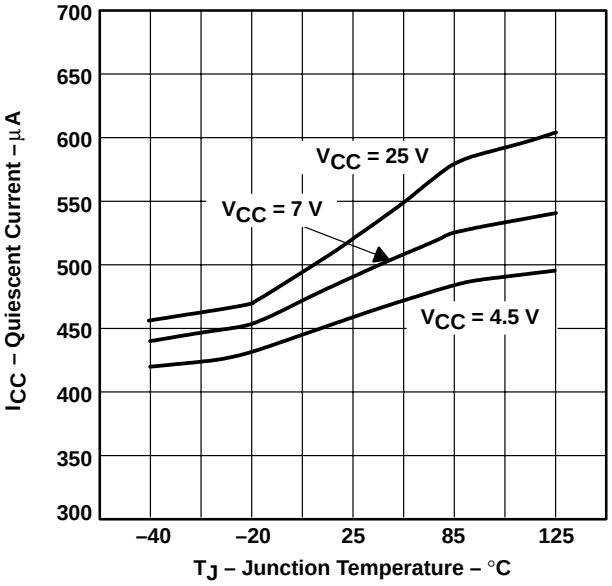


Figure 3

QUIESCENT CURRENT vs JUNCTION TEMPERATURE

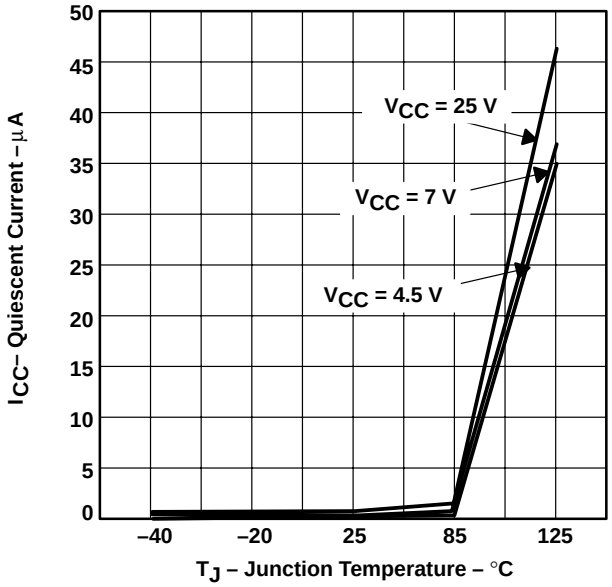


Figure 4

DRIVE OUTPUT VOLTAGE vs DRIVE SOURCE CURRENT

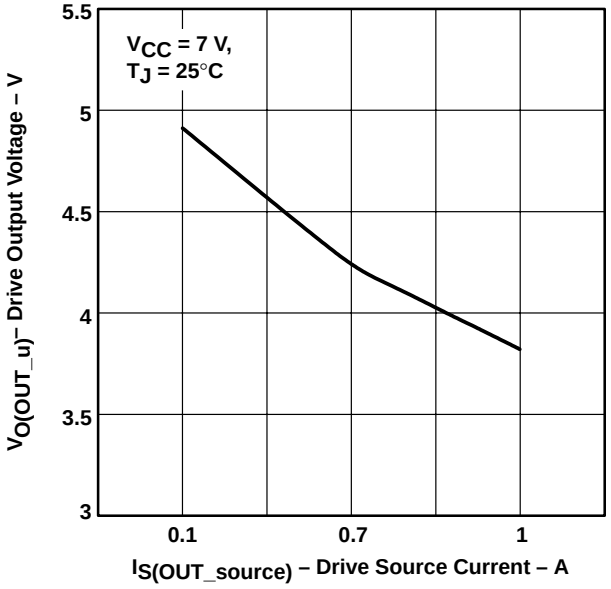


Figure 5

DRIVE OUTPUT VOLTAGE vs DRIVE SOURCE CURRENT

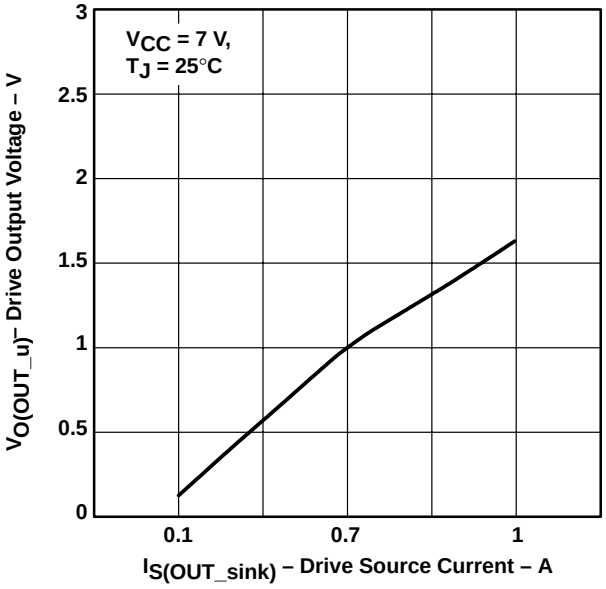


Figure 6

TYPICAL CHARACTERISTICS

DRIVE OUTPUT VOLTAGE vs DRIVE SOURCE CURRENT

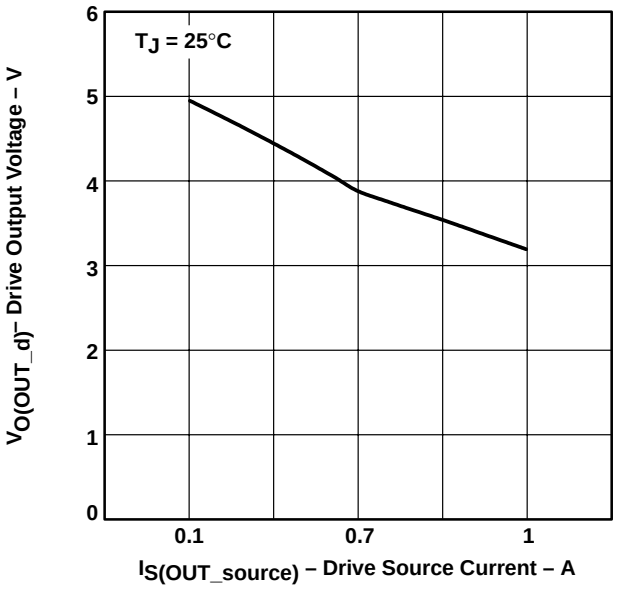


Figure 7

DRIVE OUTPUT VOLTAGE vs DRIVE SOURCE CURRENT

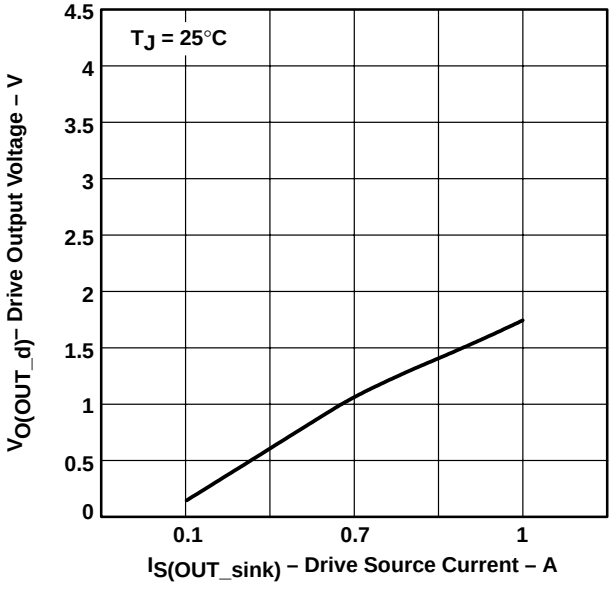


Figure 8

OSCILLATOR OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

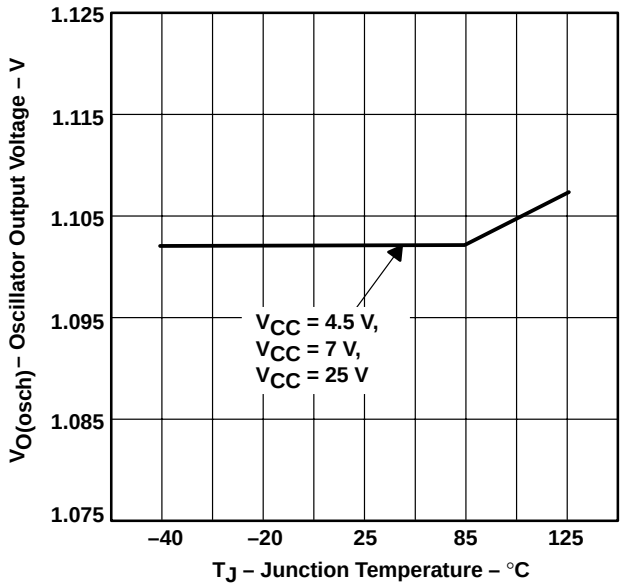


Figure 9

OSCILLATOR OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

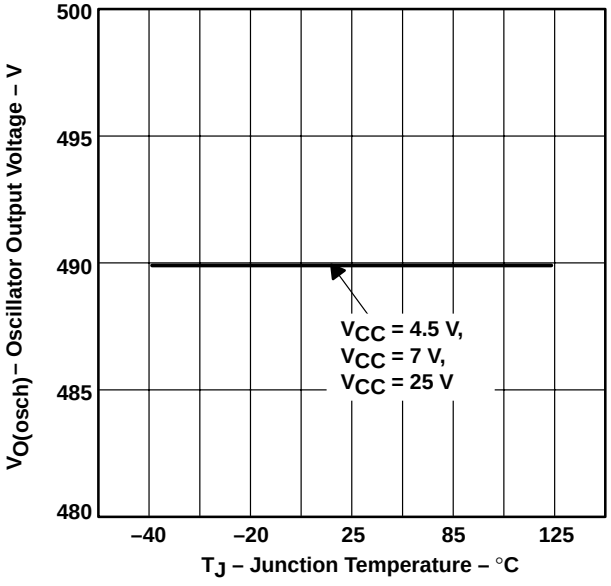


Figure 10

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER INPUT OFFSET VOLTAGE vs JUNCTION TEMPERATURE

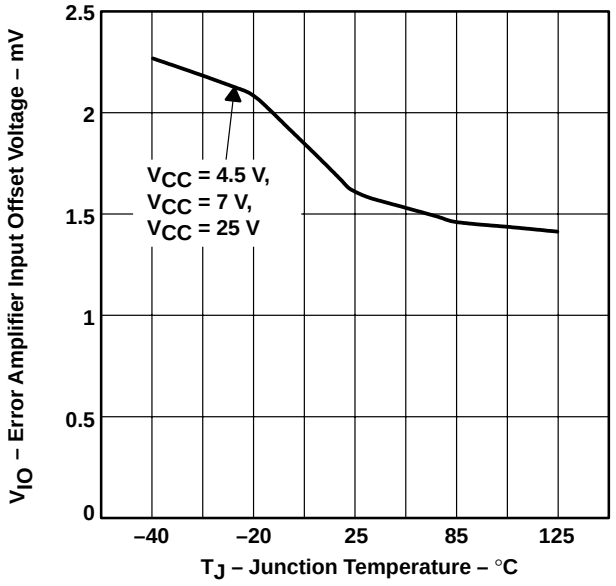


Figure 11

ERROR AMPLIFIER OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

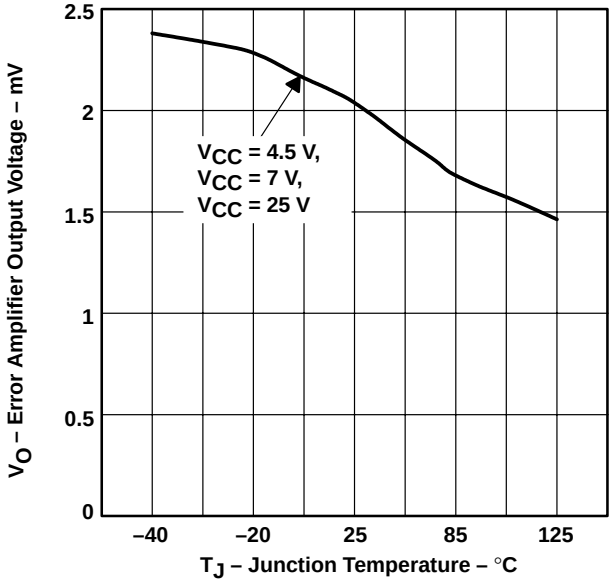


Figure 12

ERROR AMPLIFIER OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

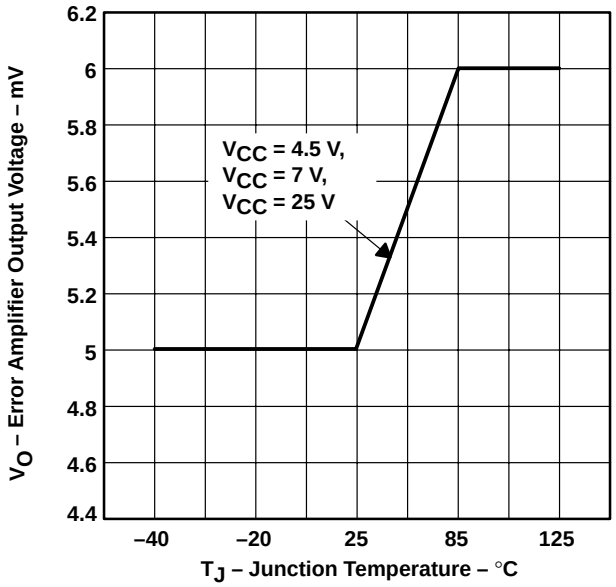


Figure 13

HYSTERESIS COMPARATOR HYSTERESIS VOLTAGE vs JUNCTION TEMPERATURE

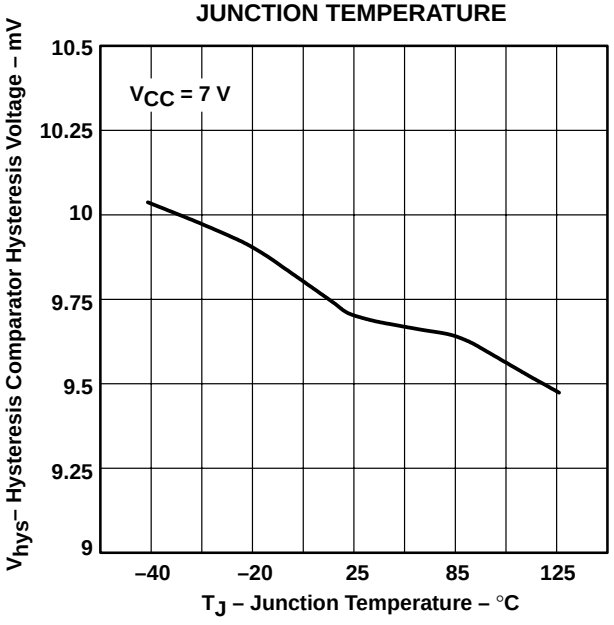


Figure 14

TYPICAL CHARACTERISTICS

STANDBY SWITCH THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

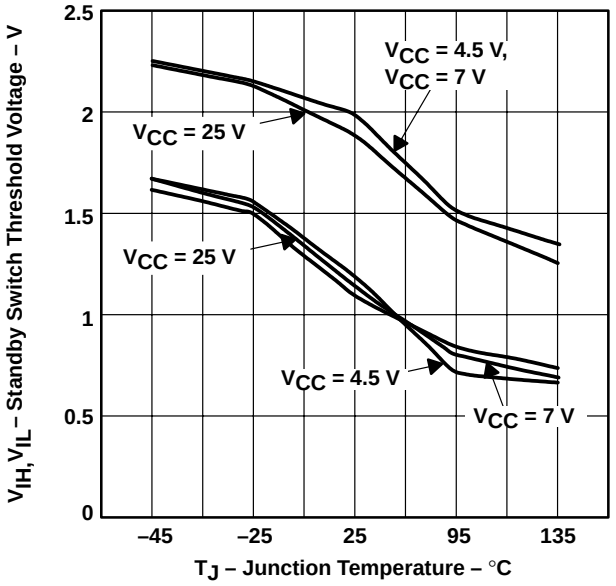


Figure 15

VREF5 OUTPUT VOLTAGE vs SUPPLY VOLTAGE

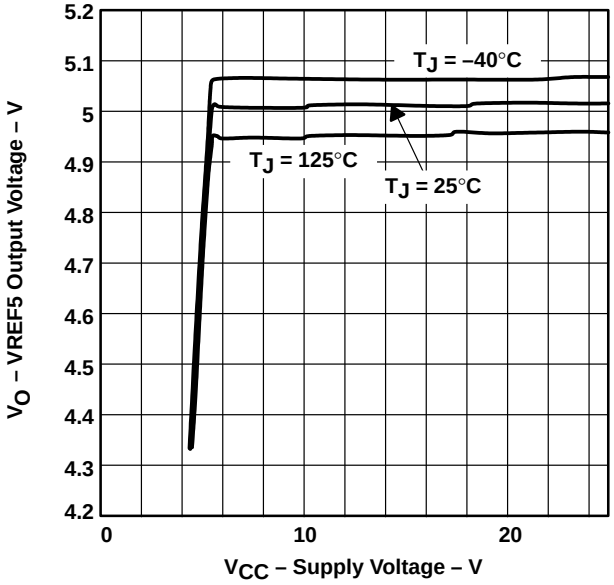


Figure 16

VREF5 OUTPUT VOLTAGE vs OUTPUT CURRENT

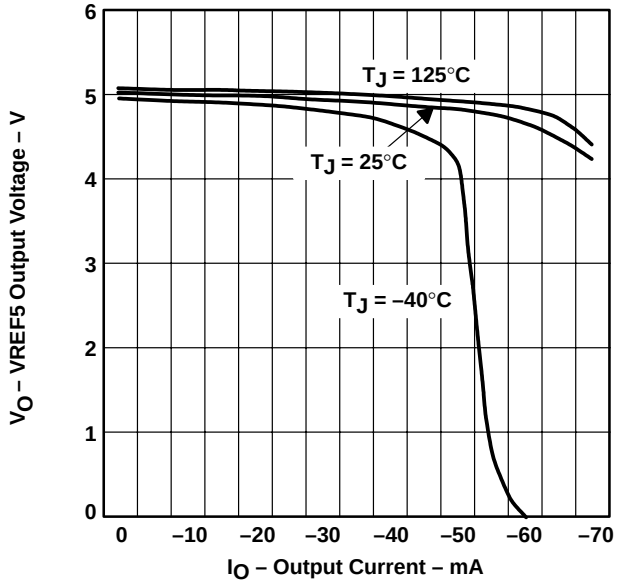


Figure 17

VREF5 SHORT CURRENT vs JUNCTION TEMPERATURE

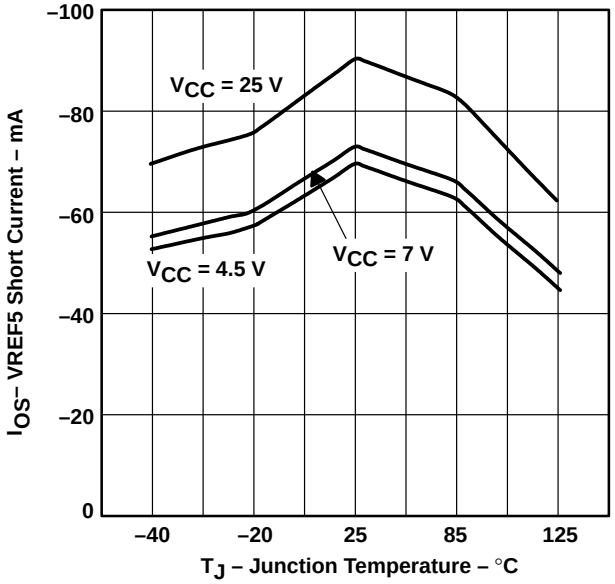


Figure 18

TYPICAL CHARACTERISTICS

UVLO THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

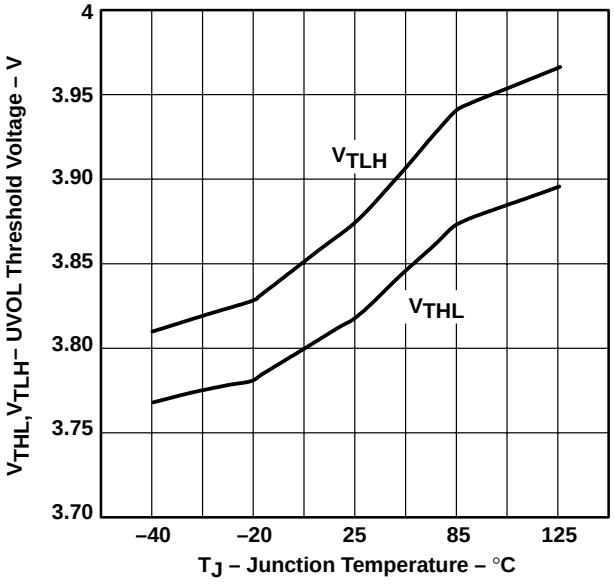


Figure 19

UVLO HYSTERESIS VOLTAGE vs JUNCTION TEMPERATURE

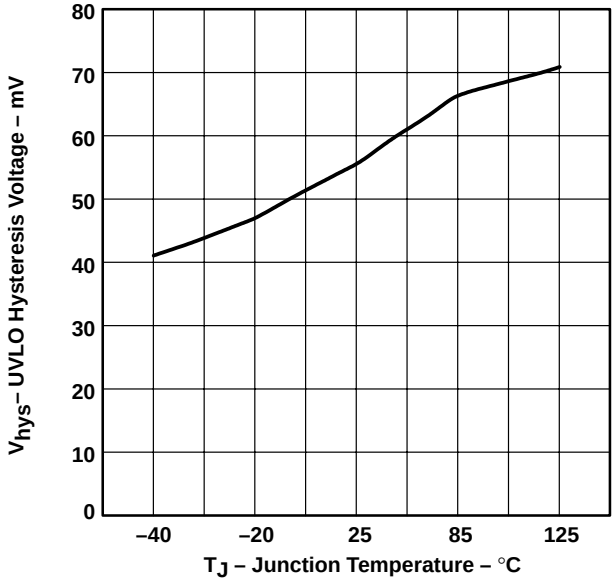


Figure 20

5 VSW THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

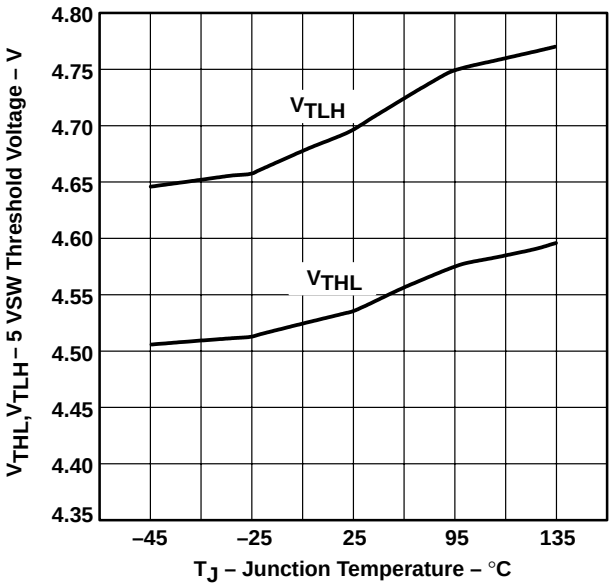


Figure 21

5 VSW HYSTERESIS VOLTAGE vs JUNCTION TEMPERATURE

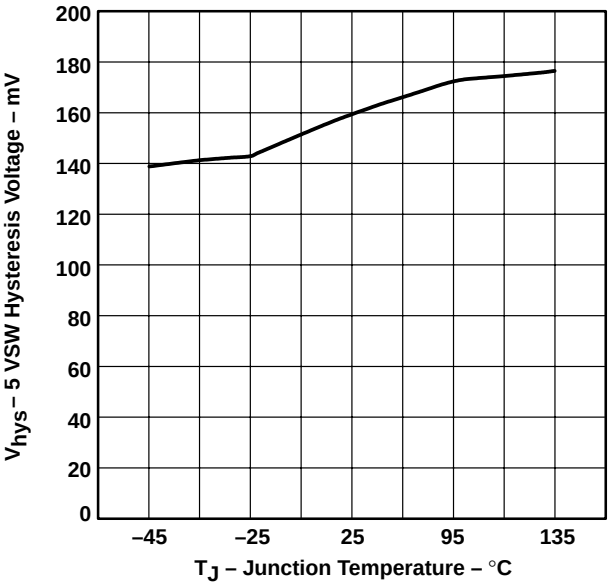


Figure 22

TYPICAL CHARACTERISTICS

SOFTSTART CURRENT vs JUNCTION TEMPERATURE

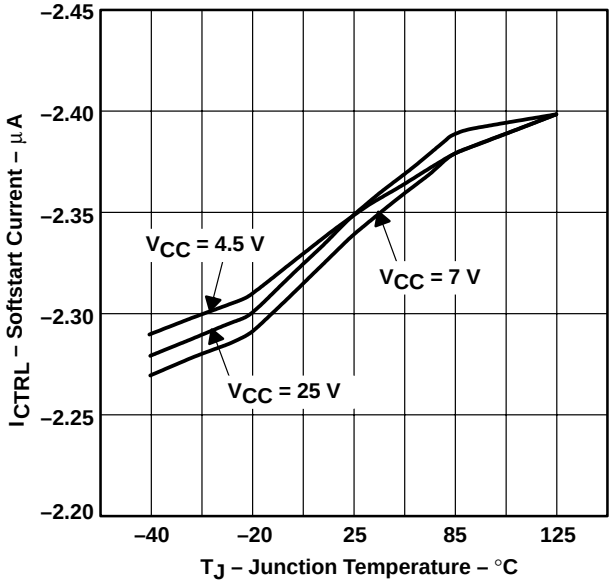


Figure 23

SOFTSTART THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

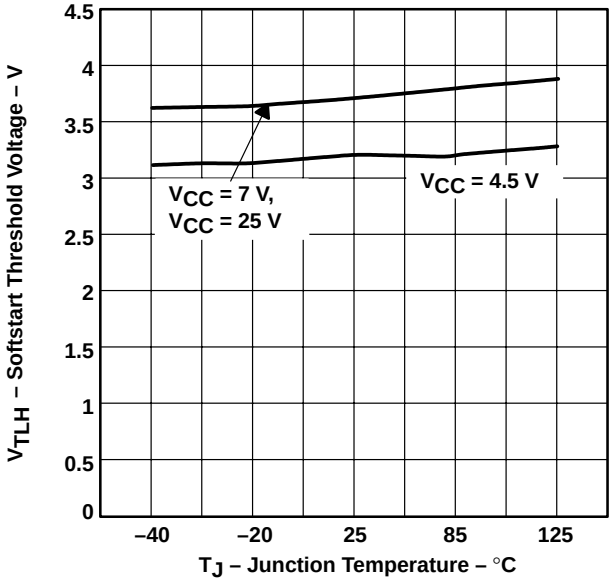


Figure 24

SOFTSTART THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

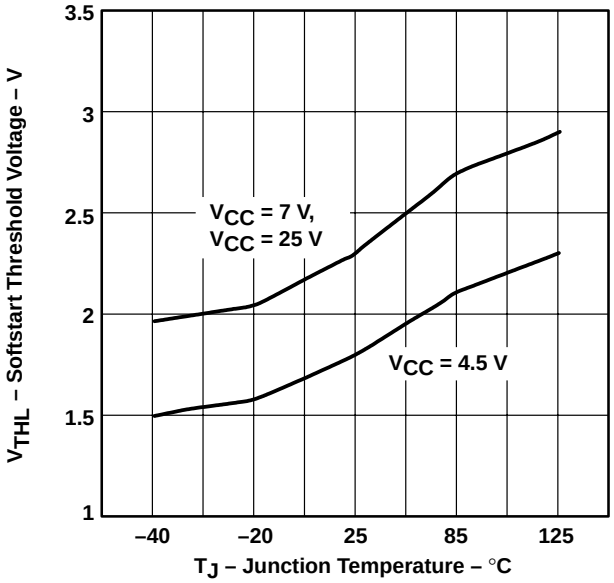


Figure 25

OUTPUT VOLTAGE MONITOR COMPARATOR THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

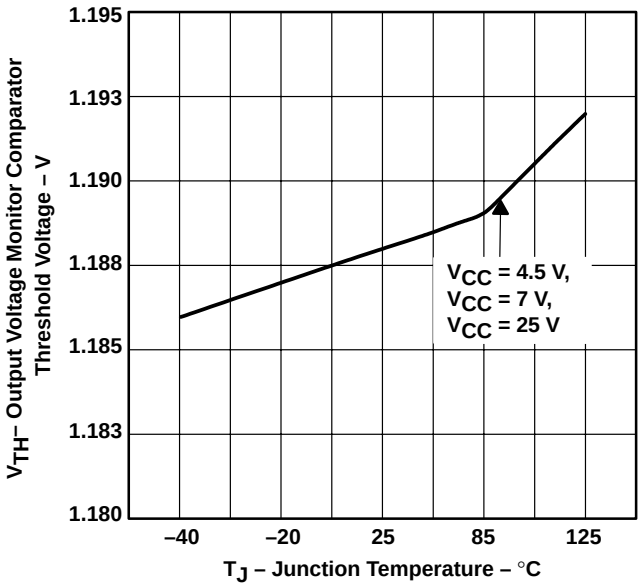


Figure 26

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

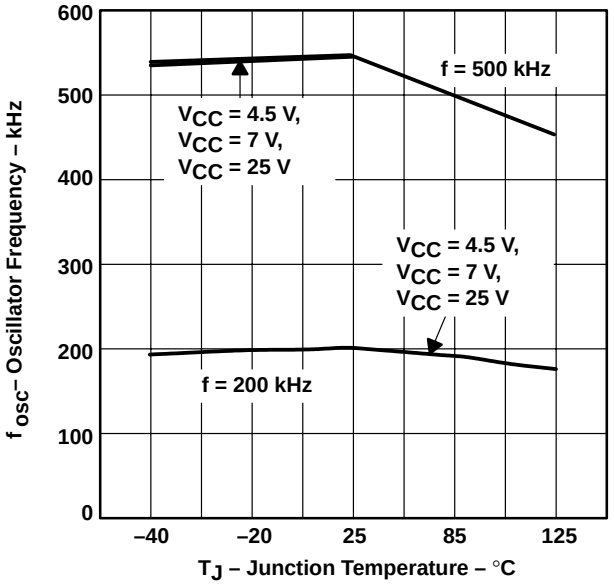


Figure 27

OSCILLATOR OUTPUT VOLTAGE vs FREQUENCY

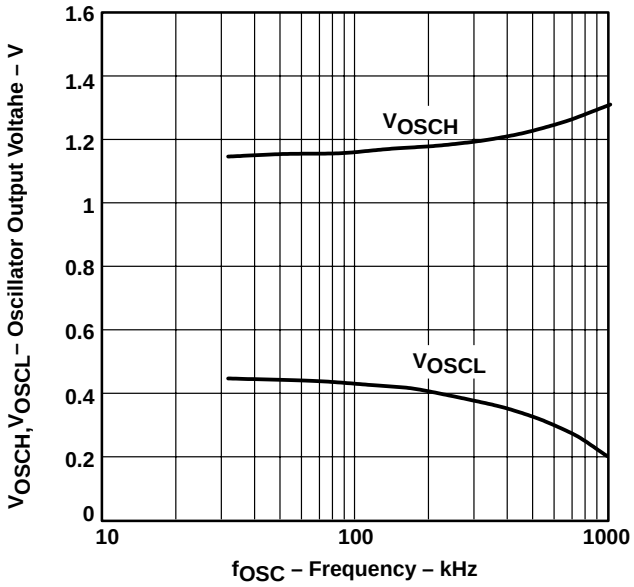


Figure 28

ERROR AMPLIFIER GAIN AND PHASE SHIFT

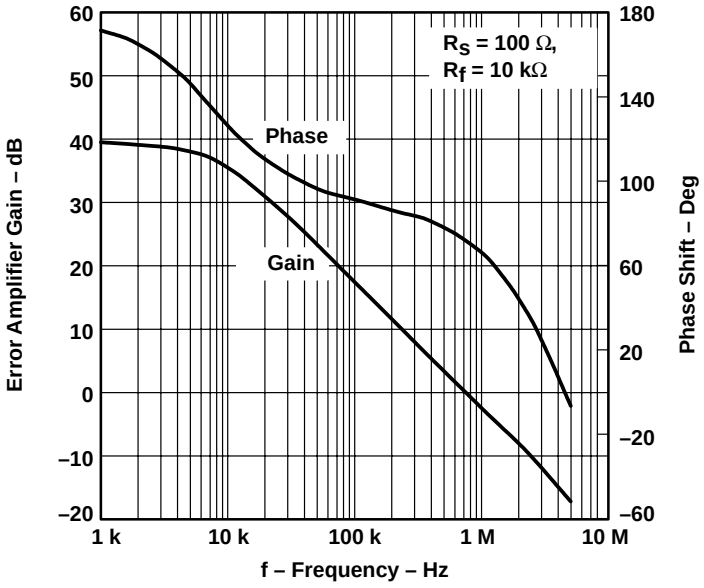


Figure 29

TYPICAL CHARACTERISTICS

MAXIMUM DUTY CYCLE vs JUNCTION TEMPERATURE

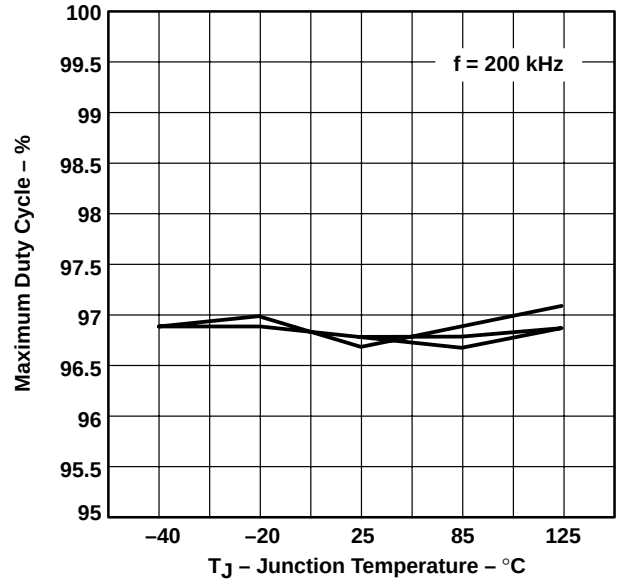


Figure 30

SOFTSTART CAPACITANCE vs SOFTSTART TIME

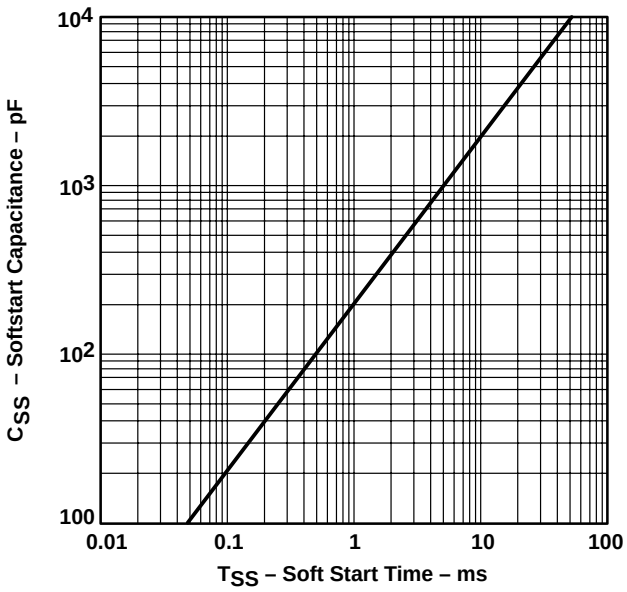


Figure 31

DRIVER DEAD TIME vs JUNCTION TEMPERATURE

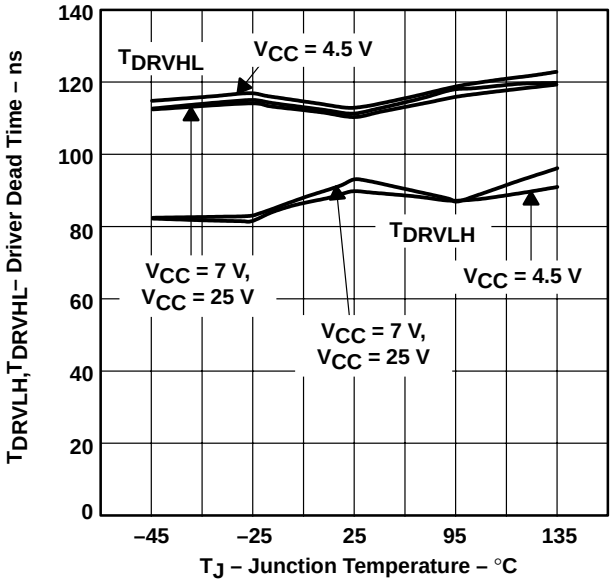


Figure 32

CURRENT PROTECTION SOURCE CURRENT vs INPUT VOLTAGE PWM MODE

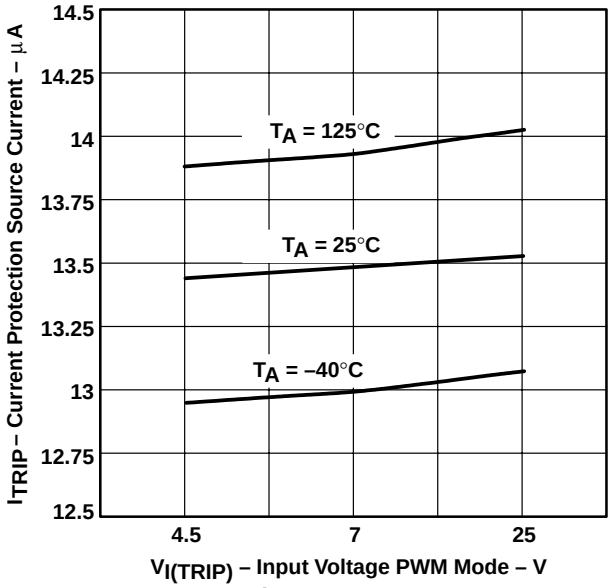


Figure 33

TYPICAL CHARACTERISTICS

**CURRENT PROTECTION SOURCE CURRENT
vs
INPUT VOLTAGE SKIP MODE**

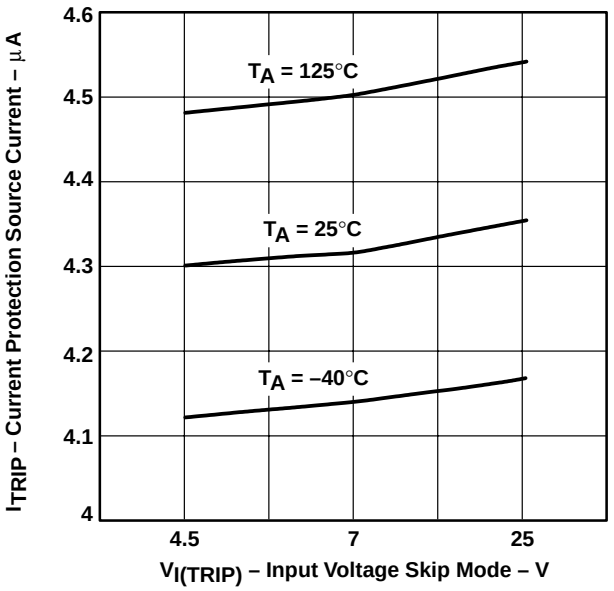


Figure 34

**OSCILLATOR FREQUENCY
vs
RESISTOR**

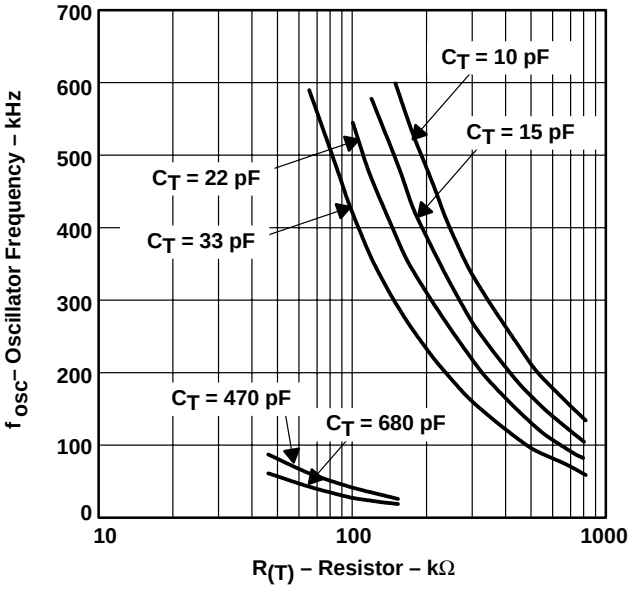


Figure 35

APPLICATION INFORMATION

overshoot of output rectangle wave

The drivers in the TPS5103 controller are fast and can produce high transients on V_{CC} or the junction of Q1 and Q2 (shown below). Care must be taken to insure that these transients do not exceed the absolute maximum rating for the device or associated external component. A low-ESR capacitor connected directly from Q1 drain to Q2 source can greatly reduce transient pulses on V_{CC}. Also, Q1 turnon speed can be reduced by adding a resistor (5 – 15 Ω) in series with OUT_u. Poor layout of the switching node (V1 in Figure 36) can result in the requirement for additional snubber circuitry required from V1 to ground.

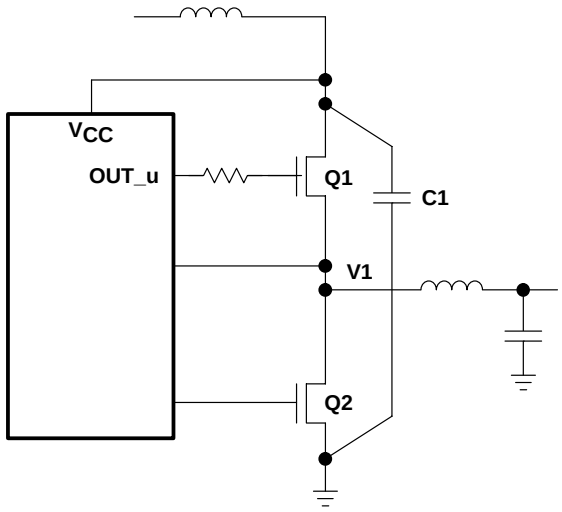


Figure 36. Output Rectangle Wave

The high-current Schottky diode (D1) can be removed provided an alternate way of preventing negative voltages on LL (≥0.5 V) is used (refer to Figure 38).

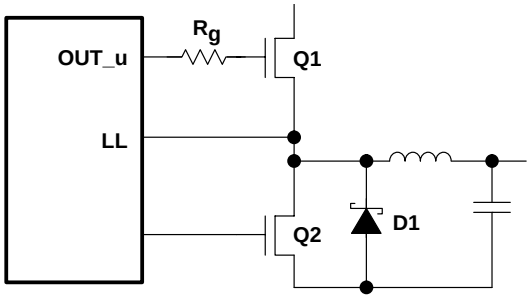


Figure 37. High-Current Schottky Diode

APPLICATION INFORMATION

Resistor (R_g) is moved from the gate of the top FET and placed in series with LL. This allows for a smaller Schottky diode (DX) to be used.

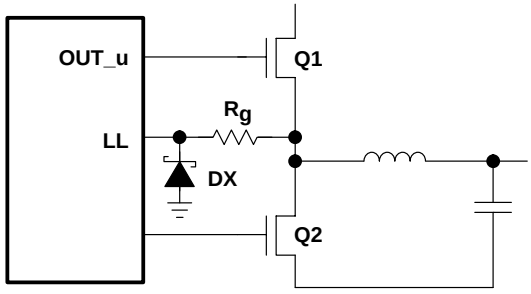
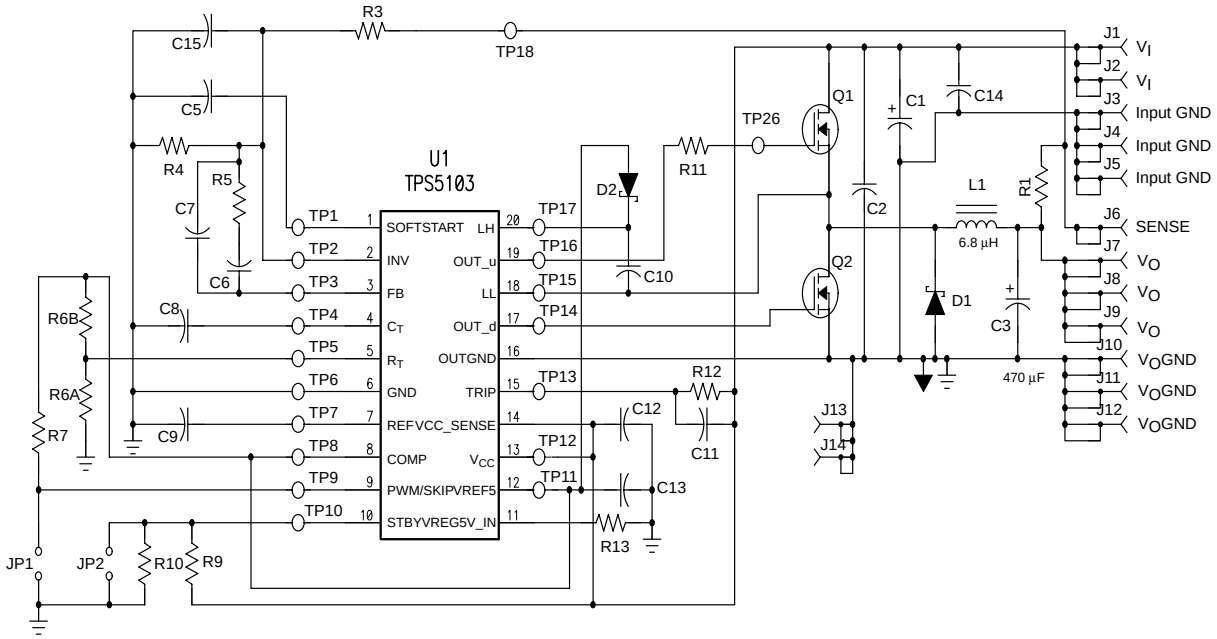


Figure 38. High-Current Schottky Diode Removed

application for general power

The design shown in this data sheet is a reference design for a general power supply application. An evaluation module (EVM), TPS5103EVM-136 (SLVP136), is available for customer testing and evaluation. The intent is to allow a customer to fully evaluate the given design using the plug-in EVM supply shown here. For subsequent customer board revisions, the EVM design can be copied onto the users PCB to shorten design cycle time, component count, and board cost.

To help the customers design the power supply using the TPS5103, some key design procedures are shown in Figure 39.



NOTE: V_I = 4. V to 10 V
V_O = 1.8 V @ 4 A

Figure 39. EVM Schematic

APPLICATION INFORMATION

output voltage setpoint calculation

The output voltage is set by the reference voltage and the voltage divider. In the TPS5102, the reference voltage is 1.185 V, and the divider is composed of two resistors in the EVM design that are R4 and R5, or R14 and R15. The equation for the setpoint is shown below.

$$R2 = \frac{R1 \times V_{ref}}{V_O - V_{ref}}$$

Where R1 (> 10 kΩ) is the top resistor R2 is the bottom resistor (kΩ), V_O is the required output voltage, and V_{ref} is the reference voltage (1.185 V in TPS5103).

Example: R1 = 1 kΩ; V_{ref} = 1.185 V; V_O = 1.8 V, then R2 = 1.9 kΩ.

Some of the most popular output voltage setpoints are calculated in Table 2.

Table 2. Output Voltage Setpoints

V_O	1.3 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
R1 (kΩ)	10	10	10	10	10	10
R2 (kΩ)	100	37	19	9	5.6	3.1

If higher precision resistor is used, the output voltage setpoint can be more accurate.

In some applications, the output voltage is required to be lower than the reference voltage. With a few extra components, this lower voltage can be easily achieved. Figure 40 shows the method for accomplishing this.

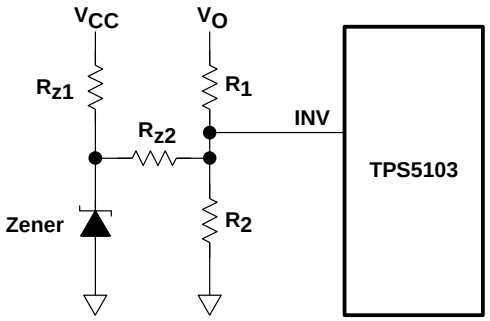


Figure 40. Application With Extra Components for Lower Output Voltage

In the schematic, R_{z1}, R_{z2}, and the Zener are the extra components. R_{z1} is used to give the Zener enough current to build up the Zener voltage. The Zener voltage is added to INV through R_{z2}. Therefore, the voltage on INV is still equal to the IC internal voltage (1.185 V), even if the output voltage is regulated at a lower setpoint. The equation for setting up the output voltage is shown below:

$$R_{z_2} = \frac{\left(V_{(z)} - V_{ref}\right)}{\frac{\left(V_{ref} - V_O\right)}{R1} + \frac{V_{ref}}{R2}}$$

Where R_{z2} is the adjusting resistor for low-output voltage, $V_{(z)}$ is the Zener voltage, V_{ref} is the internal reference voltage, R1 is the top resistor of the voltage sensing network, R2 is the bottom resistor of the sensing network, and V_O is the required output voltage setpoint.

Example: Assuming the required output voltage setpoint is V_O = 0.8 V, $V_{(z)}$ = 5 V, R1 = 1 kΩ; R2 = 1 kΩ, then the R_{z2} = 2.43 kΩ.

APPLICATION INFORMATION

switching frequency

With hysteretic control, the switching frequency is a function of the following:

- input voltage
- output voltage
- hysteresis window
- delay of the hysteresis comparator and the driver
- output inductance
- resistance in the output inductor
- output capacitance
- ESR and ESL in the output capacitor
- output current
- turnon resistance of the high-side and the low-side MOSFET

This is a very complex equation if everything is included. To make it more useful to the designers, a simplified equation only considers the most influential factors. The tolerance of this equation is about 30%.

$$fs = \frac{V_O \times (V_I - V_O) \times (ESR - (10 \times 10^{-7} + Td)/C_O)}{V_I \times (V_I \times ESR \times (10 \times 10^{-7} + Td) + 0.0097 \times L_{(O)} - ESL \times V_I)}$$

Where fs is the switching frequency (Hz), V_O is the output voltage, V_I is the input voltage, C_O is the output capacitance, ESR is the equivalent series resistance in the output capacitor (Ω), ESL is the equivalent series inductance in the output capacitor (H), $L_{(O)}$ is the output inductance (H), and Td is the output feedback RC filter time constant (s).

For example: V_I = 5 V, V_O = 1.8 V, C_O = 680 µF; ESR = 40 mΩ; ESL = 3 nH; $L_{(O)}$ = 6 µH; Td = 0.5 µs.

Then, the frequency (fs) = 122 kHz.

output inductor ripple current

The output inductor current ripple can affect not only the efficiency and the inductor saturation, but also the output voltage capacitor selection. The equation is exhibited as below:

$$I_{(ripple)} = \frac{V_I - V_O - I_O\left(r_{ds(on)} + RL\right)}{L_O} \times D \times Ts$$

Where $I_{(ripple)}$ is the peak-to-peak ripple current (A) through inductor; V_I is the input voltage, V_O is the output voltage, I_O is the output current, $r_{ds(on)}$ is the on-time resistance of MOSFET (Ω), D is the duty cycle, and Ts is the switching cycle (S). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example: V_I = 5 V, V_O = 1.8 V, I_O = 5 A, $r_{ds(on)}$ = 10 mΩ, RL = 5 mΩ, D = 0.36, Ts = 10 µs, $L_{(O)}$ = 6 µH

Then, the $I_{(ripple)}$ = 2 A.

output capacitor RMS current

Assuming the inductor ripple current totally goes through the output capacitor to the ground, the RMS current in the output capacitor can be calculated as:

$$I_{O(rms)} = \frac{\Delta I}{\sqrt{12}}$$

APPLICATION INFORMATION

output capacitor RMS current

Where $I_{O(rms)}$ is the maximum RMS current in the output capacitor (A), and ΔI is the peak-to-peak inductor ripple current (A).

Example: ΔI = 2 A, so $I_{O(rms)}$ = 0.58 A

input capacitor RMS current

Assuming the input ripple current totally goes into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

$$I_{I(rms)} = \sqrt{I_o^2 \times D \times (1 - D) + \frac{1}{12} \times D \times Iripple^2}$$

Where $I_{I(rms)}$ is the input RMS current in the input capacitor (A), I_O is the output current (A), and D is the duty cycle. From the equation, it can be seen that the highest input RMS current usually occurs at the lowest input voltage, so it is the worst case design for the input capacitor ripple current.

Example: I_O = 5 A; D = 0.36

Then, $I_{I(rms)}$= 3.36 A

softstart

The softstart timing can be adjusted by selecting the soft-start capacitor value. The equation is shown below.

$$C_{(soft)} = 2 \times T_{(soft)}$$

Where $C_{(soft)}$ is the softstart capacitance (μF), $T_{(soft)}$ is the start-up time on the softstart terminal (s).

Example: $T_{(soft)}$ = 5 ms, so, $C_{(soft)}$ = 0.01 μF.

current protection

The current protection in the TPS5103 is set using an internal current source and an external resistor to set up the current limit. The sensed, high-side MOSFET drain-to-source voltage drop is compared to the set point, if the voltage drop exceeds the limit, the internal oscillator is activated, and continuously resets the current limit until the over-current condition is removed. The equation below should be used for calculating the external resistor value for current protection:

PWM or HYS mode

$$Rcl = \frac{r_{ds(on)} \times \left(I_{(trip)} + Iind(p\text{-}p)/2\right)}{0.000015}$$

SKIP mode

$$Rcl = \frac{r_{ds(on)} \times I_{(trip)} + Iind(p\text{-}p)/2}{0.000005}$$

Where, Rcl is the external current limit resistor (R10, R11), $r_{ds(on)}$ is the high side MOSFET on-time resistance, $I_{(trip)}$ is the required current limit, and Iind(p-p) is the peak-to-peak output inductor current.

Example: PWM mode or HYS mode

$r_{ds(on)}$ = 10 mΩ, $I_{(trip)}$ = 5 A, Iind(p-p) = 2 A, so Rcl = 4 kΩ

Example: SKIP mode

$r_{ds(on)}$ = 10 mΩ, $I_{(trip)}$ = 2 A, Iind(p-p) = 1 A, so Rcl = 5 kΩ

APPLICATION INFORMATION

loop-gain compensation

Voltage mode control is used in this controller for the output voltage regulation. To achieve fast, stabilized control, two parts are discussed in this section: the power stage small signal modeling and the compensation circuit design.

For the buck converter, the small-signal modeling circuit is shown in Figure 41.

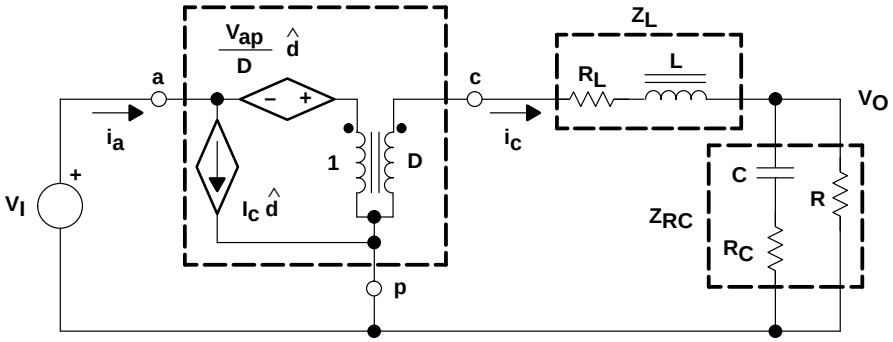


Figure 41. Small-Signal Modeling Circuit

From this equivalent circuit, several control transfer functions can be derived: input-to-output, output impedance, and control-to-output. Typically, the control-to-output transfer function is used for the feedback control design.

Assuming R_C and R_L are much smaller than R, the simplified small signal control-to-output transfer function equation is shown below.

$$\frac{\hat{V}od}{\hat{d}} = \frac{(1 + sCRc)}{1 + s\left[C \times \left(Rc + R_L\right) + \frac{L}{R}\right] + s^2LC}$$

Where C is the output capacitance, Rc is the equivalent serial resistance (ESR) in the output capacitor, L is the output inductor, RL is the equivalent serial resistance (ESR) in the output inductor, and R is the load resistance.

To achieve the fast transient response and the better output voltage regulation, a compensation circuit is added to improve the feedback control. The whole system is shown in Figure 42.

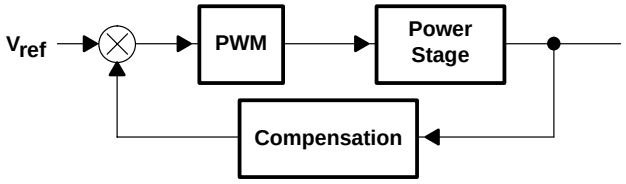


Figure 42. Loop-Gain Compensation

The typical compensation circuit used as an option in the EVM design is a part of the output feedback circuit. The circuitry is shown in Figure 43.

APPLICATION INFORMATION

loop-gain compensation (continued)

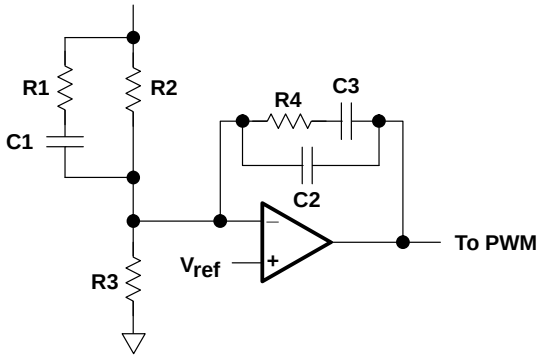


Figure 43. Typical Compensation Circuit

This circuit is composed of one integrator, two poles, and two zeros.

Assuming R1 << R2 and C2 << C3, the equation is:

$$\text{Comp} = \frac{(1 + sC3R4) \times (1 + sC2R2)}{sC3R2(1 + sC2R4)(1 + sC1R1)}$$

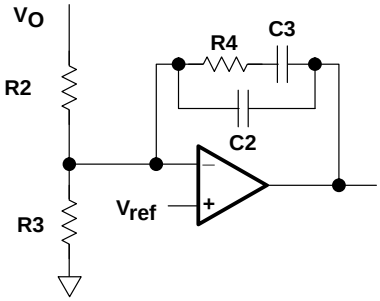
Therefore,

$$\text{Pole } 1 = \frac{1}{2\pi C1R1} \qquad \text{Pole } 2 = \frac{1}{2\pi C2R4}$$

$$\text{Zero } 2 = \frac{1}{2\pi C3R4} \qquad \text{Zero } 1 = \frac{1}{2\pi C2R2}$$

$$\text{Integrator} = \frac{1}{2\pi f C3R2}$$

A simplified version used in the EVM design is shown in Figure 44.



NOTE: R2 > 10 kΩ

Figure 44. Simplified Compensation Circuit

Assuming C2 << C3, the equation is:

$$\text{Comp} = \frac{(1 + sC3R4)}{sC3R2(1 + sC2R4)}$$

APPLICATION INFORMATION

loop-gain compensation (continued)

There is one pole, one zero, and one integrator.

$$\text{Zero} = \frac{1}{2\pi C3R4} \qquad \text{Pole} = \frac{1}{2\pi C2R4} \qquad \text{Integrator} = \frac{1}{2\pi f C3R2}$$

The loop-gain concept is used to design a stable and fast feedback control. The loop-gain equation is derived by the control-to-output transfer function times the compensation. The equation is shown below.

$$\text{Loop} - \text{gain} = \text{Vod X Comp}$$

By using a bode plot, the amplitude and the phase of this equation can be drawn with software such as MathCad. In turn, the stability can be easily designed by adjusting the compensation perimeters. The sample bode plot shown in Figure 45 explains the phase margin, gain margin, and the crossover frequency.

The gain is drawn as 20 log (loop-gain), and the phase is in degrees. To explain them clearer, 180 degrees is added to the phase, so that the gain and phase share the same zero.

Where the gain curve touches the zero is the crossover frequency. The higher this frequency is, the faster the transient response is, since the transient recovery time is 1/(crossover frequency). The phase to the zero is the phase margin at the crossover frequency. The phase margin should be at least 60 degrees to cover all the condition changes, such as temperature. The gain margin is the gap between the gain curve and the zero when the phase curve touches the zero. This margin should be at least 20 dB to assure the stability over all conditions.

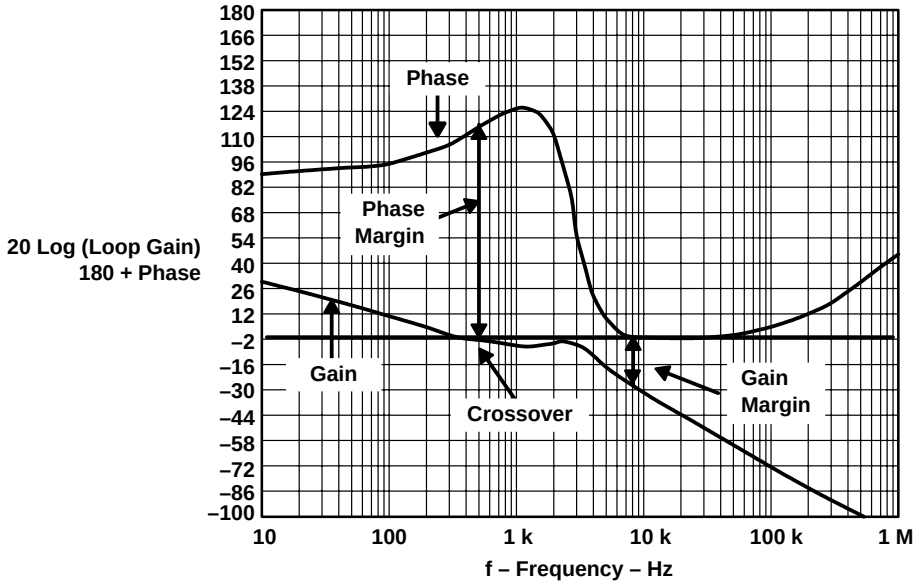


Figure 45. Sample Bode Plot (not the EVM)

synchronization

Some applications require switching-clock synchronization. The following two methods are used for synchronization.

- Triangle-wave synchronization

APPLICATION INFORMATION

synchronization (continued)

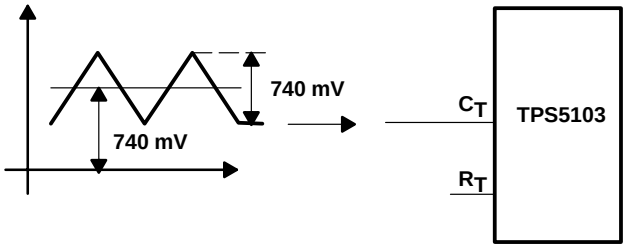


Figure 46. Triangle-Wave Synchronization

- Square-wave synchronization

It can be seen that R_T and C_T are removed from the circuit. Therefore, two components are saved. This method is good for the synchronization between two controllers. If the controller needs to be synchronized with a digital circuit such as a DSP, usually the square-type clock signal is used. The configuration shown in Figure 47 is for this type of application.

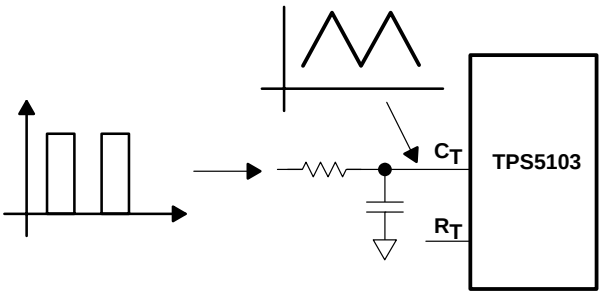


Figure 47. Square-Wave Synchronization

An external resistor is added into the circuit, but R_T is still removed. C_T is kept to be a part of the RC circuit generating the triangle waveform for the controller. Assuming the peak value of the square is known, the resistor and the capacitor can be adjusted to achieve the correct peak-to-peak value and the offset value.

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation, and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power-supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, place the low-level components. Below are several specific points to consider before layout of a TPS5103 design begins.

- All sensitive analog components should be referenced to ANAGND. These include components connected to VREF5, Vref, INV, LH, and COMP .
- Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
- Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
- The bypass capacitor for V_{CC} should be placed close to the TPS5103.

APPLICATION INFORMATION

layout guidelines (continued)

- When configuring the high-side driver as a floating driver, the connection from LL to the power FETs should be as short and as wide as possible.
- When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from LH to LL) should be placed close to the TPS5103.
- When configuring the high-side driver as a ground-referenced driver, LL should be connected to DRVGND.
- The bulk-storage capacitors across V_I should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
- High-frequency bypass capacitors should be placed across the bulk-storage capacitors on V_O.
- LH and LL should be connected very close to the drain and source, respectively, of the high-side FET. LH and LL should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic-decoupling capacitors should be placed close to where V_{CC} connects to V_I, to reduce high-frequency noise coupling on V_{CC}.
- The output-voltage sensing trace should be isolated by either ground trace or V_{CC} trace.

test results

The tests are conducted at T_A = 25°C, the point voltage is 5 V.

APPLICATION INFORMATION

EFFICIENCY vs OUTPUT CURRENT

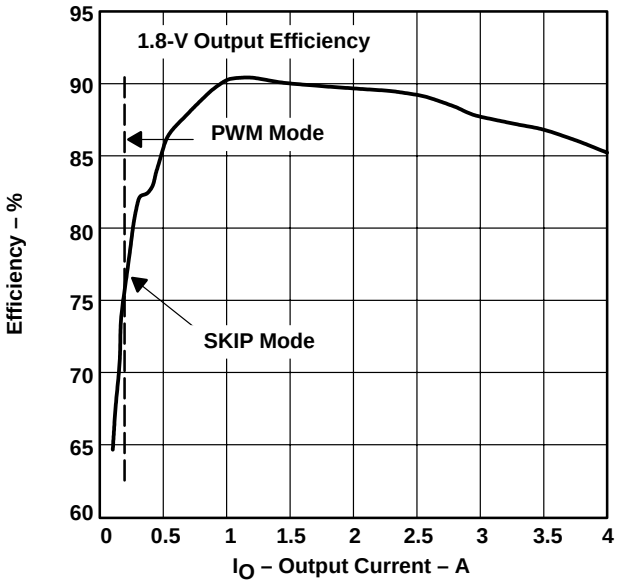


Figure 48

EFFICIENCY vs OUTPUT CURRENT

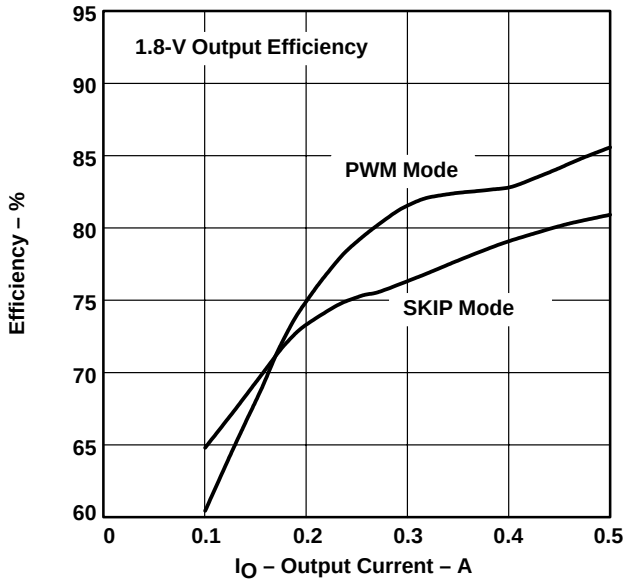


Figure 49

OUTPUT VOLTAGE vs INPUT VOLTAGE

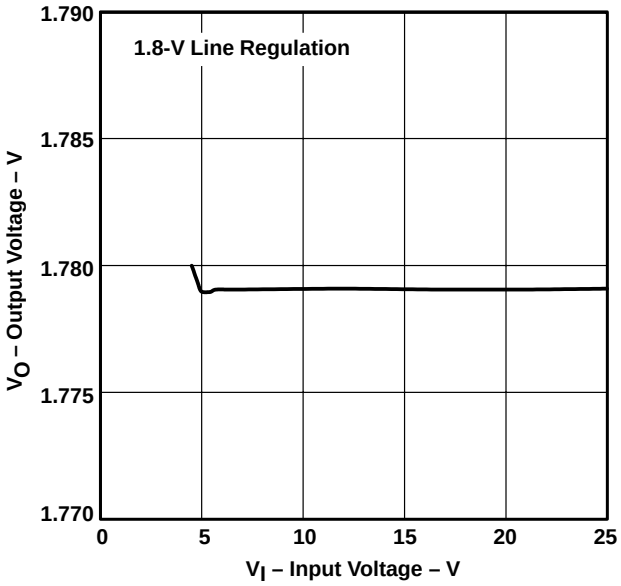


Figure 50

OUTPUT VOLTAGE vs OUTPUT CURRENT

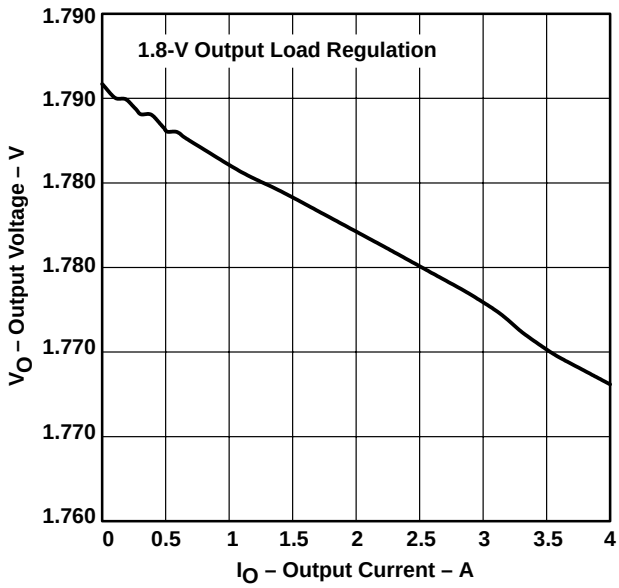


Figure 51

APPLICATION INFORMATION

EFFICIENCY vs OUTPUT CURRENT

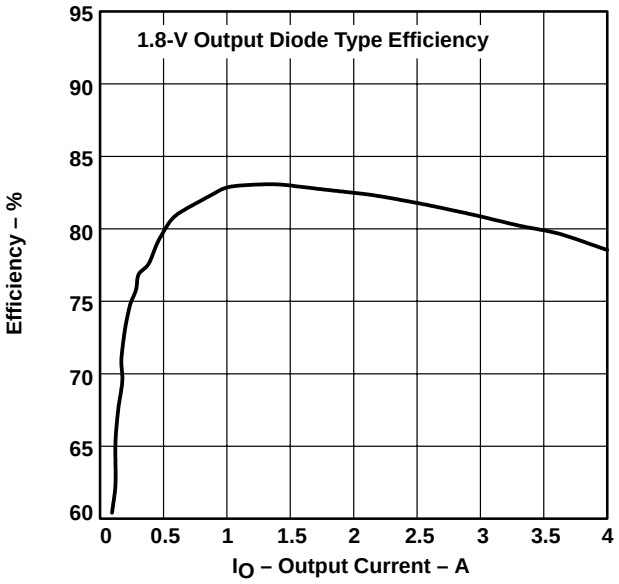


Figure 52

OUTPUT/VOLTAGE

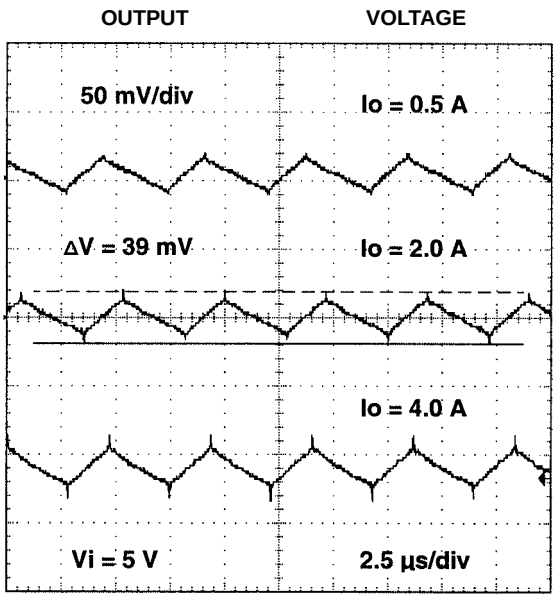


Figure 53

TRANSIENT RESPONSE (OVERSHOOT)

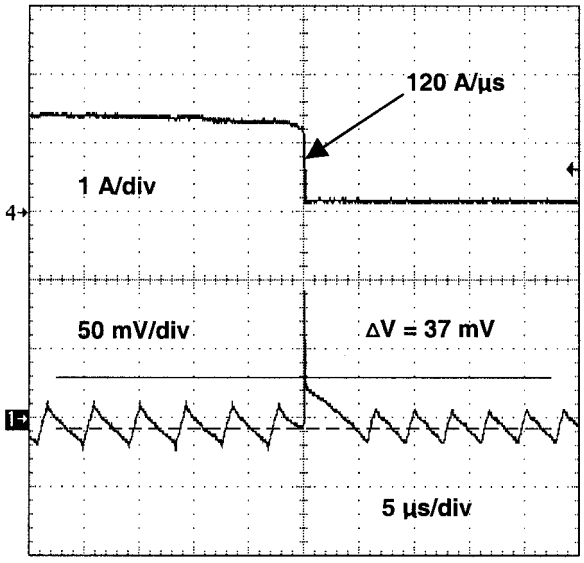


Figure 54

TRANSIENT RESPONSE (UNDERSHOOT)

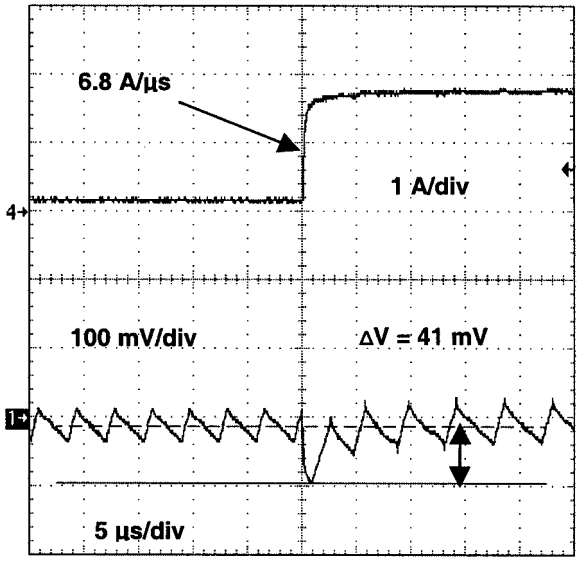


Figure 55

APPLICATION INFORMATION

Table 3. Bill of Materials (see Note 3)

REF	PN	DESCRIPTION	MFG	SIZE
C1opt	10TPB220M	Capacitor, POSCAP, 220 μF, 10 V	Sanyo	7,3 x 4,3 mm
C1	RV-35V221MH10-R	Capacitor, electrolytic, 220 μF, 35 V	ELNA	10 x 10 mm
C2	GMK325F106ZH	Capacitor, ceramic, 10 μF, 35 V	Taiyo Yuden	1210
C3	4TPB470M	Capacitor, POSCAP, 470 μF, 4 V	Sanyo	7,3 x 4,3 mm
C4†	std	Open, capacitor, ceramic, 2.2 μF, 16 V		805
C5	std	Capacitor, ceramic, 1 μF, 16 V		805
C6	std	Capacitor, ceramic, 0.01 μF, 16 V		805
C7	std	Capacitor, ceramic, 220 pF, 16 V		805
C8	std	Capacitor, ceramic, 100 pF, 16 V		805
C9	std	Capacitor, ceramic, 1 μF, 16 V		805
C10	GMK316F225ZG	Capacitor, ceramic, 2.2 μF, 35 V	Taiyo Yuden	1206
C11†	std	Open		805
C12	GMK316F225ZG	Capacitor, ceramic, 2.2 μF, 35 V	Taiyo Yuden	1206
C13	GMK325F106ZH	Capacitor, ceramic, 10 μF, 35 V	Taiyo Yuden	1210
C14		Open		
C14†opt		Open		10 x 10 mm
C15†	std	Open, capacitor, ceramic, 1000 pF, 16 V		805
D1	MBRS340T3	Diode, Schottky, 40 V, 3 A	Motorola	SMC
D1opt	MBRS130LT3	Diode, Schottky, 30 V, 1 A	Motorola	SMB
D2	SD103-AWDICT-ND	Diode, Schottky, 40 V, 200 mA, 400 mW	DigiKey	3,5 x 1,5 mm
L1	DO3316P-682	Inductor, 6.8 uH, 4.4 A	Coilcraft	0.5 x 0.37 in
J1–J14	CA26DA-D36W-0FC	Edge connector, surface-mount, 0.040” board, 0.090” standoff	NAS Interplex	0.040”
JP1	S1132-2-ND	Header, straight, 2-pin, 0.1 ctrs, 0.3” pins	Sullins	Digi-Key #S1132-2-ND
JP1 Shunt	929950-00-ND	Shunt, jumper, 0.1”	3M	Digi-Key #929950-00-ND
JP2	S1132-2-ND	Header, straight, 2-pin, 0.1 ctrs, 0.3” pins	Sullins	Digi-Key #S1132-2-ND
R1	std	Resistor, 5.1 kΩ, 5 %		805
R2†	std	Open, resistor, 1 kΩ, 5%		805
R3	std	Resistor, 910 Ω, 1%		805
R4	std	Resistor, 1.74 kΩ, 1%		805
R5	std	Resistor, 5.1 kΩ, 5%		805
R6A	std	Resistor, 82 kΩ, 5%		805
R6B†	std	Open, 0 Ω, 5%		805
R7	std	Resistor, 1 kΩ, 5%		805
R9	std	Resistor, 1 kΩ, 5%		805
R10	std	Resistor, 1 kΩ, 5%		805
R11	std	Resistor, 10 Ω, 5%		805
R12	std	Resistor, 51 kΩ, 5%		805
R13†	std	Open		805
Q1	Si4410DY	Transistor, MOSFET, n-ch, 30-V, 10-A, 13-mΩ	Siliconix	SO–8
Q2	Si4410DY	Transistor, MOSFET, n-ch, 30-V, 10-A, 13-mΩ	Siliconix	SO–8
U1	TPS5103	IC, controller	TI	SSOP–20

† Components for optional mode test only.

NOTE 3: This operation mode is PWM mode only. V_I = 4.5 V to 10 V, V_O = 1.8 V, and I_O = 4 A (see Table 8 for other applications.)

APPLICATION INFORMATION

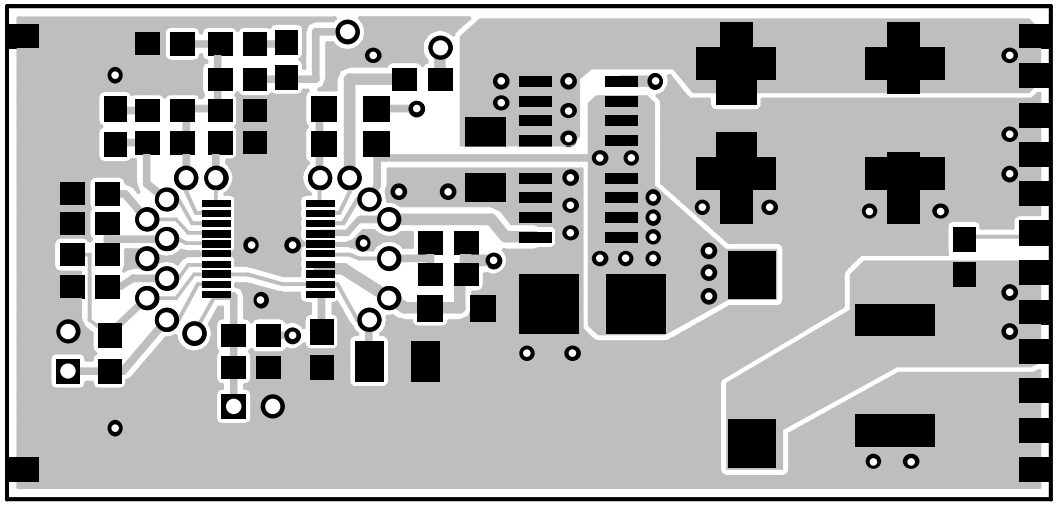


Figure 56. Top Layer

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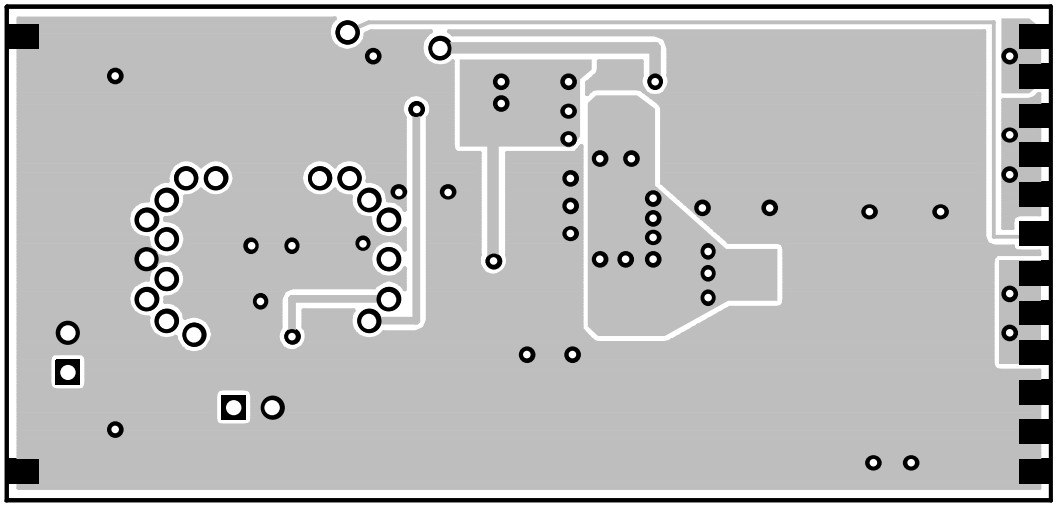


Figure 57. Bottom Layer (Top View)

APPLICATION INFORMATION

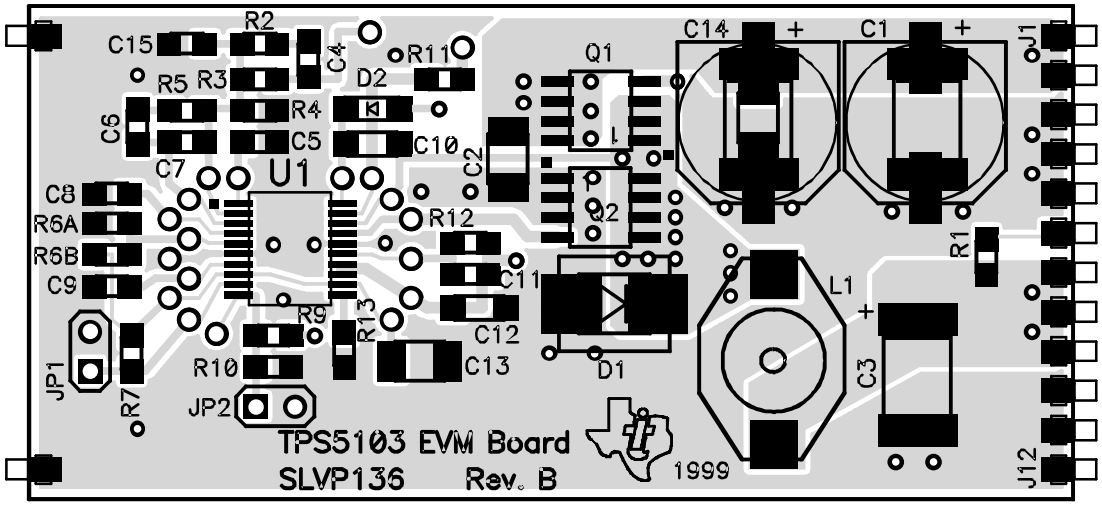
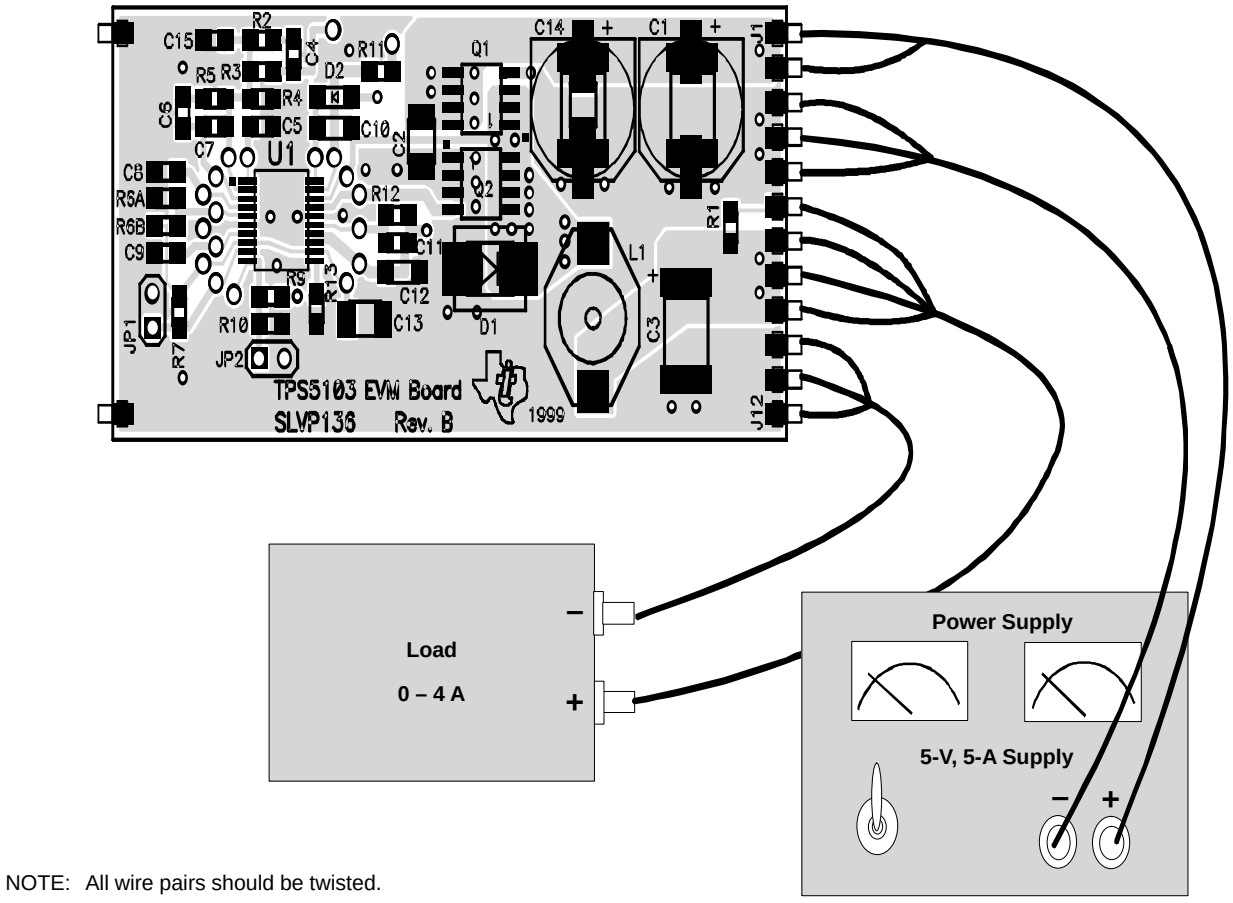


Figure 58. Top Assembly



NOTE: All wire pairs should be twisted.

Figure 59. Test Setup

APPLICATION INFORMATION

Table 4. Test Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range, V_I		5		25	V
Output voltage range, V_O	V_I = 5 – 25 V, I_O = 0 – 4 A	1.7	1.8	1.9	V
Output current range, I_O	V_I = 5 – 10 V	0		4	A
Output current limit	V_I = 5 V	4.3			A
Output ripple	V_I = 5 V, I_O = 4 A			50	mVp–p
Operating frequency, f	I_O = 4 A	150		250	kHz
Efficiency	V_I = 5 V, V_O = 1.8 V, I_O = 4 A		90		%

Table 5. EVM Operating Specifications

SKIP MODE	HYS MODE
Remove JP1 shunt	Remove R5, C6, and C7
	Remove R6A
	Add R6B
	Add C15
	If it needs the loop compensation, add R2 and C4

This EVM is designed to cover as many applications as possible. For more specific applications, the circuit can be simpler. Table 6 gives some recommendations.

Table 6. EVM Application Recommendations

5-V INPUT VOLTAGE	<3-A OUTPUT CURRENT	DIODE VERSION
Change C1 to low-profile capacitor Sanyo 10TPB220M (220 μF, 10 V) or 6TPB330M (330 μF, 6.3 V)	Change Q1 and Q2 to dual-pack MOSFET, IRF7311 to reduce the cost	Remove Q2 to reduce the cost
Remove R10		

Table 7. Vendor and Source Information

MATERIAL	SOURCE	PART NUMBER	DISTRIBUTORS
MOSFETS (Q1–Q2)	In EVM design	Si4410	Local distributor
	Second source	IRF7811 (International Rectifier)	
Input capacitors (C1)	In EVM design	RV–35V221MH10–R (ELNA)	Bell Microproducts 972–783–4191
	Second source	35CV330AX/GX (Sanyo)	870–633–5030
		UUR1V221MNR1GS (Nichicon)	Future Electronics (Local Office)
Main diodes (D1)	In EVM design	MBRS340T3 (Motorola)	Local distributors
	Second source	U3FWJ44N (Toshiba)	Local distributors
Inductors (L1)	In EVM design	DO3316P–682 (Coilcraft)	972–458–2645
	Second source	CTDO3316P–682 (Inductor Warehouse)	800–533–8295
Ceramic capacitors (C2, C14) (C12, C10)	In EVM design	GMK325F106ZH GMK316F225ZG (Taiyo Yuden)	SMEC 512–331–1877
	Taiyo Yuden		email: mike@millsales.com

APPLICATION INFORMATION

High-current applications are described in Table 8. The values are recommendations based on actual test circuits. Many variations are possible based on the requirements of the user. Performance of the circuit is dependent upon the layout rather than on the specific components, if the device parameters are not exceeded. The power stage, having the highest current levels and greatest dv/dt rates, should be given the most attention, as both the supply and load can be severely affected by the power levels and edge rates.

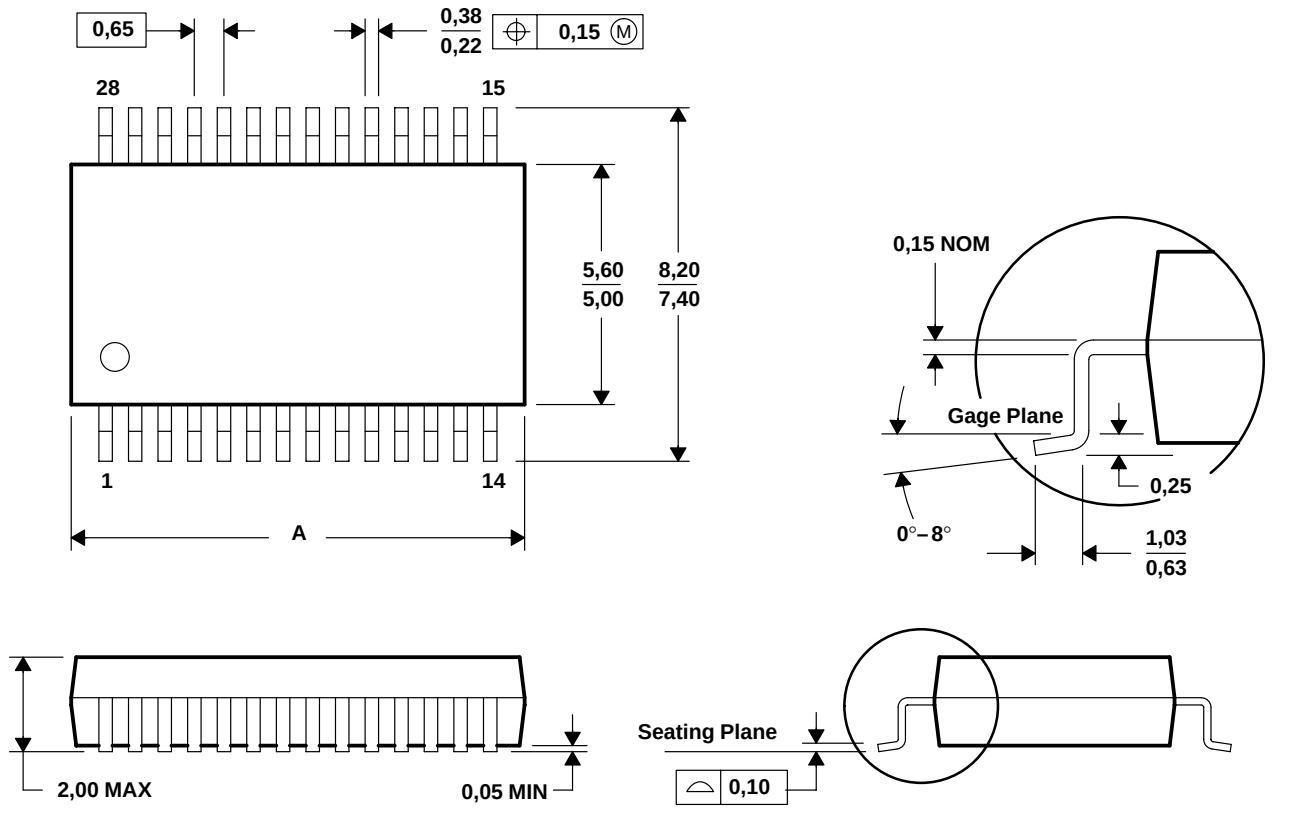
Table 8. High-Current Applications

REFERENCE DESIGNATIONS	Operational Conditions	FUNCTION	8-A OUTPUT	12-A OUTPUT	16-A OUTPUT
C1		Input-bulk capacitor	2x ELNA RV-35V221MH10-R 220 μF, 35 V	3x ELNA RV-35V221MH10-R 220 μF, 35 V	4x ELNA RV-35V221MH10-R 220 μF, 35 V
C2		Input-bypass capacitor	2x Taiyo Yuden GMK325F106ZH 10 μF, 35 V	3x Taiyo Yuden GMK325F106ZH 10 μF, 35 V	4x Taiyo Yuden GMK325F106ZH 10 μF, 35 V
C6	0.01 μΩ at V_I = 4.5 V to 10 V				
L1		Output-filter indicator	Coiltronics UP3B-2R2 2.2 μH, 9.2 A	Coiltronics UP4B-1R5 1.5 μH, 13.4 A	MicorMetals T68-8/90 Core w/7T, #16 1.0 μH, 25 A
C3		Output-filter capacitor	2x Sanyo 4TPB470M 470 μF, 4 V	3x Sanyo 4TPB470M 470 μF, 4 V	4x Sanyo 4TPB470M 470 μF, 4 V
Q1		Power switch	2x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	3x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	4x Siliconix Si4410DY 30 V, 10 A, 13 mΩ
Q2		Power switch	2x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	3x Siliconix Si4410DY 30 V, 10 A, 13 mΩ	4x Siliconix Si4410DY 30 V, 10 A, 13 mΩ
R3	910 kΩ at V_I = 4.5 V to 10 V				
	10 kΩ at V_I = 10 V to 25 V				
R4	1.74 kΩ at V_I = 4.5 V to 10 V				
	19 kΩ at V_I = 10 V to 25 V				
R5	5.1 kΩ at V_I = 4.5 V to 25 V				
R11		Gate-drive resistor	7 Ω	5 Ω	4 Ω
R12		Current-limit resistor	10 kΩ	15 kΩ	20 kΩ
Switching frequency			200 kHz	150 kHz	100 kHz

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS5103IDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS5103IDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS5103IDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS5103IDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

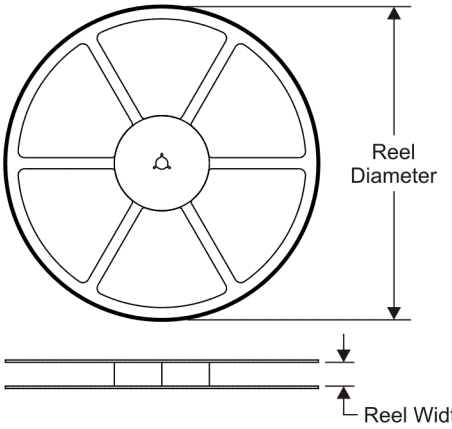
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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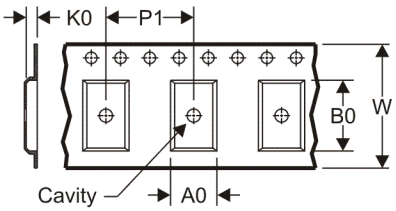
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

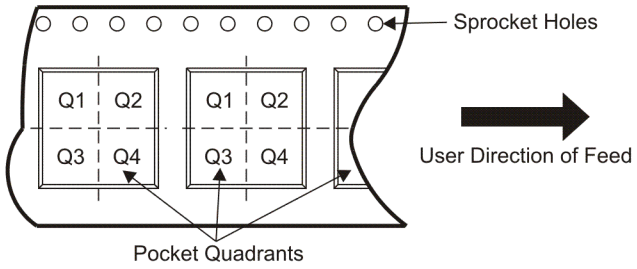


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

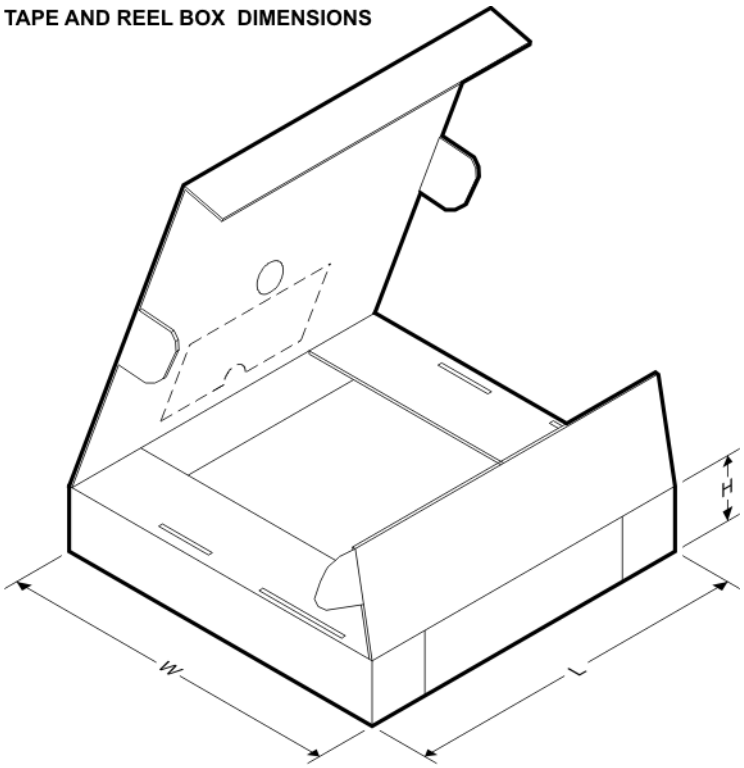
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5103IDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5103IDBR	SSOP	DB	20	2000	346.0	346.0	33.0

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