DATA SHEET

GPC11501C

512KB Sound Controller (OTP)

May 08, 2014

Version 1.7

Table of Contents

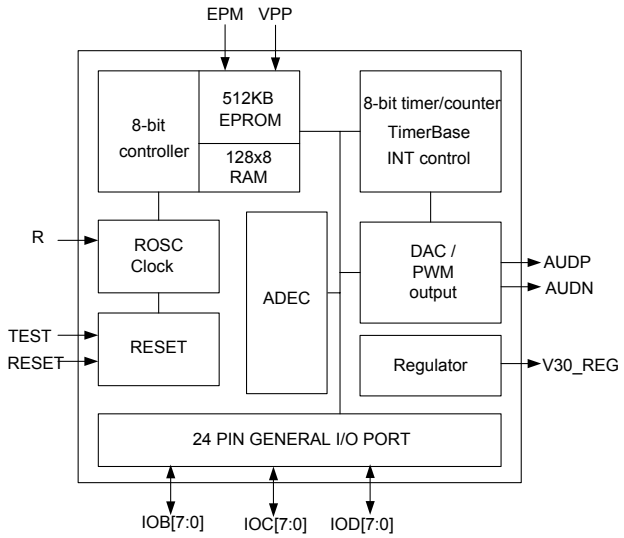
PAGE

512KB SOUND CONTROLLER (OTP)

1. GENERAL DESCRIPTION

The GPC11501C, a speech/wavetable synthesizer, equips an 8-bit CMOS microprocessor, and 512K-byte OTP EPROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 24 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The GPC11501C loads, not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 512K bytes OTP EPROM
- 128-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 6.0MHz
  3.6V - 5.5V @ 8.0MHz
- Supports ROSC only
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings
  Max. 5.0uA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- 24 general I/Os (include 4 high brightness LED driving I/O)
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake -up function
- IR function
- External feedback input
- Watch dog function
- Low voltage reset（LVR）function
- One DAC and A pair of PWM output

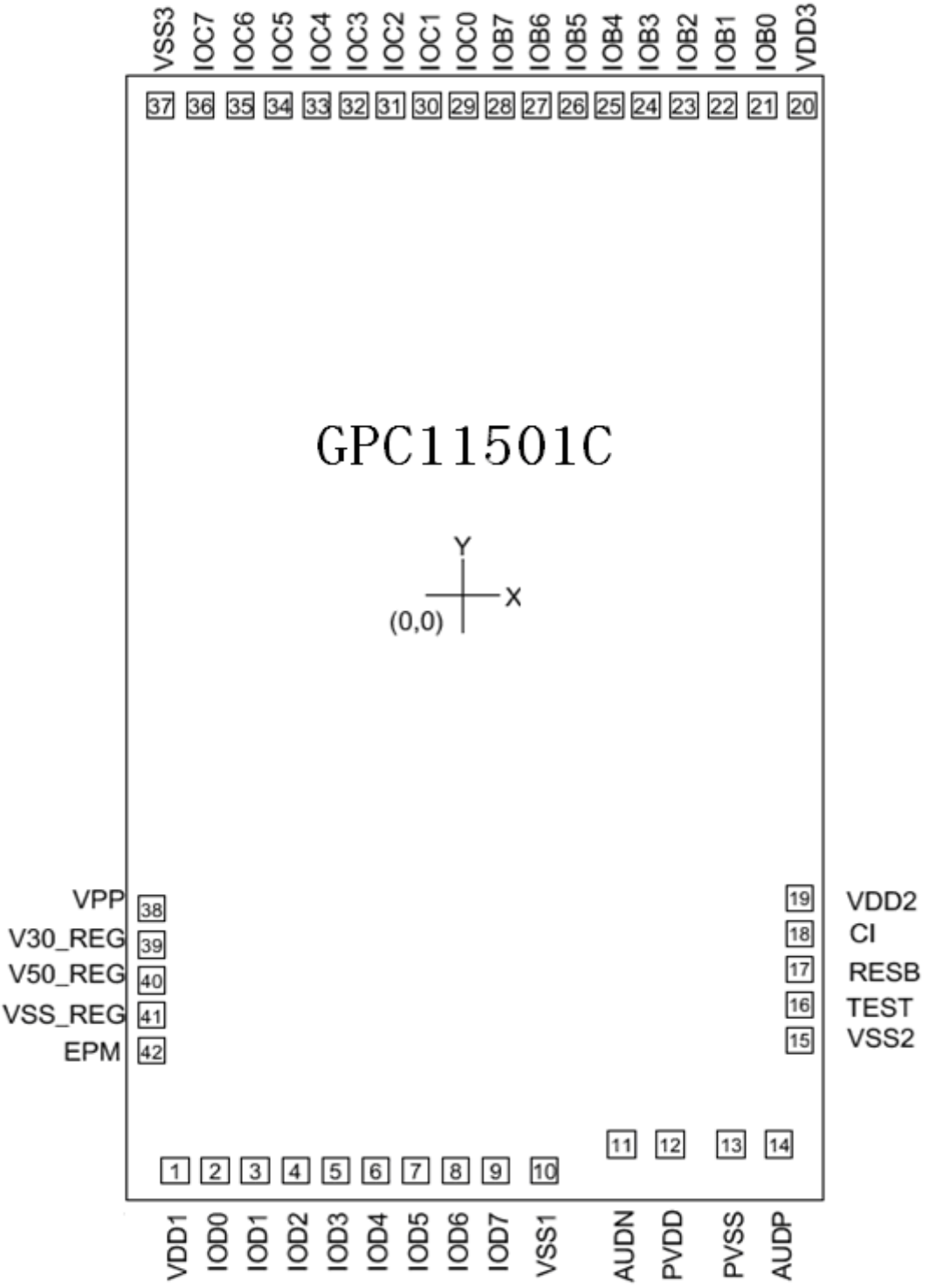
4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No	LQFP 44 Package No	Type	Description
VDD1	1	1	I	Digital Power Pad
VSS1	10	10	I	Digital Ground
VDD2	19	22	I	Digital Power Pad
VSS2	15	18	I	Digital Ground
VDD3	20	23	I	Digital Power Pad
VSS3	37	38	I	Digital Ground
VPP	38	40	I	High voltage input for EPROM programming use, keep it floating in normal run.
V30_REG	39	41	O	3.3v Regulator output Power Pad Need connect it with one 10uF capacitor to Ground.
V50_REG	40	42	I	Regulator Power Pad
VSS_REG	41	43	I	Regulator Ground
EPM	42	44	I	Connect it to VDD during OTP programming cycle, keep it floating in normal run.
PVDD	12	12	I	PWM Power Pad
PVSS	13	13	I	PWM Ground
CI	18	21	I	ROSC Resistor input (Resistor must be connected to VDD)
RESB	17	20	I	Reset pin, active low to reset whole system
TEST	16	19	I	Test pin, NC
AUDP	14	17	O	Audio output
AUDN	11	11	O	Audio output
IOB0	21	-	I/O	Nibble-controlled programmable I/O pins
IOB1	22	-	I/O	In input mode, port B can be either pure or pull-low states. In
IOB2	23	-	I/O	output mode, port B can be buffer.
IOB3	24	-	I/O	
IOB4	25	24	I/O	
IOB5	26	25	I/O	
IOB6	27	26	I/O	
IOB7	28	27	I/O	
IOC0	29	28	I/O	Nibble-controlled programmable I/O pins
IOC1	30	29	I/O	In input mode, port C can be either pure or pull-low states. In
IOC2	31	30	I/O	output mode, port C can be buffer.
IOC3	32	31	I/O	IOC[3:0] can drive high brightness LED
IOC4	33	32	I/O	
IOC5	34	33	I/O	
IOC6	35	34	I/O	
IOC7	36	35	I/O	
IOD0	2	2	I/O	Bit-controlled programmable I/O pins
IOD1	3	3	I/O	In input mode, port D can be either pure or pull-low states
IOD2	4	4	I/O	In output mode, port D can be buffer
IOD3	5	5	I/O	Port D are the key wakeup I/O pins
IOD4	6	6	I/O	IOD4: feedback input of clock generator
IOD5	7	7	I/O	IOD5: feedback output of clock generator
IOD6	8	8	I/O	IOD6: external interrupt
IOD7	9	9	I/O	IOD7: IR transmitter

5.1. PAD Assignment



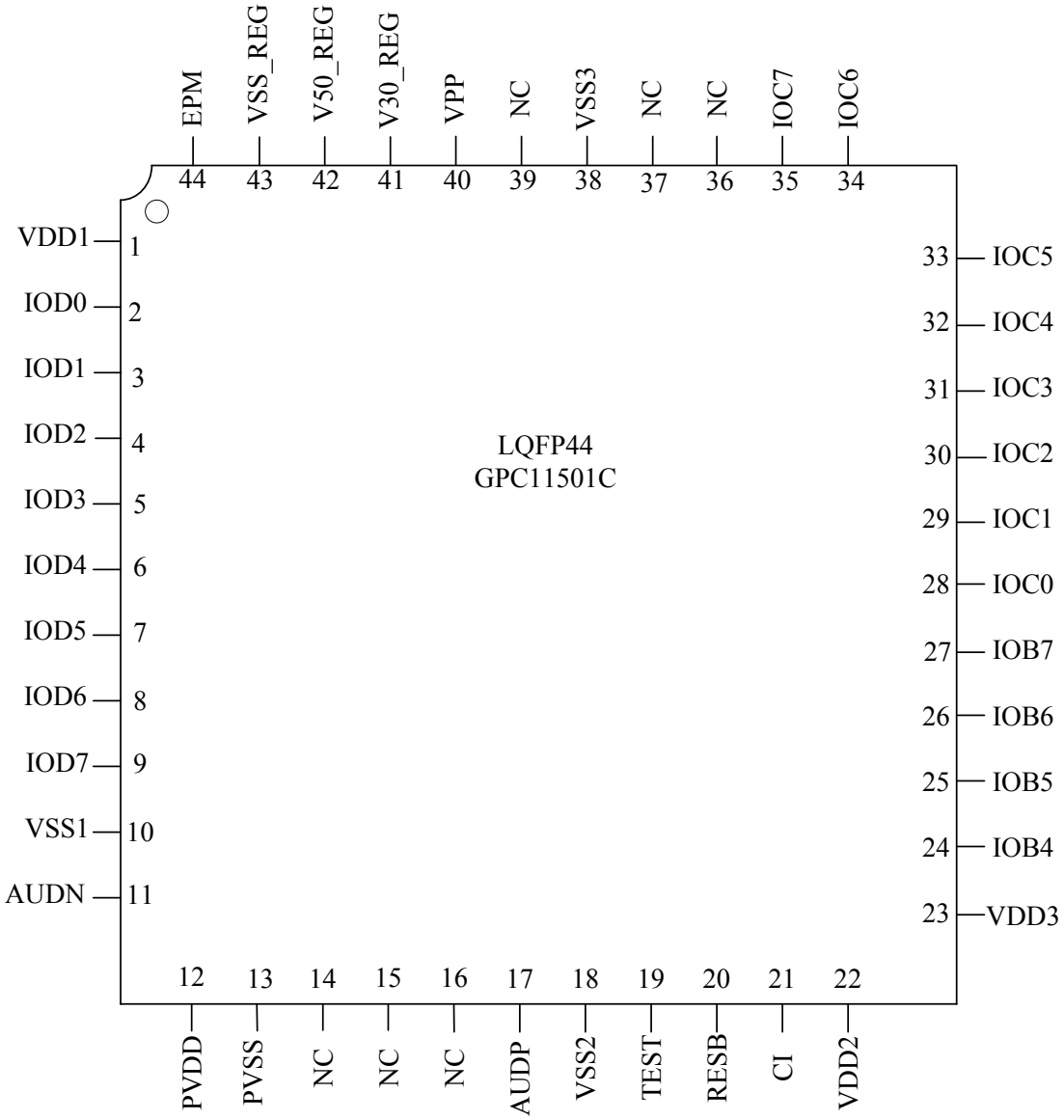
The IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

5.2. PIN Map

LQFP44



6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in GPC11501C is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

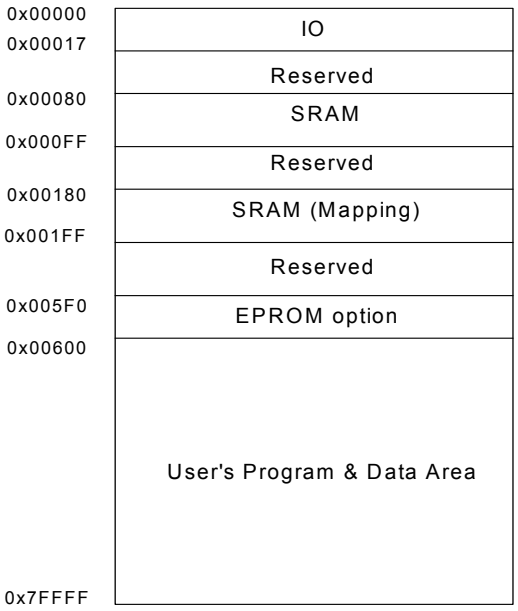
6.2. RAM Area

The total RAM size is 128-bytes (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

6.3. OTP EPROM Area

The GPC11501C provides a 512K-byte OTP EPROM that can be defined as the program area, audio data area, or both.

6.4. Map of Memory and I/Os



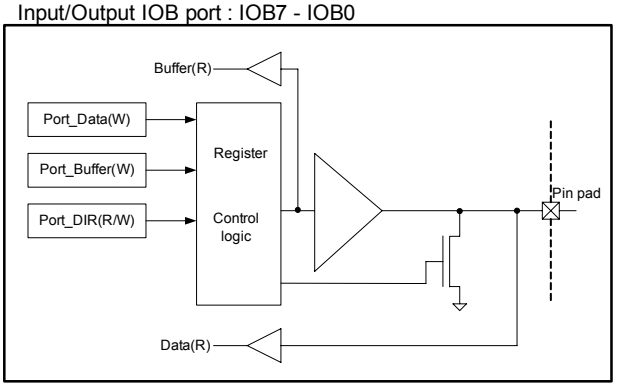
6.5. I/O Port Configuration

There are 24 IOs (IODB7-0, IOC7-0 and IOD7-0) in the GPC11501C. IOB7-0 and IOC7-0 are nibble-controlled IOs, but IOD7-0 are bit-controlled IOs. They can be programmed as input (pure input or pull-low) or output buffer. As pull-low input IOD7-0 keep a less impedance to get good noise immunity. While pressing the key (IOD7-0 to VDD), a large impedance remained to save the DC power. IOD4, IOD5 can be programmed as a RC or crystal clock generator by adding external resistor and capacitor. IOD6 can be programmed as an external interrupt source. IOD7 can be programmed as an IR transmitter.

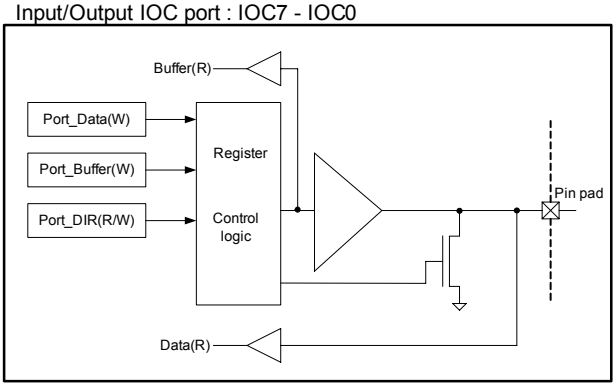
IOC[3:0] can sink high current to drive high brightness LED.

IO port configuration:

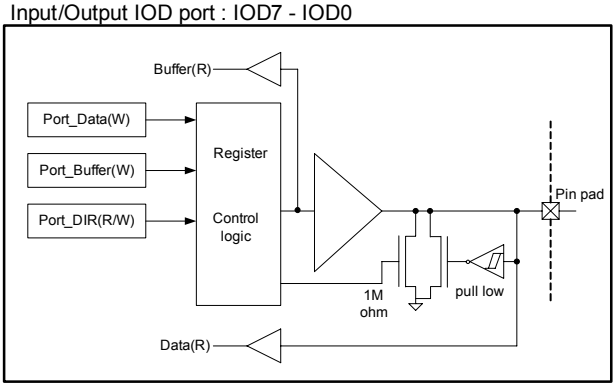
Input/Output IOB port : IOB7 - IOB0



Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



6.6. Power Saving Mode

The GPC11501C includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD7-0 is the only wake-up source in the GPC11501C. After the GPC11501C is awaken, the internal CPU will go to the RESET State (Tw ≧ 64 x T1) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os.

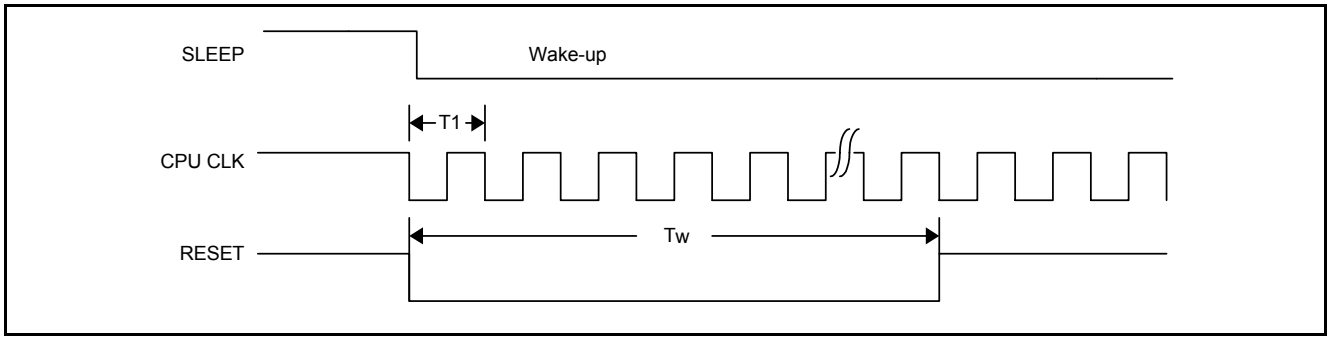


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧64 x T1

6.7. Timer/Counter

The GPC11501C has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.8. Speech and Melody

In speech synthesis, the GPC11501C can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, LOG PCM, ADPCM and SACMA34.

6.9. EPROM Option

5F0[0] : disable/enable security

1: Security disable

0: Security enable

5F0[1]: disable/enable watchdog

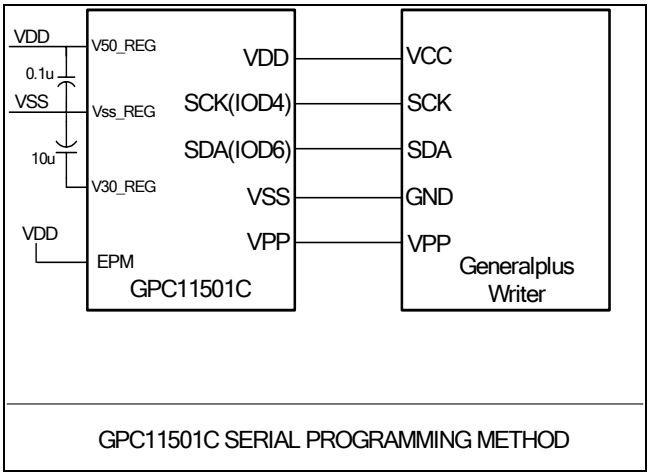
1: disable

0: enable

5F1 ~ 5FF: for Identifying use(EPROM area)

All the above option bits can be read even security bit is enabled.

6.10. OTP Programming Circuit



GPC11501C SERIAL PROGRAMMING METHOD

Note1: Don't connect any component with IOD4 and IOD6 when programming.

Note2: Connect EPM to VDD during OTP programming cycle, and keep it floating in normal run.

Note3: Make sure the power source of Generalplus Writer is 18Volts.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F_{OSC2}	-	4.0	6.0	MHz	VDD = 2.4V - 3.6V, for 2-battery
		-	6.0	8.0	MHz	VDD = 3.6V - 5.5V, for 3-battery

7.3. DC Characteristics (VDD =5.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	-
Operating Current	I_{OP}	-	3.5	-	mA	F_{CPU} = 6.0MHz @ 5.0V(no load)
Standby Current	I_{STBY}	-	-	5	uA	VDD = 5.0V
Audio Output Current	I_{AUD}	-	5.0	-	mA	VDD = 5.0V
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output Source Current (IOB,IOC, IOD)	I_{OH}	-	-10	-	mA	VDD = 5.0V, V_{OH} = 4V
Output Sink Current (IOB,IOC[7:4], IOD)	I_{OL}	-	27	-	mA	VDD = 5.0V, V_{OL} = 1V
Output Sink Current (IOC[3:0])	I_{OL}	-	39	-	mA	VDD = 5.0V, VOL = 1V
PWM Output Current	I_{OH}	-	-188	-	mA	VDD = 5.0V, V_{OH} = 4.0V
	I_{OL}	-	278	-	mA	VDD = 5.0V, V_{OL} = 1.0V
Input Resistor (IOB,IOC)	R_{IN}	-	75	-	Kohm	VDD = 5.0V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	75	-	Kohm	VDD = 5.0V, V_{IN} = 0V
Input Resistor (IOD)	R_{IN}	-	1000	-	Kohm	VDD = 5.0V, V_{IN} = VDD

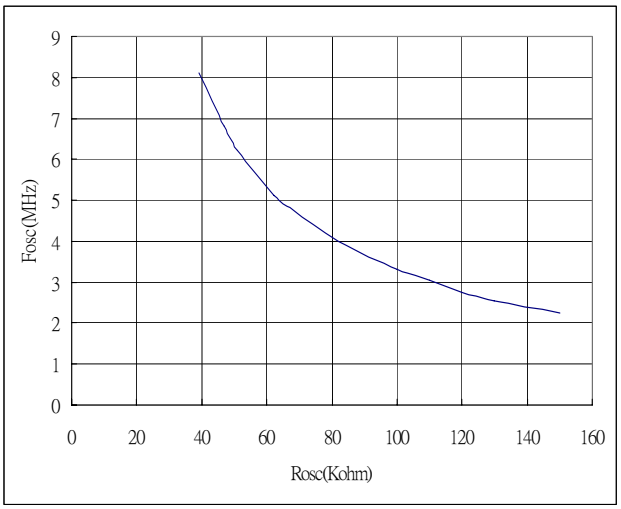
7.4. DC Characteristics (VDD = 3.0V, T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	-
Operating Current	I_{OP}	-	2.8	-	mA	F_{CPU} = 6.0MHz @ 3.0V(no load)
Standby Current	I_{STBY}	-	-	3.0	uA	VDD = 3.0V
Audio Output Current	I_{AUD}	-	2.4	-	mA	VDD = 3.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V

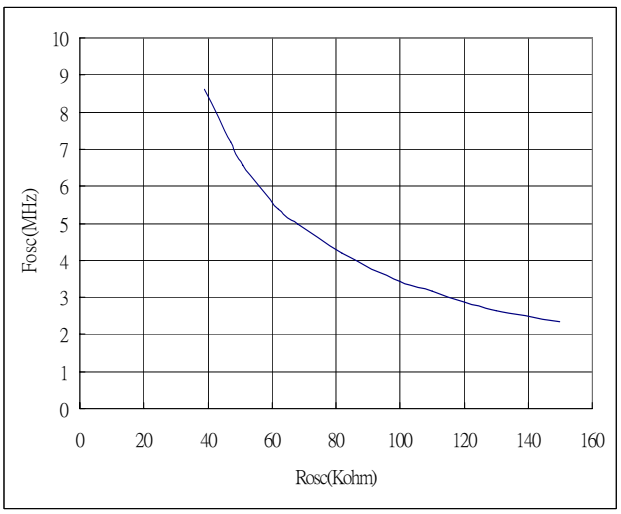
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output Source Current (IOB,IOC, IOD)	I_{OH}	-	-4	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (IOB,IOC[7:4], IOD)	I_{OL}	-	12	-	mA	VDD = 3.0V, V_{OL} = 0.6V
Output Sink Current (IOC[3:0])	I_{OL}	-	17	-	mA	VDD = 3.0V, V_{OL} = 0.6V
PWM Output Current	I_{OH}	-	-72	-	mA	VDD = 3.0V, V_{OH} = 2.4V
	I_{OL}	-	132	-	mA	VDD = 3.0V, V_{OL} = 0.6V
Input Resistor (IOB,IOC)	R_{IN}	-	140	-	Kohm	VDD = 3.0V, V_{IN} = VDD
Input Resistor (IOD)	R_{IN}	-	140	-	Kohm	VDD = 3.0V, V_{IN} = 0V
Input Resistor (IOD)	R_{IN}	-	2200	-	Kohm	VDD = 3.0V, V_{IN} = VDD

7.5. The Relationship between the ROSC and the FCPU

7.5.1. VDD = 3.0V, T_A = 25℃

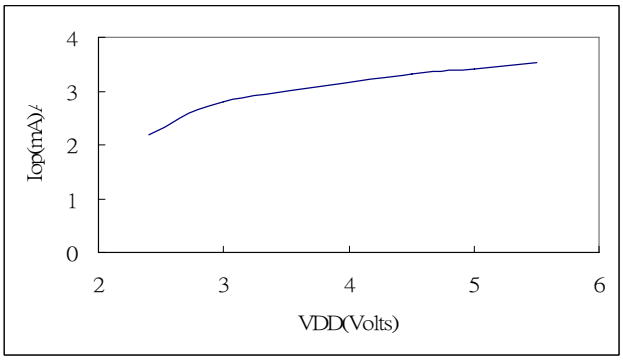


7.5.2. VDD = 5.0V, T_A = 25℃

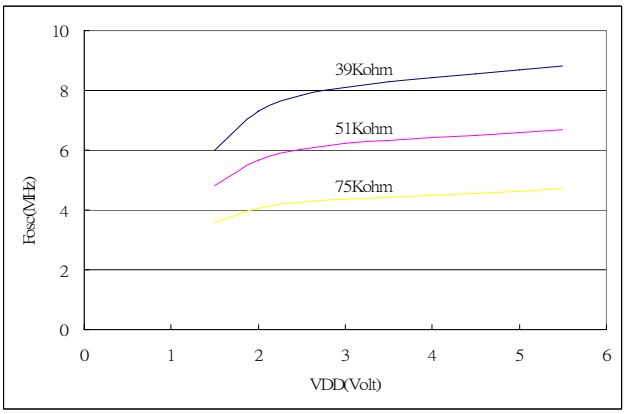


7.5.3. Operating current vs. VDD

PWM with no load, R_{osc}=51Kohm, F_{osc}=6MHz

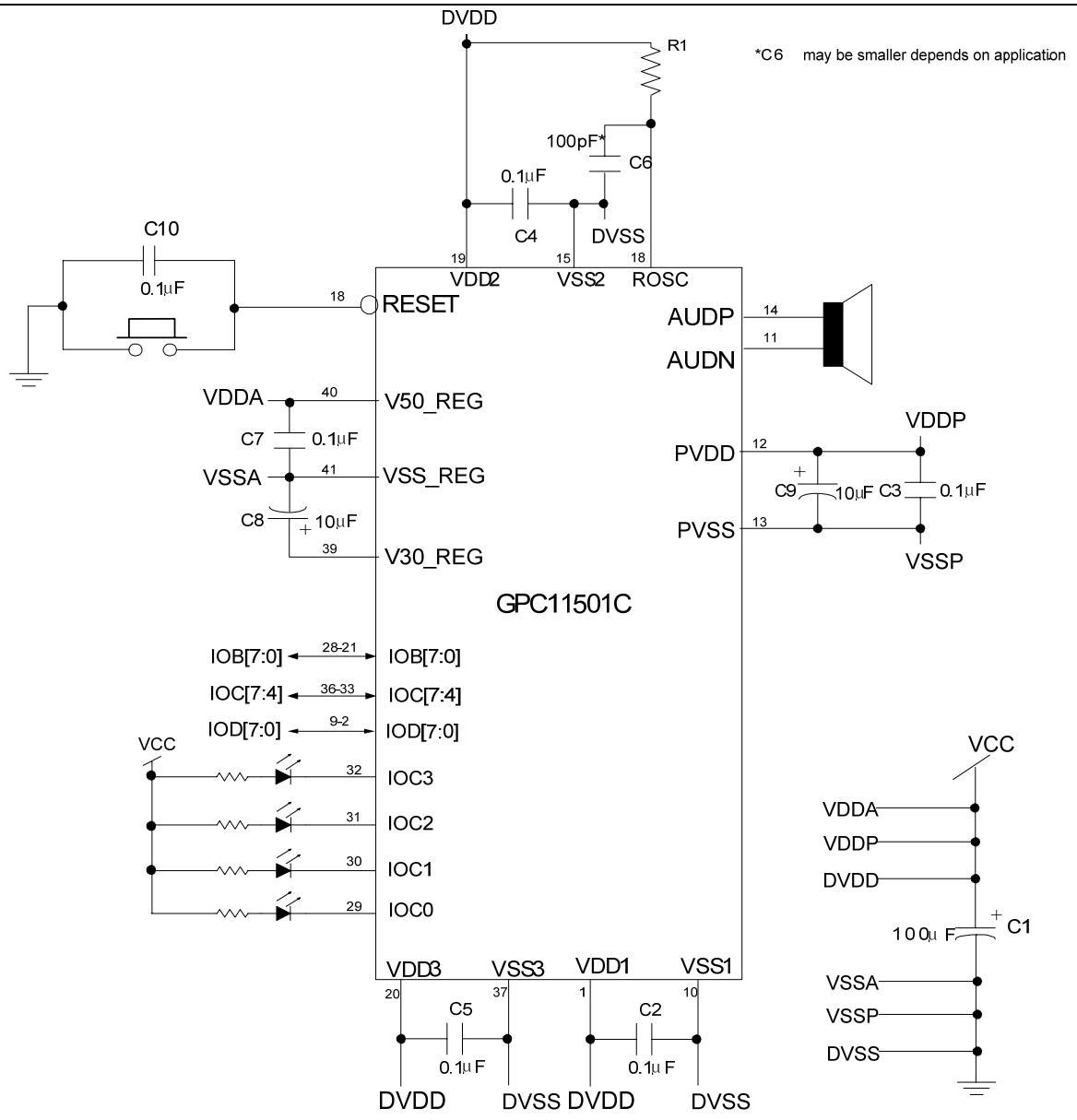


7.5.4. Frequency vs. VDD



8. APPLICATION CIRCUITS

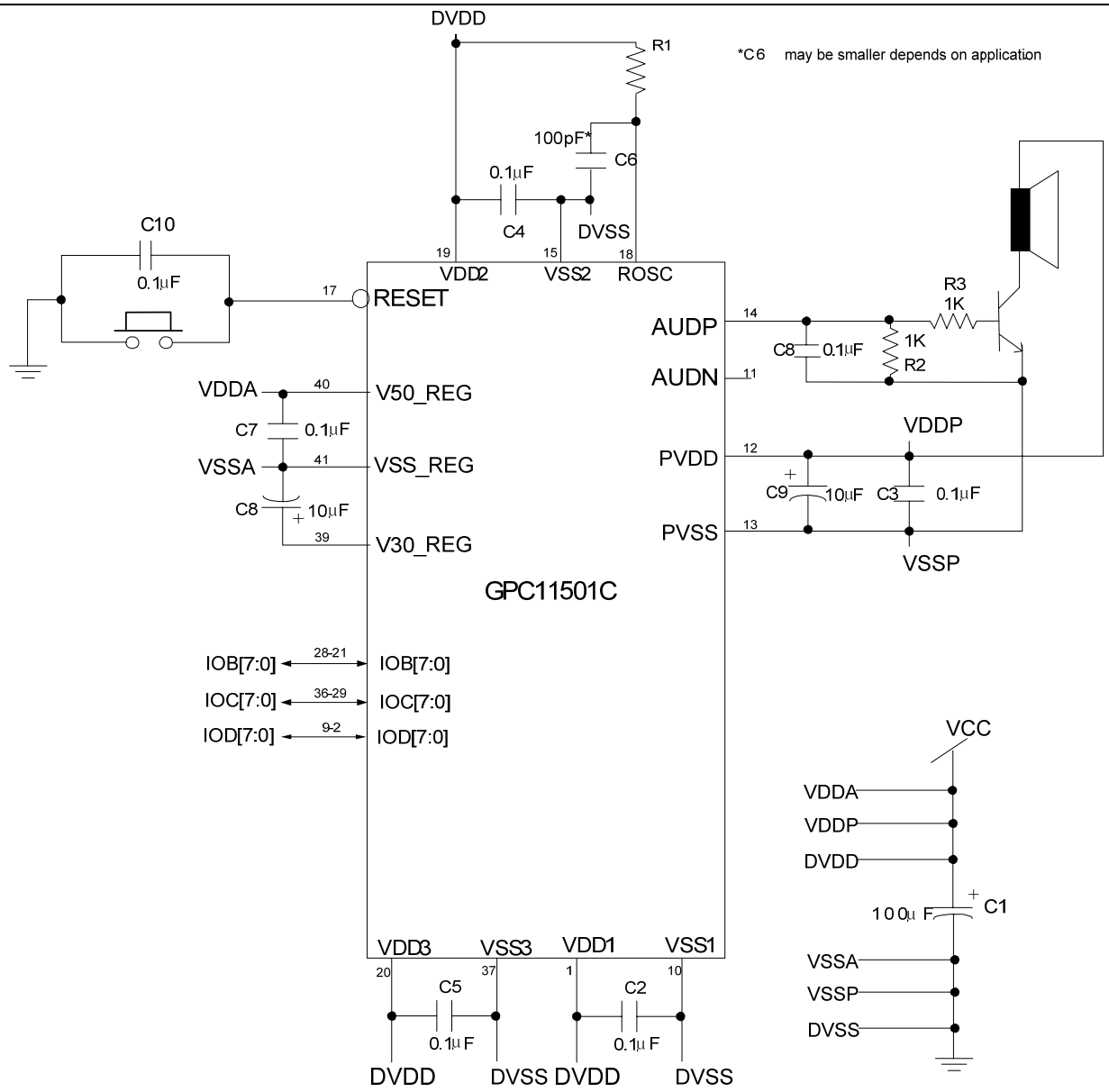
8.1. PWM Output and LED



PCB Layout Guidelines:

1. V50_REG , VDD1 , VDD2 , VDD3 , PVDD must be connected to power input port directly,not to be the branch of each other.
2. VSS_REG , VSS1 , VSS2 , VSS3 , PVSS must be connected to ground input port directly,not to be the branch of each other.
3. R1 and C6 should be as close as possible to ROSC pin.
4. C2 should be as close as possible to VDD1/VSS1 pin.
5. C3 and C9 should be as close as possible to PVDD/PVSS pin.
6. C4 should be as close as possible to VDD2/VSS2 pin.
7. C5 should be as close as possible to VDD3/VSS3 pin.
8. C7 should be as close as possible to V50_REG/VSS_REG pin.
9. C8 should be as close as possible to V30_REG/VSS_REG pin.
10. C10 capacitance 0.1u~10uF is suggested to extend the reset time depending on different application circuits.

8.2. DAC Output



PCB Layout Guidelines:

1. V50_REG , VDD1 , VDD2 , VDD3 , PVDD must be connected to power input port directly,not to be the branch of each other.
2. VSS_REG , VSS1 , VSS2 , VSS3 , PVSS must be connected to ground input port directly,not to be the branch of each other.
3. R1 and C6 should be as close as possible to ROSC pin.
4. C2 should be as close as possible to VDD1/VSS1 pin.
5. C3 and C9 should be as close as possible to PVDD/PVSS pin.
6. C4 should be as close as possible to VDD2/VSS2 pin.
7. C5 should be as close as possible to VDD3/VSS3 pin.
8. C7 should be as close as possible to V50_REG/VSS_REG pin.
9. C8 should be as close as possible to V30_REG/VSS_REG pin.
10. C10 capacitance 0.1u~10uF is suggested to extend the reset time depending on different application circuits.

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPC11501C - NnnV - C	Chip form
GPC11501C - NnnV - QL01x	Halogen Free Package

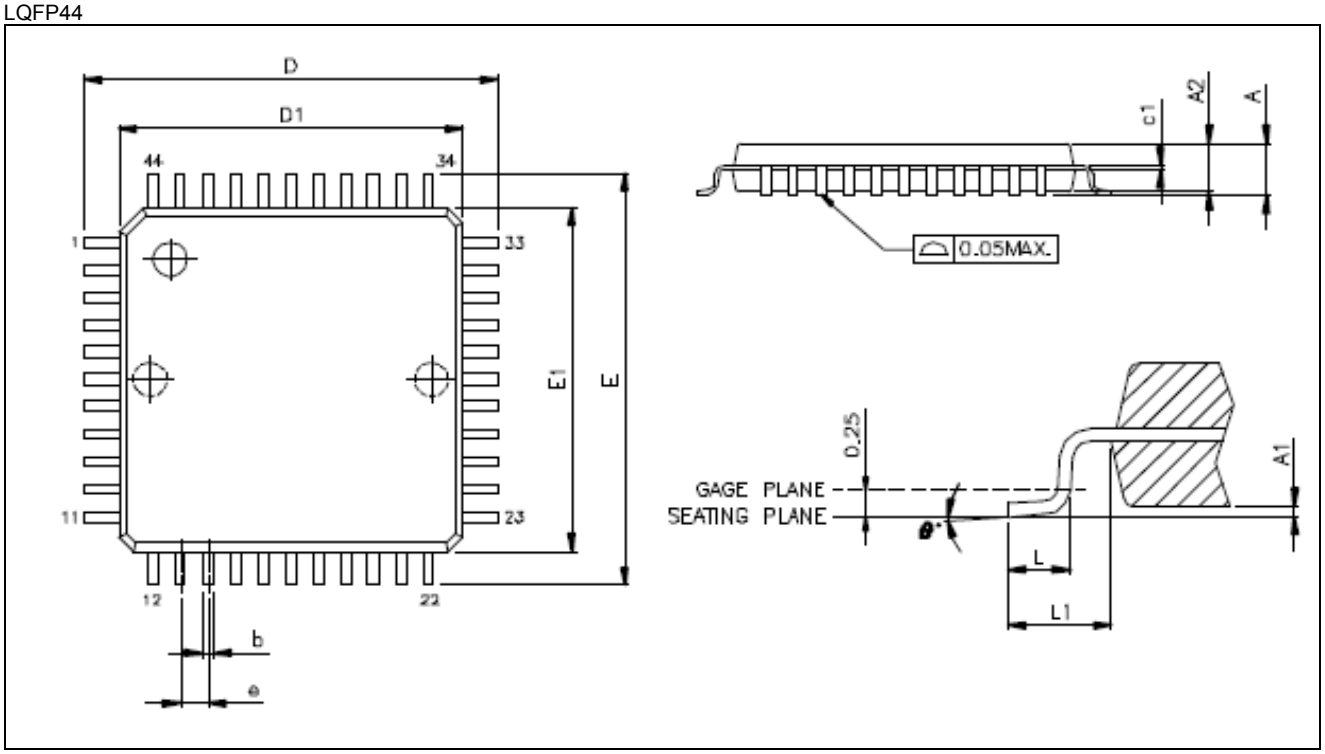
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

LQFP44



Symbols	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1	1.00 REF		
θ°	0°	3.5°	7°

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAY 08, 2014	1.7	Add notice for Application Circuit	11-12
OCT. 15, 2010	1.6	Add 6.10 OTP Programming Circuit	8
APR. 30, 2010	1.5	Remove the related data about QFN48.	4, 6, 14
DEC. 02, 2009	1.4	Add LQFP44 package information.	6, 13
SEP. 22, 2009	1.3	1. Modify 1.DESCRIPTION.	3
		2. Modify 3.FEATURES.	3
		3. Delete 6.7 Low Voltage Reset.	8
		4. Modify 7.2 AC Characteristics.	10
		5. Modify 7.3 DC Characteristics.	10
SEP. 17, 2008	1.2	1. Modify the SIGNAL DESCRIPTIONS in section 5.	4
		2. Add the PIN Map in section 5.2.	6
		3. Modify the Ordering Information in section 9.1.	14
		4. Add the Package Information in section 9.2.	14
APR. 11, 2008	1.1	1. Modify the GENERAL DESCRIPTION in section 1.	3
		2. Modify the FEATURES in section 3.	3
		3. Modify the DC Characteristics (VDD =5.0V, T_A = 25℃) in section 7.3.	9
		4. Modify the DC Characteristics (VDD =3.0V, T_A = 25℃) in section 7.4.	10
		5. Modify the APPLICATION CIRCUITS in section 8.	11-12
OCT. 24, 2007	1.0	Original	15