AN1902
APPLICATION NOTE

VIPower: HF CONVERTER BASED ON VK06TL DEVICES TO DRIVE 58W TL TUBES

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This document describes a reference design for Lighting Ballast dedicated to drive 58W T8 tubes. The board accepts DC input voltage (up to 430V) realizing the cathodes preheating, the EoL protection and the maximum current limitation. It is based on the new VK06 device that integrates the controller and the Power stage on the same chip. It is housed in SO-16 and SIP-9 packages.

INTRODUCTION

The European Community has agreed on a new directive for banning electromagnetic control gear for fluorescent lamps. The aim is to improve the system efficiency (EEI-Energy Efficiency Index) reducing the environmental impact. This new directive divides the ballast in different classes from A1 to D. A1 is the most efficient system, D the least efficient.

- A1 → Dimmable electronic
- A2 → Low-loss electronic
- A3 → Standard electronic
- B1 → Extra low-loss magnetic
- B2 → Low-loss magnetic
- C → Normal-loss magnetic
- D → High-loss magnetic

Since 1998, the energy classification has become compulsory and it has been inserted in a Cenelec standard. It means:

- since April 2002, all ballasts with an EEI of D are banned;
- starting from October 2005, all ballasts with an EEI of C will be banned.

Thus the market is asking for cost effectiveness, good performance, low noise and compact ballasts to feed this kind of applications. The VK06 is a very suitable device, satisfying all the requirements with few external components.

The proposed reference design can supply 58W T8 FL tube with preheating function and EoL protection. Being the design reference focused on the converter realization (we don't cover the PFC stage) it has been set to give out the right output power when 400V dc voltage is applied.

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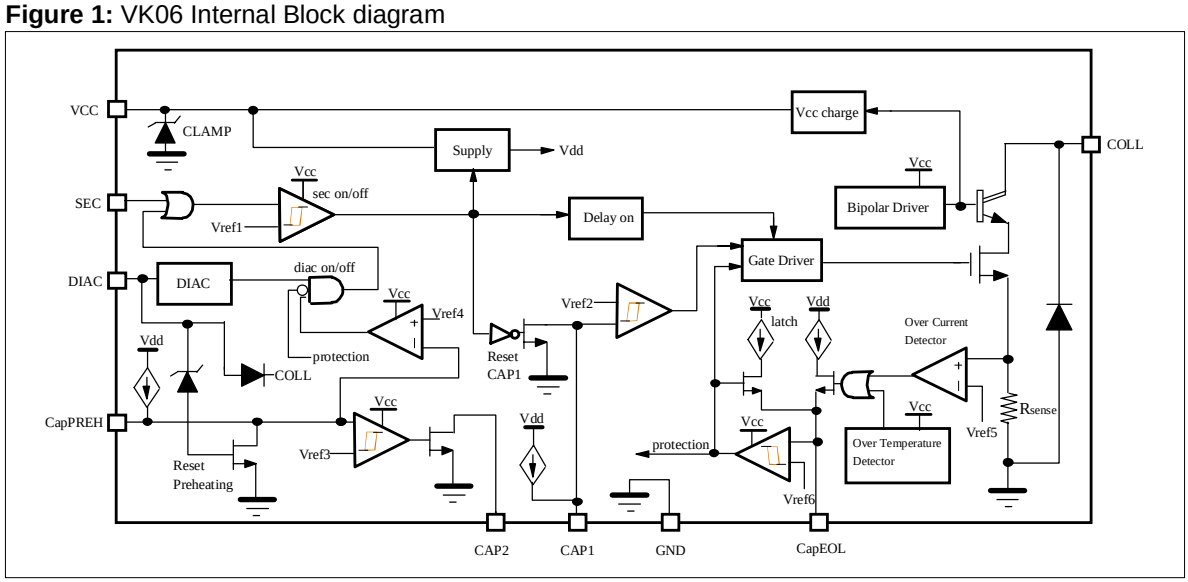
1. VK06 DESCRIPTION

The VK06 is a monolithic device made by using the VIPower® M3-3 STMicroelectronics proprietary technology that integrates in the same chip a vertical flow Power stage and a BCD based control circuit. The Power stage is made by a high voltage Bipolar transistor together with a low voltage n-channel MOS transistor in emitter switching configuration Its performances are a good trade-off between the Bipolar transistor low drop/high breakdown voltages and the MOS transistor high switching speed. The block diagram is shown in figure 1.

In the control part the following sections can be analyzed:

1) Supply
2) Oscillator/Trigger
3) Diac
4) Protections

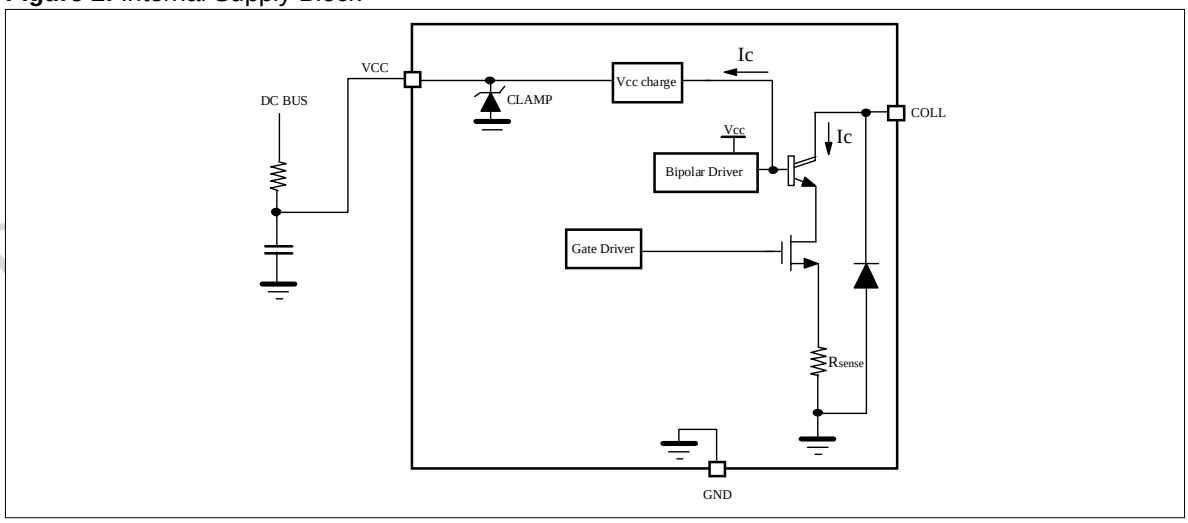
Figure 1: VK06 Internal Block diagram



1.1 SUPPLY (Figure 2)

The device is supplied from the V_{CC} pin connected to an R-C network. From V_{CC} both the control and the power stage are supplied. At start up the supply capacitor is charged through a resistor and only few hundreds µA are needed. During the operation the device is self-supplied recovering on V_{CC} the charge taken from the Power Bipolar base at turn-off. The voltage on V_{CC} is internally clamped at ~6.8V.

Figure 2: Internal Supply Block



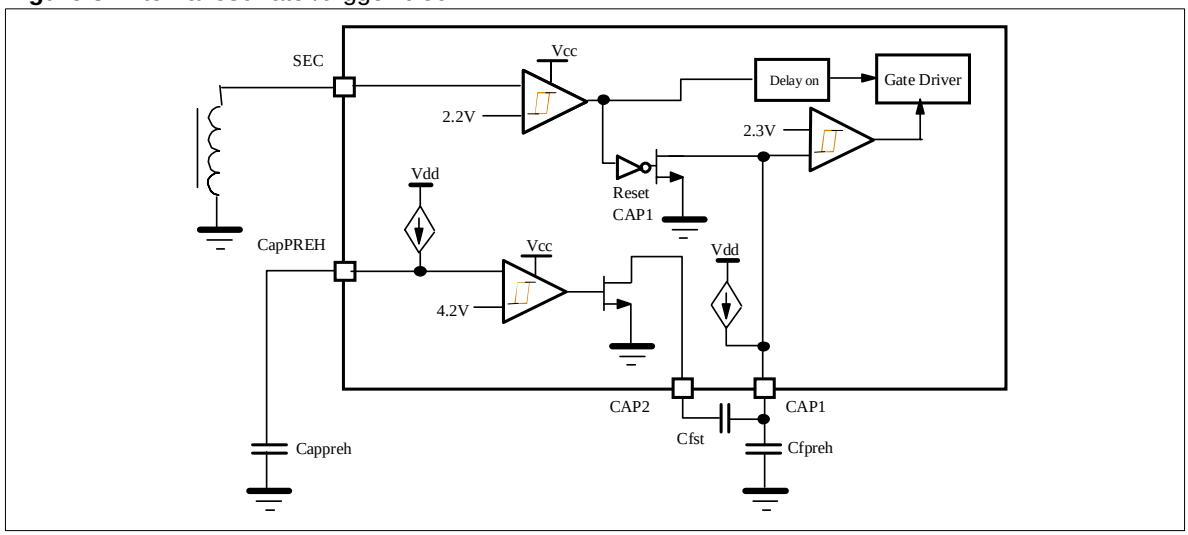
1.2 OSCILLATOR/TRIGGER (Figure 3)

It fixes the converter working frequencies (preheating, ignition, and steady-state). The t_{ON} (conduction time) is set using SEC, CAP1, CAP2 and CapPREH pins. The device is triggered ON when the voltage on SEC reaches ~2.2V. When this condition is detected the Power stage is switched ON and internal current generators start to give constant currents to CAP1 and CapPREH. The device will be switched OFF when one of the two following conditions is present: the voltage across CAP1 is equal to the internal voltage reference (~2.3V), the voltage on SEC is lower than 0.9V. Using a capacitor on CapPREH and the two frequency capacitors on CAP1 and CAP2 it is possible to have both preheating and steady state frequencies. Until the voltage on CapPREH is lower than 4.2V only the Cfpreh (capacitor connected to CAP1) will be charged setting the preheating frequency. When 4.2V on CapPREH pin is overcome, an internal switch puts in parallel Cfpreh with the Cfst capacitors (connected between CAP1 and CAP2) lowering the frequency to the steady-state one. The value of CapPREH fixes the preheating duration. In all the operative conditions the frequency capacitors will be discharged when the voltage on SEC becomes lower than 0.9V.

During the lamp ignition the frequency control is realized through the secondary windings wound on the primary choke and connected to the SEC pins. In this phase the voltage on SEC reaches 0.9V before the t_{ON} is set by the frequency capacitors. The system oscillate at its resonance frequency (higher than steady state one) allowing the tube ignition. After the tube ignition the t_{ON} will be set by the frequency capacitors.

An internal delay at Power turn-on avoids the hard switching condition.

Figure 3: Internal oscillator/trigger block



1.3 DIAC (Figure 4)

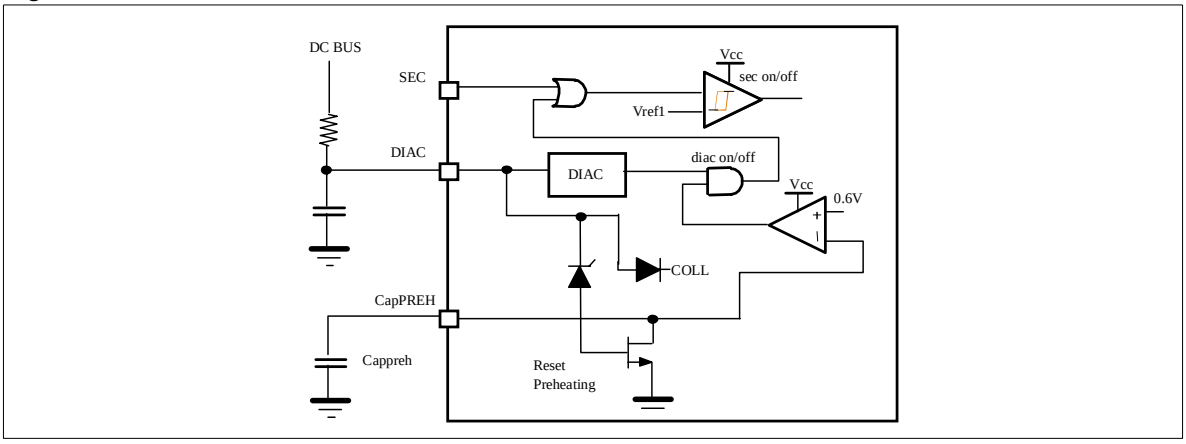
Through the DIAC pin two functions are achieved: start of oscillations and reset of the preheating capacitor CapPREH.

1) Start of oscillation: in OFF condition (voltage on the SEC pin lower than 2.2V) the device can be turned ON when the voltage across DIAC overcomes ~28V. An HV diode keeps the DIAC low when the Power stage is ON.

2) Reset of preheating capacitor: in order to guarantee the right preheating timing the preheating capacitor must be discharged before starting oscillations. To realize this function a switch on CapPREH

pin is activated when the voltage across DIAC pin overcomes ~12V. On the other side the diac can activate the circuit only when the voltage on CapPREH becomes lower than ~0.6V.

Figure 4: Internal diac block

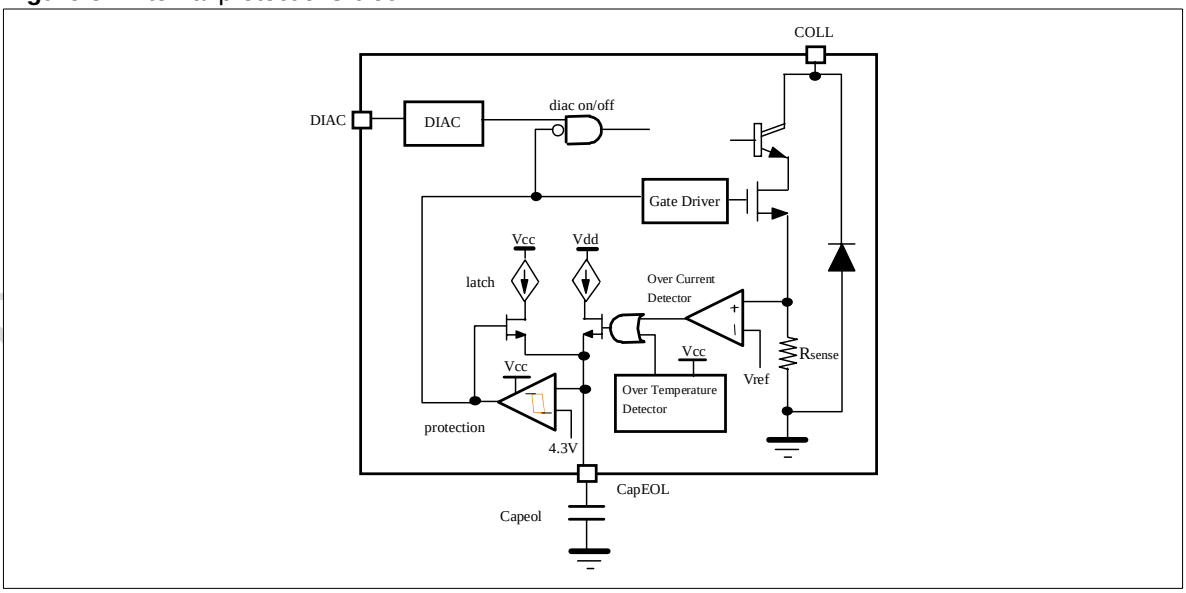


1.4 PROTECTIONS (see figure 5)

The device is protected against over-current and over-temperature. Both protections are activated connecting on the CapEOL pin a capacitor that fixes the timing. The over-current protection works as follows: an internal Rsense checks the current through the Power stage and if it exceeds ~1.5A, an internal generator gives current to CapEOL pin. When the voltage across CapEOL pin reaches ~4.3V the Power stage is kept OFF, the diac is deactivated and the current consumption from V_{CC} is lowered. At the same time another current generator is activated latching the device in OFF state.

The thermal protection is activated when the junction temperature exceeds ~150°C. This block, when activated, acts on the same EoL circuit latching the device.

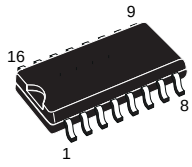
Figure 5:. Internal protections block

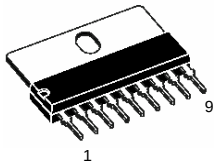


2. PACKAGES

The VK06 is assembled in two different packages in order to cover both the surface mounting and the through-hole PCB. The packages are the SO-16 narrow and the SIP-9 (see figure 6).

Figure 6: Package outline and pin configuration



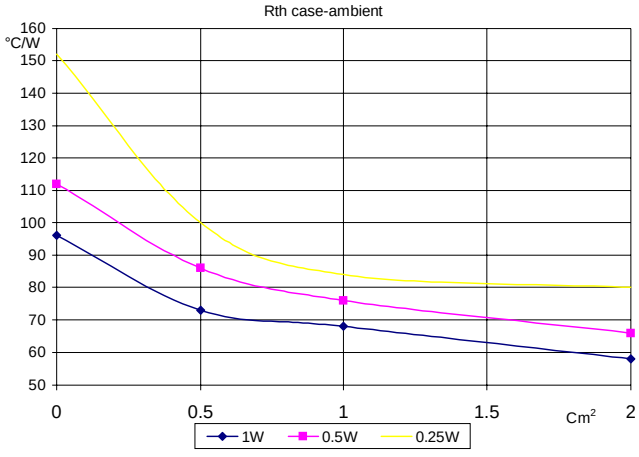


SO16 PACKAGE	
N° pin	Name
1	CAP1
2	CapPREH
3	GND
4	DIAC
5	SEC
6	V_{CC}
7	CAP2
8	CapEOL
9÷16	COLL

SIP9 PACKAGE	
N° pin	Name
1	CAP1
2	CapPREH
3	GND
4	DIAC
5	COLL.
6	SEC
7	V_{CC}
8	CAP2
9	CapEOL

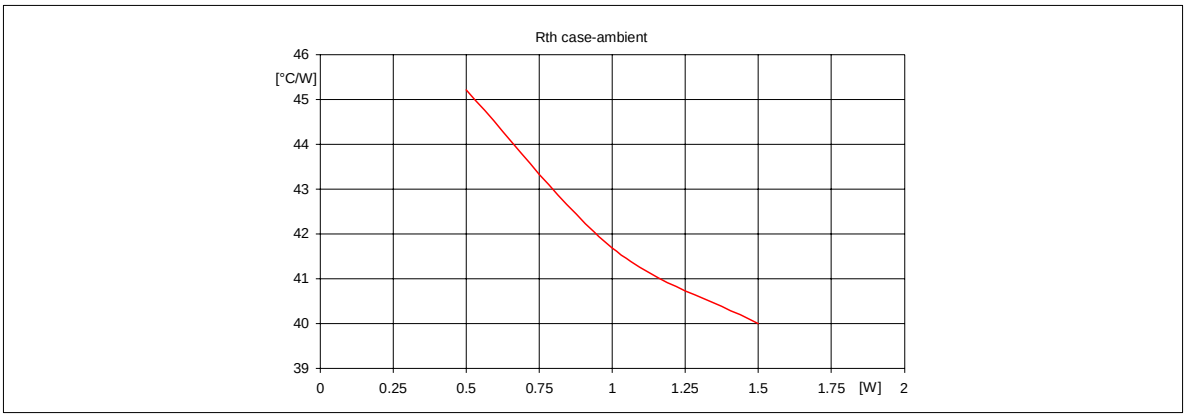
In figure 7 the SO-16 thermal characterization is reported. In this package eight pins are connected to the tab to reduce the junction-pin thermal resistance whereas the case-ambient thermal resistance is related to the copper area on the PCB (device heat-sink). The device has been characterized at three different copper areas: 0.5, 1 and 2 cm^2; at three different power dissipations: 0.25, 0.5 and 1W and measuring the devices case temperatures.

Figure 7: SO-16 $R_{th\ case\text{-}ambient}$ Vs. PCB Copper Area



In Figure 8 the SIP-9 thermal characterization (no heat-sink) is reported.

Figure 8: SIP-9 $R_{th\ case\text{-}ambient}$ (no heat-sink)

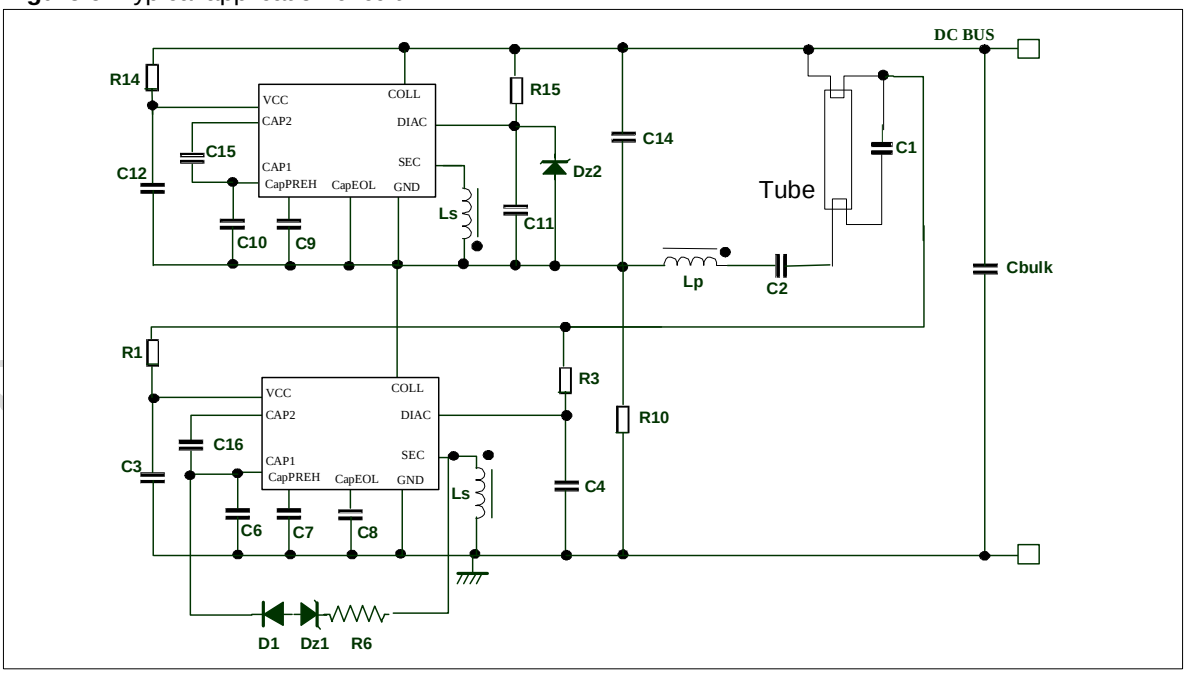


3. CONVERTER DESCRIPTION

In figure 9 the electrical scheme, realizing a voltage-feed converter based on VK06 is reported. The two windings L_s connected to the SEC pins are wound on the choke L_p. Four different operative phases can be described:

- start-up
- preheat
- steady state
- ignition

Figure 9: Typical application circuit



3.1 START-UP

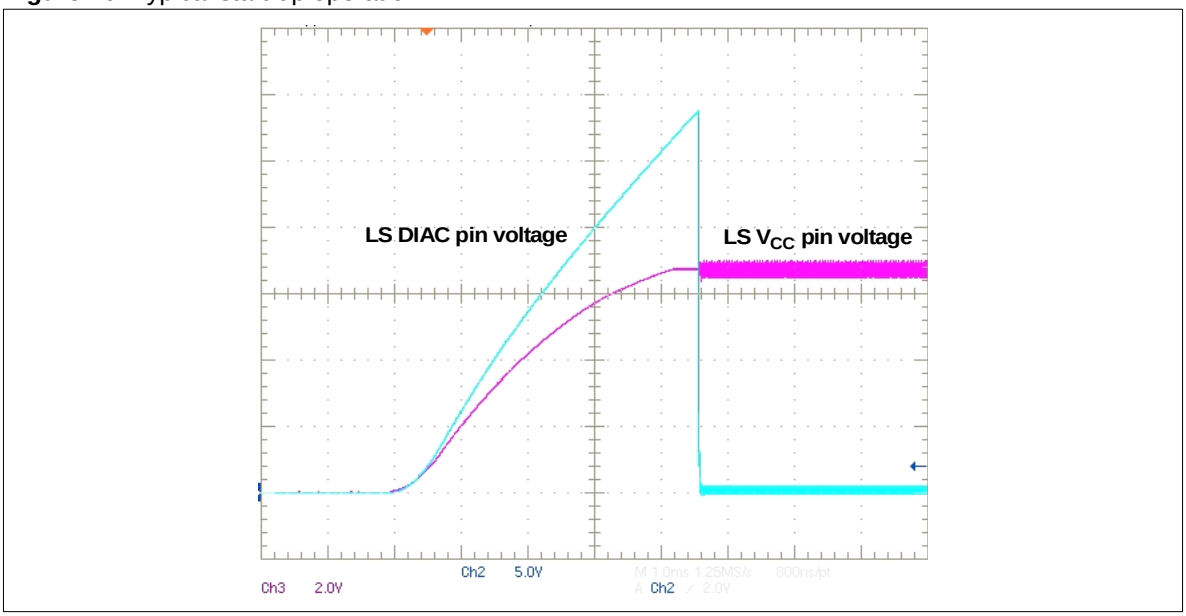
As soon as the system is supplied, the V_{CC} capacitors C3 and C12 start to be charged from the DC bus respectively by means of the resistors R1 and R14-R10. At the same time, the low side diac capacitor C4 starts to be charged by the resistor R3. The network R15-C11 biases the high side DIAC.

In normal operations the low side device is the one to go on the first time, while in the high side device the DIAC pin, clamped by Dz2, is used only to reset the preheating capacitor C9.

As soon as the voltage on C4 reaches about 28.5V the diac block switch ON the device. At that time both devices must be biased with the minimum requested V_{CC} voltage (~ 5V) in order to make the system oscillate properly.

In figure 10 low side (LS) diac and V_{CC} typical waveforms are shown. In the picture the V_{CC} voltage reaches 6.8V after 4.2m sec remaining constant at this value (it is internally clamped) until the converter starts to oscillate. At that time the storage charge recovery will be responsible for the device supply, charging the V_{CC} capacitor at the final voltage value (~6.8V).

Figure 10: Typical start-up operation



For the diac and V_{CC} biasing networks the following choices can be done:

$$R_{14}=R_{10};\ R_{14}+R_{10}=R_1;\ C_3=C_{12}$$

$$R_{15}>>R_{14}$$

With this setting the converter midpoint will stay at $V_{dcbus/2}$ and the voltages across C3 and C12 will be the same for any DC bus voltage.

For a proper start up phase the following condition has to be satisfied:

$$V_{C3}=V_{C12} \geq 5V \text{ when } V_{C4}=28.5V$$

Where:

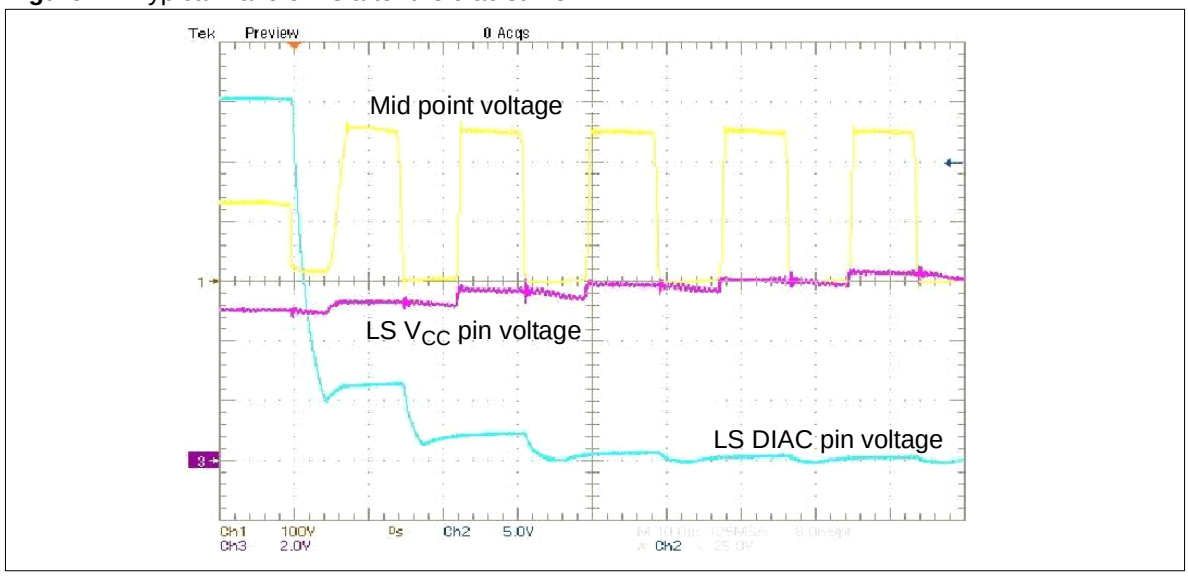
$$\tau_{Vc3}=R_1 \bullet C_3 = (R_{14} + R_{10}) \bullet C_{12}$$

$$\tau_{Vc4}=R_3 \bullet C_4 \text{ (low side)}$$

The network R15-C11 must be chosen to have the complete discharge of C9 when the low side diac strikes the converter. The zener diode Dz2 (~18V) clamps the DIAC pin below the diac activation threshold.

During oscillations the diac capacitors C4 and C11 will be discharged by the internal diodes connected between DIAC and Power collector while the V_{CC} capacitor will be charged by the charge recovered from the Power stage (see figure 11).

Figure 11: Typical waveforms after the diac strike



3.2 PRE-HEAT

Still referring to the figure 9, the capacitors C7-C9 (with C7=C9) fix the cathodes preheating time duration. The preheating frequency is set by the capacitors C10-C6 (with C10=C6).

3.2.1 PRE-HEATING TIME

CapPREH pin supplies a constant current $I_{capPREH}$~55µA. This current is supplied only during the t_{ON}.

The preheating ends when 4.2V is reached on CapPREH.

Assuming that

$$\Delta V_{CapPREH} = 4.2V$$

$$I_{CapPREH} \cong 55\mu A$$

the preheating time t_{preh} will be:

$$t_{preh} = C7 \bullet \frac{\Delta V_{CapPREH}}{\frac{I_{CapPREH}}{2}} = 0.15s/\mu F$$

3.2.2 PRE-HEATING FREQUENCY

For the pre-heating frequency calculation the following considerations can be done:

$$f = \frac{1}{T}$$

$$\frac{1}{2}T = t_{ON} + t_{storage} + t_{dV/dt}$$

$t_{storage} = const \approx 300nsec$ (storage duration of the device Power stage)

tdV/dt is the duration of the snubber capacitor (C14) charge during the half-bridge mid-point commutation between ground and V_{DC} bus.

It can be calculated using the following relationship:

$$t_{dV/dt} = C_{snubber} \times \Delta V / i_{peak}$$

where:

- ΔV (DC bus voltage);
- i_{peak} (peak current);
- $C_{snubber}$ (snubber capacitance).

t_{ON} is the conduction time fixed by the preheating frequency capacitor (C6) and device characteristics.

It can be calculated according to the following formula:

$$t_{ON} = K \bullet C6$$

Where K=6.7µsec/nF (fixed by the VK06)

3.3 STEADY STATE

The steady state frequency is set by the parallel of the capacitors C6-C16 for the low side and C10-C15 for the high side, where C16=C15. The same formulae of the preheat can be applied:

$$f = \frac{1}{T}$$

$$\frac{1}{2}T = t_{ON} + t_{storage} + t_{dV/dt}$$

$t_{storage} = const \approx 300nsec$

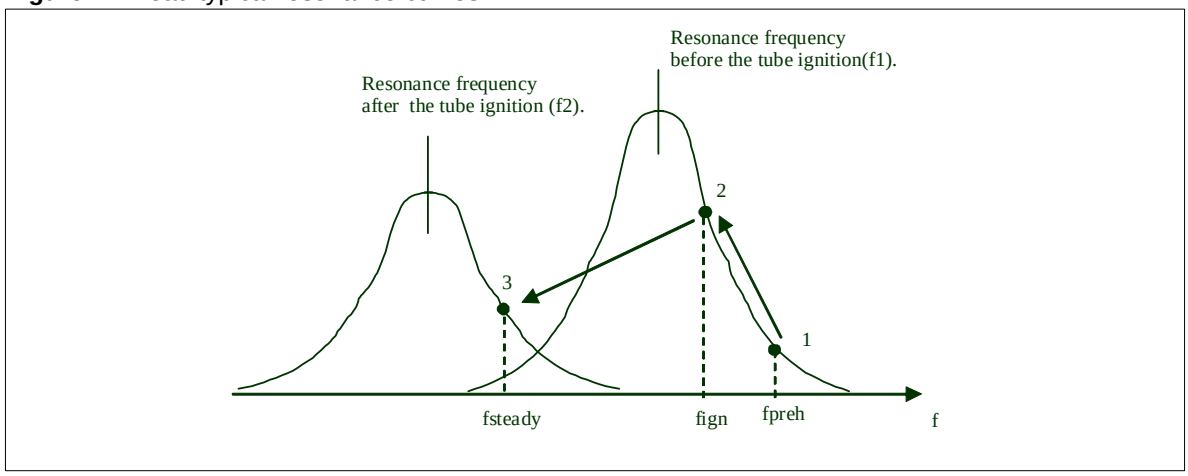
$$t_{ON} = K(C_6 + C_{16})$$

3.4 IGNITION

The converter of figure 9 has two different resonance frequencies, the first one before the tube ignition the second one after the tube ignition. The converter operation from preheat to steady state is shown in figure 12.

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Figure 12: Load typical resonance curves



Where the two frequencies are:

$$f_1 = \frac{1}{2\pi\sqrt{L_P(C_1 \text{ series } C_2)}}$$ (before the tube ignition)

$$f_2 = \frac{1}{2\pi\sqrt{L_P C_2}}$$ (after the tube ignition)

In good ballast design the cathode preheating is requested in order to increase the tube lifetime. It is obtained making high current flow through the cathodes for a fixed time. A simple rule for the preheating efficiency check is reported:

1) measure the cathode resistance at the beginning of the preheating;

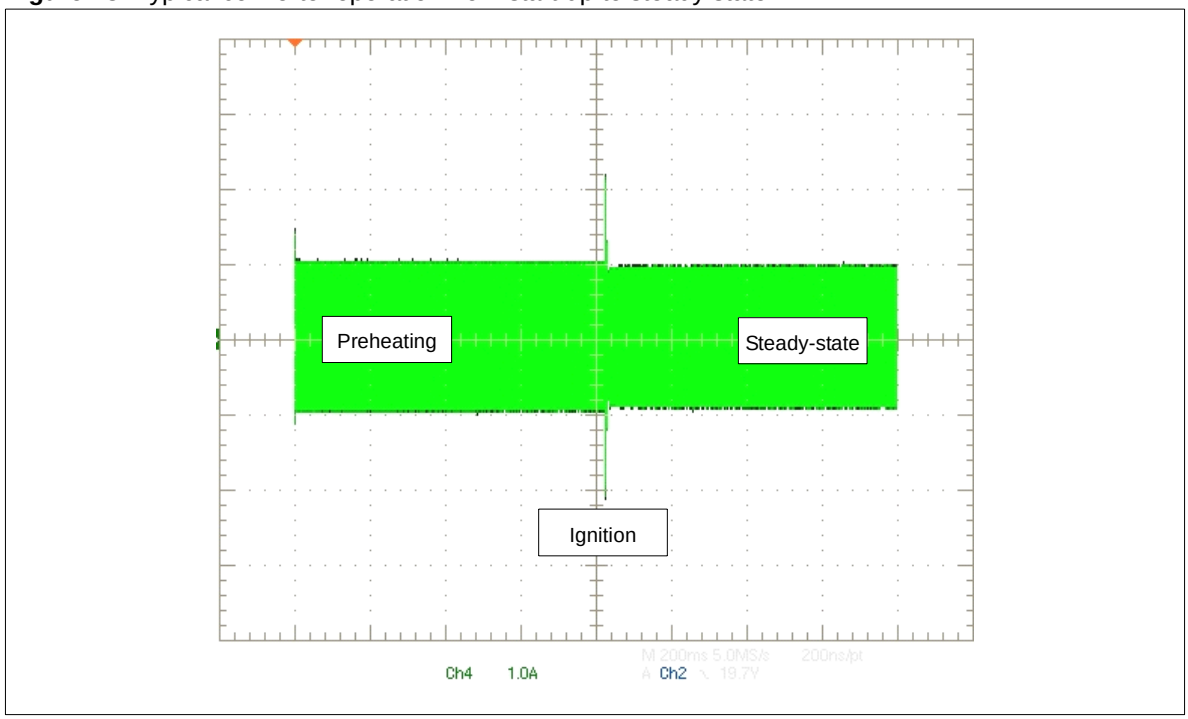
2) measure this resistance at the end of the preheating;

3) if its value is increased 3-4 times, the cathodes will work at the right temperature during ignition.

During the preheating the current level has to be able to heat the cathodes without generating the ignition voltage on the start-up capacitor C1. Still referring to figure 12, the converter will operate as follows: it will start working at the preheating frequency (dot 1) that must be higher than the resonance frequency f1. It will remain in this condition for the time fixed by the preheating capacitor. After the preheating the device frequency control is taken by the two secondary windings moving the working frequency up to the dot 2 where the tube is supposed to ignite. Once the tube is ignited the converter resonance frequency is lowered to f2 and the converter can work at the steady state frequency (dot 3) fixed by the oscillator capacitors.

In figure 13 the complete start-up sequence is shown.

Figure 13: Typical converter operation from start-up to steady state



3.5. PROTECTIONS

The converter is protected against:

- End of Life (EoL)
- Overtemperature
- Overcurrent

3.5.1 End of Life

If the tube is in EoL condition it will not ignite anymore forcing the converter to work at its resonance (f1) with very high current levels. This condition must be checked, stopping the oscillation, before the system destruction for high power dissipation. In the suggested converter (figure 9) the EoL condition is detected in the low side VK06 using the capacitor C8 connected to CapEOL pin. This pin is shorted (disabled) in the high side device.

The protection is activated as follows: an internal Rsense checks the current through the Power stage. If this current exceeds ~1.5A an internal generator supplies current (i_{EOL} about 350µA) to CapEOL pin. As soon as the voltage across CapEOL pin reaches ~4.3V (Δv_{EOL}) the Power stage is switched OFF, the diac is deactivated and the current consumption from V_{CC} is lowered. At the same time another current generator is activated latching the device. This condition is maintained until the DC bus voltage is present. The duration of EoL condition before latching is established by C8 according to the following considerations.

$$C_8 = \frac{I_M \times t_{EOL}}{\Delta v_{EOL}}$$

where:

I_M = average current flowing into C8 during the period of oscillation. Referring to the figure 14, I_M can be

$$I_M = \frac{i_{EOL} \times t_{charge}}{T} = i_{EOL} \times t_{charge} \times f$$

f is the frequency during EoL condition (~ resonance frequency)

Combining the equations we obtain:

$$C_8 = \frac{i_{EOL} \times t_{charge} \times f \times t_{EOL}}{\Delta v_{EOL}}$$

Figure 14: Device current during the EoL condition

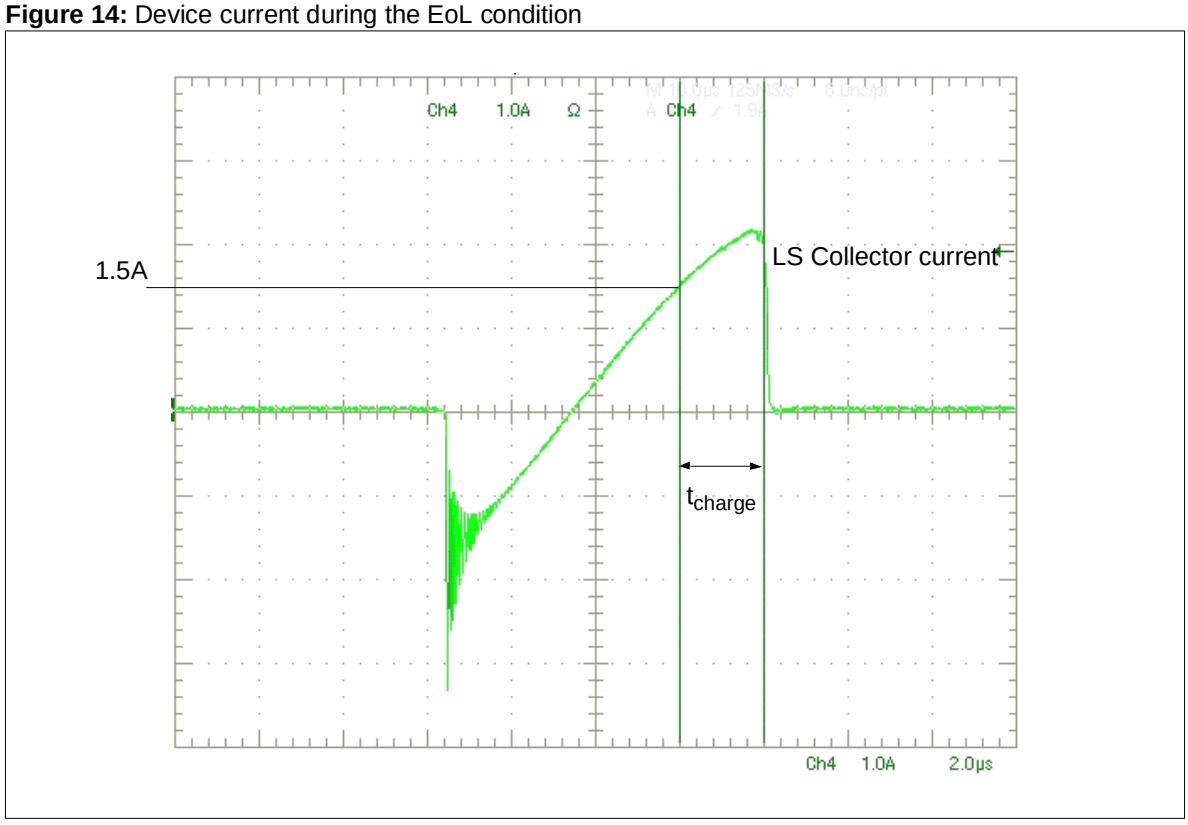
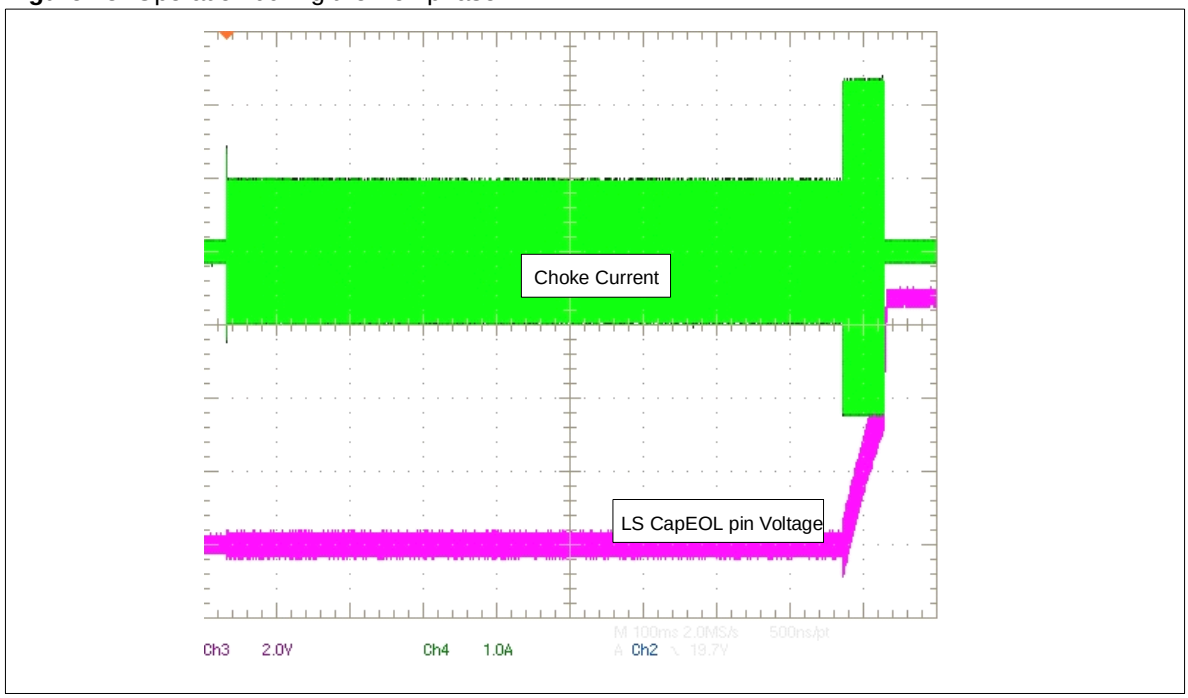


Figure 15 shows the operation during the EoL condition. The capacitor C8 is maintained discharged during the preheating phase and the oscillation are stopped as soon as it is charged to 4.3V

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Figure 15: Operation during the EoL phase



3.5.2 OVERTEMPERATURE

A thermal protection is activated when the junction temperature exceeds ~150°C. Its effect is the same of the EoL detection. For the timing definition it must be considered that the current generator on CapEOL pin is activated during the t_{ON} of the device.

The duration of the over-temperature condition before latching (t_{TH}) can be calculated as follows

$$t_{th} = C_8 \times \frac{\Delta v_{EOL}}{\frac{I_{EOL}}{2}}$$

where:

i_{EOL}= 350µA;

Δv_{EOL} =4.3V.

3.5.3 OVERCURRENT

The network D1, Dz1 and R6 connected between SEC and CAP1 pins realizes the overcurrent protection limiting the maximum accepted peak current. This function is very useful during the ignition and the EoL, where the converter, working very close to the resonance frequency (f1), can reach very high current levels (possibility of saturation of the transformer). This circuit is applied only on the low side VK06. It works anticipating the device switch OFF when a defined current level is reached, in other words the working frequency is increased. The modality is the following: an increasing in the current value causes an increase of the secondary winding voltage (we are working at the resonance frequency). As soon as this voltage exceeds the zener Dz1 + diode D1 breakdown, an amount of current will flow into

the frequency capacitor anticipating the device switch-OFF. The resistance R6 limits injected current realizing a delay in the capacitor charge. The diode D1 decouples SEC and CAP1 pins during the OFF state (negative voltage on SEC pin). In figure 15 the EoL intervention with the current limited at 2,4A is shown.

3.6 MORE ABOUT THE TRIGGER

With high resistive tubes the voltage on the secondary windings could decrease very rapidly, reaching the SEC pin switch-OFF threshold (0.9V), before than the internal oscillator switch OFF the device. This cause an increase of the working frequency.

The phenomenon can be explained as follows: the voltage drop on the choke Lp is equal to $V_{DCbus}/2$ minus the drop on the impedance made by the tube and C1 that is proportional to the current.

The voltage on the secondary windings is a fixed portion of the primary one. If the voltage on Lp becomes zero no voltage will be transferred on SEC pin and the device will be switched-OFF.

The higher is the tube impedance the lower is the current level at which the situation can occur.

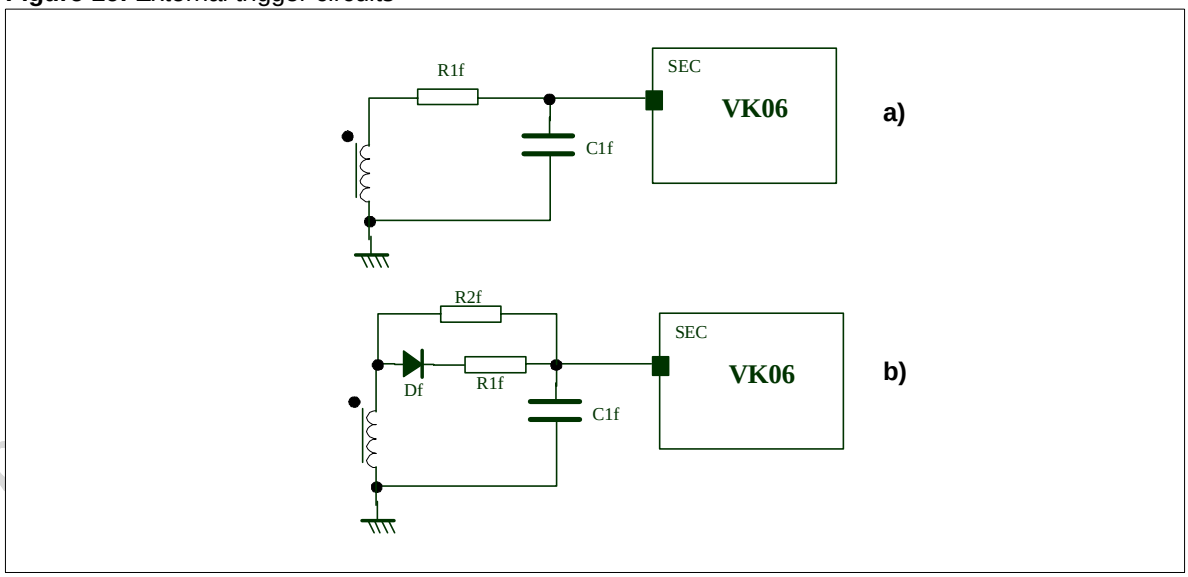
In this case to guarantee the right frequency control, an R-C or R-C-D filter has to be inserted between the secondary winding and SEC (see figure 16).

The values of R1f and C1f have to be chosen in order to maintain the voltage on SEC pin higher than ~0.9V during the fixed t_{ON} even if the voltage on the secondary winding becomes zero or negative.

On the other side it is important to have the SEC pin voltage higher than 2.2V before the end of the free-wheeling diode conduction to avoid delay at Power switch-ON. Therefore the filter dimensioning is a trade-off between the charge and the discharge time constant.

The circuit reported in figure 16b can be used if different and independent time constants are necessary.

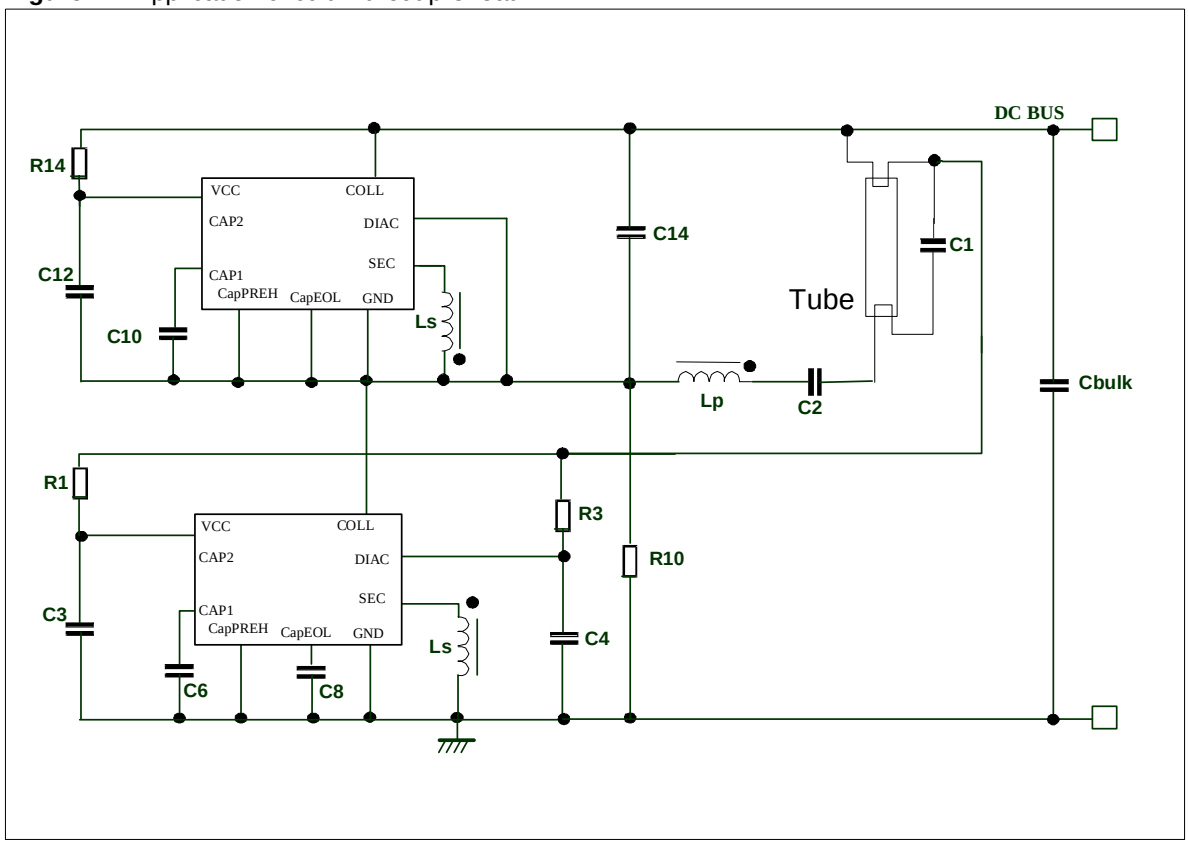
Figure 16: External trigger circuits



3.7 CONVERTER FOR COLD IGNITION APPLICATIONS (NO PRE-HEAT)

For applications where the pre-heating of the cathodes is not requested, it is possible to use a simplified converter as reported in figure 17.

Figure 17: Application circuit without preheat

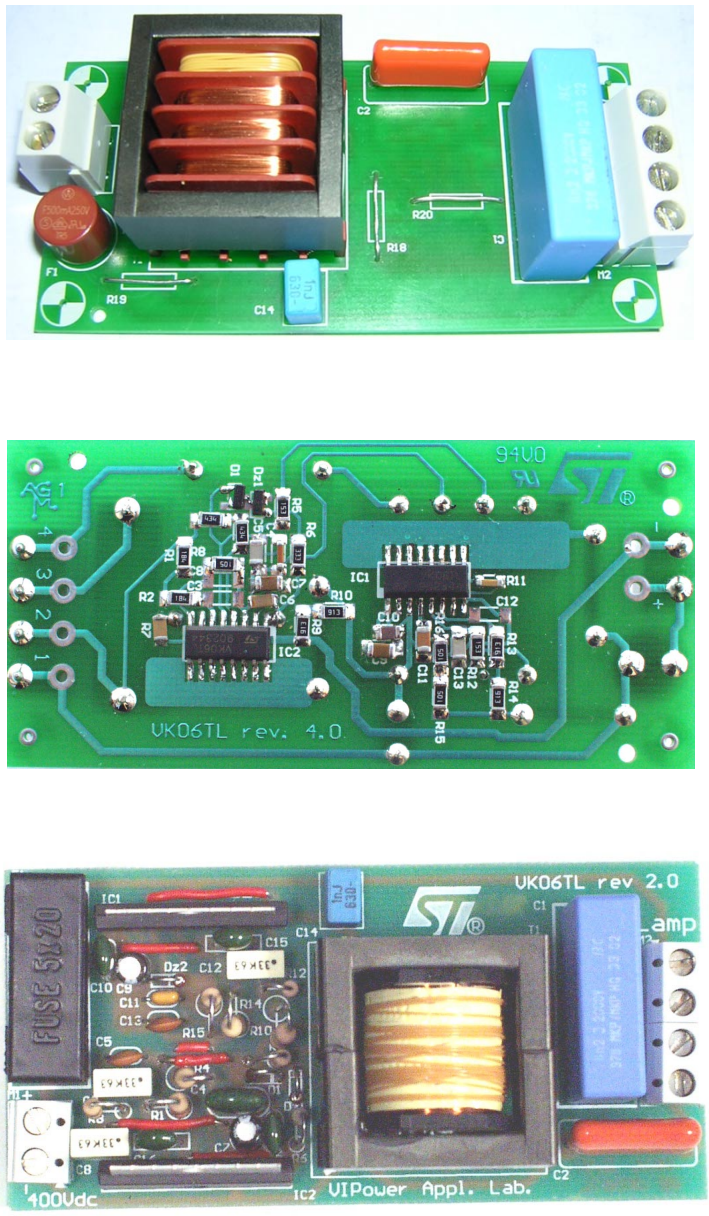


4. VK06 Design Reference

This design reference has been developed to help the VK06 users in the application board development.

To point out the maximum VK06 performances we decided to drive a 58W T8 FL tube. Two different PCBs have been realized, the first one using only surface mounting components and the second one using only through hole components. In the figure 18a, 18b, 18c their photos are shown.

Figure 18: VK06 demoboard: SMD components, top (a) and bottom (b) view; through-hole top view (c)



4.1 Electrical scheme

In figures 19 and 20 the electrical schemes for both trough hole and surface mounting demoboards are shown.

Figure 19: Through hole components demoboard electrical scheme

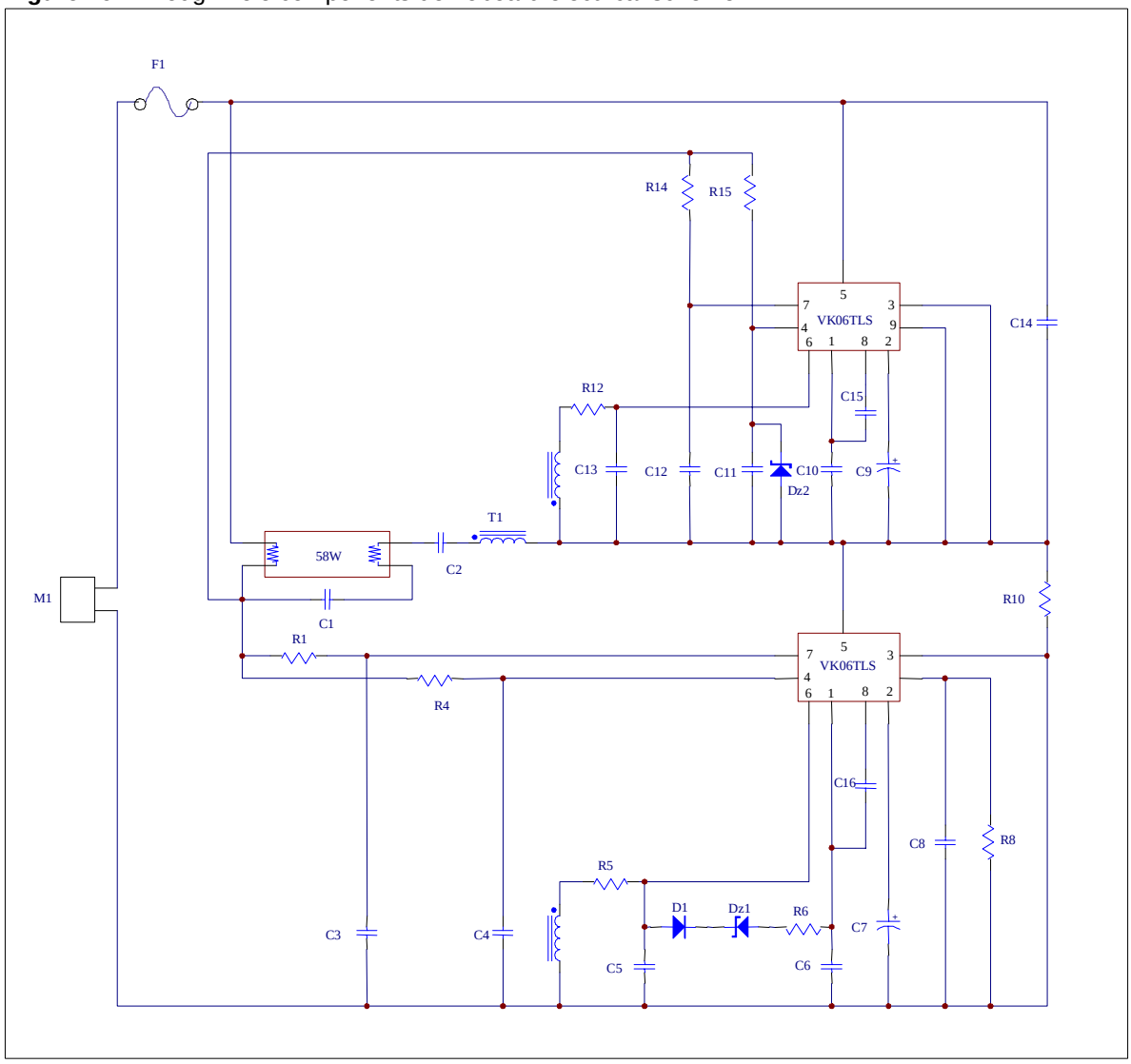
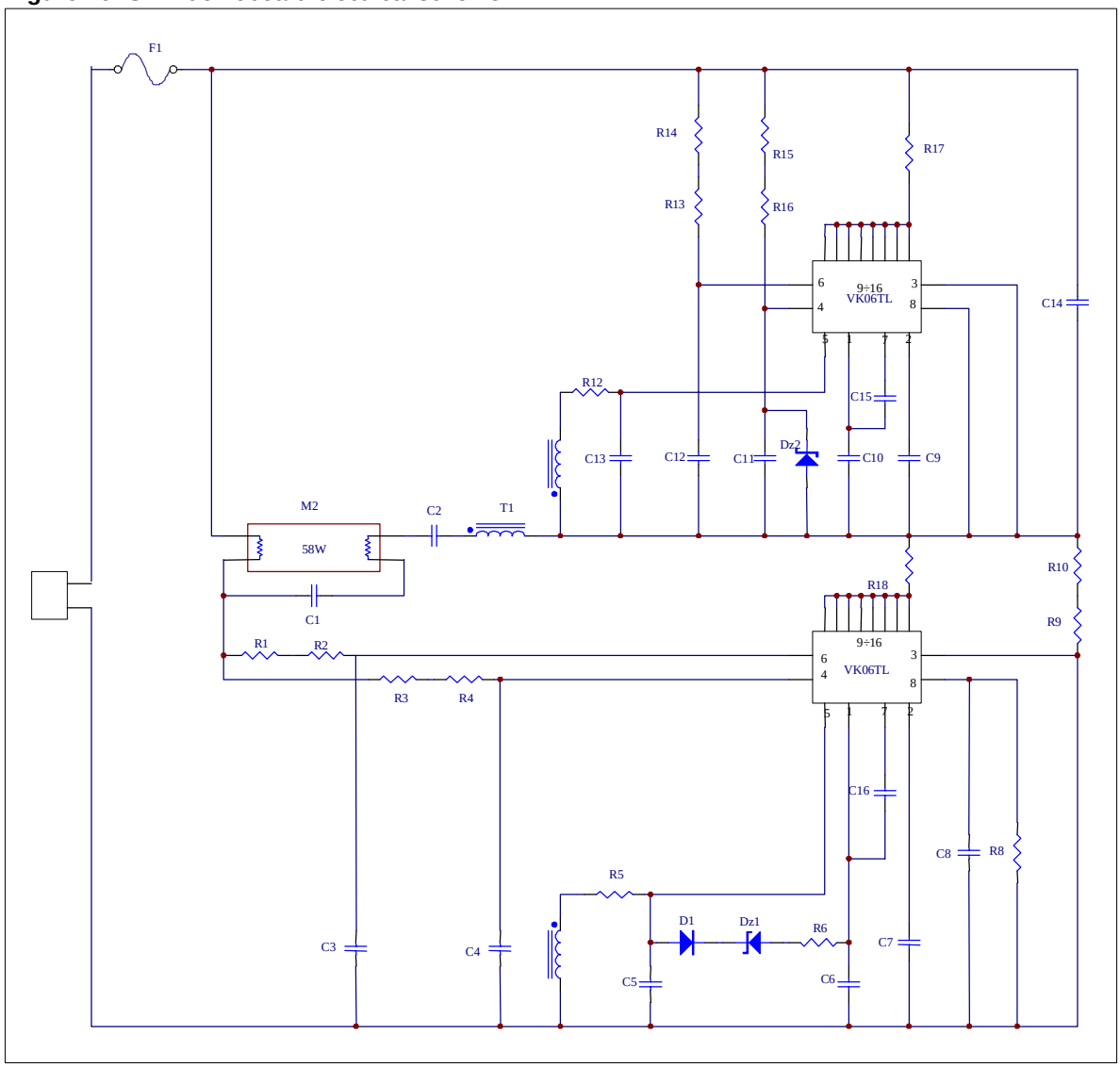


Figure 20: SMD demoboard electrical scheme



4.2. COMPONENTS LIST

The material lists for both PCB are reported in tables 1 and 2.

Table 1: Components list of the VK06 demoboard with trough hole components

Reference	Value	Description
R1	330kΩ 1/2W 5% 400V	Resistor
R4	1MΩ 1/2W 5% 400V	Resistor
R5, R12	15kΩ 1/4W 5%	Resistor
R6	68kΩ 1/4W 5%	Resistor
R8	1MΩ 1/4W 5%	Resistor
R10, R14	180kΩ 1/2W 5% 400V	Resistor
R15	2.2MΩ 1/2W 5% 400V	Resistor
C1	8.2nF 2000V 5%	Resonant capacitor
C2	100nF 400V	Capacitor
C3, C12, C8	330nF 16V 10%	Capacitor
C4	47nF 50V 10%	Capacitor
C5, C13	100 pF 100V 10%	Capacitor
C6, C10, C15, C16	1nF 2%	Capacitor
C7, C9	4.7µF16V 20%	Electrolytic capacitor
C11	10nF 50V	Capacitor
C14	1nF 630V	Snubber capacitor
D1	If=0.15A Vrrm=75V	Rectifier diode
Dz1	36V	Zener diode
Dz2	18V	Zener diode
T1	1.8 mH 10%	Resonant Inductor Pulse Eldor 60010019
IC1, IC2		**STMicroelectronics VK06TLS**

THROUGH HOLE COMPONENTS DEMOBOARD INDUCTOR SPECIFICATION

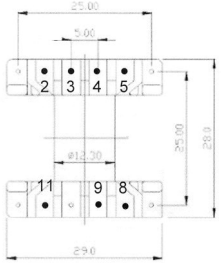
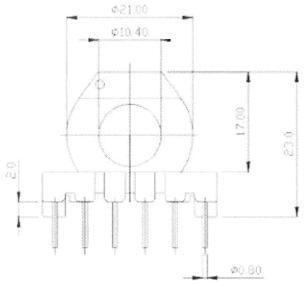
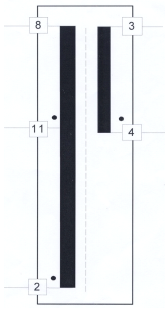
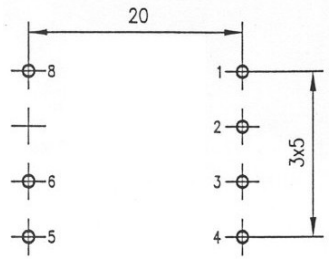
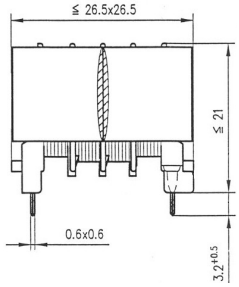
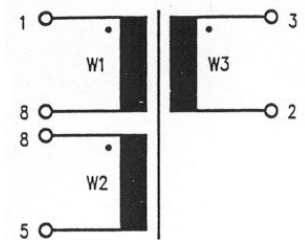
MECHANICAL DRAWING (Bottom view)	MECHANICAL DRAWING
	
ELECTRICAL CONNECTION	ELECTRICAL CHARACTERISTICS
	Nominal Inductance (W1=1-8) L=1.8mH ± 10% Core EC 28 Turn ratio = W1/W2=W1/W3=10 2 = Lamp; 3 = Ground; 4 = Low Side SEC pin; 5 = Not connected; 8 = High Side SEC pin; 9 = Not connected; 11 = Mid Point

Table 2: Components list of the VK06 demoboard with SMD components

Reference	Value	Description
R17,R18 R19,R20	0 Ω	Zero ohm Resistor
R15,R16	1MΩ 200V 5% 200V	Resistor 1206
R8	1MΩ 5%	Resistor
R3,R4	470kΩ 5% 200V	Resistor 1206
R1,R2	220kΩ 5% 0.25W 200V	Resistor 1206
R9,R10 R13,R14	100kΩ 5% 0.25W 200V	Resistor 1206
R5,R12	15kΩ 5%	Resistor
R6	68kΩ 5%	Resistor
C5,C13	100pF 100V 10%	Capacitor
C6,C10, C15,C16	1nF 2% 16V	Capacitor
C7,C9	4.7uF 10% 16V	Capacitor
C3,C8,C12	330nF10% 16V	Capacitor
C11	10nF 50V	Capacitor
C4	47nF 50V 10%	Capacitor
C1	8.2nF 5% 2000V	Resonant capacitor
C2	100nF 400V	Capacitor
C14	1nF 630V	Snubber capacitor
D1	If=0.15A Vrrm=75V	Rectifier diode
Dz1	36V	Zener diode
Dz2	18V	Zener diode
T1	1.8 mH 5%	Resonant Inductor VOGT: LL 010 205 31 TDK: SRW25EVD4-E01H003.
IC1, IC2		**STMicroelectronics VK06TL**

SMD COMPONENTS DEMOBOARD INDUCTOR SPECIFICATION

MECHANICAL DRAWING (Bottom view)	MECHANICAL DRAWING
	
ELECTRICAL CONNECTION	**ELECTRICAL CHARACTERISTICS**
	Nominal Inductance (W1=1-8) L=1.8mH ± 5% Core EVD 25 Turn ratio = W1/W2=W1/W3=10 1 = Lamp; 2 = Ground 3 = Low Side SEC pin; 5 = High Side SEC pin; 8 = Mid point

4.3. PCB DEFINITION

In figures 21 and 22 the proposed PCB for both SMD and trough hole demoboards are shown.

Figure 21: SMD PCB Bottom view (not in scale)

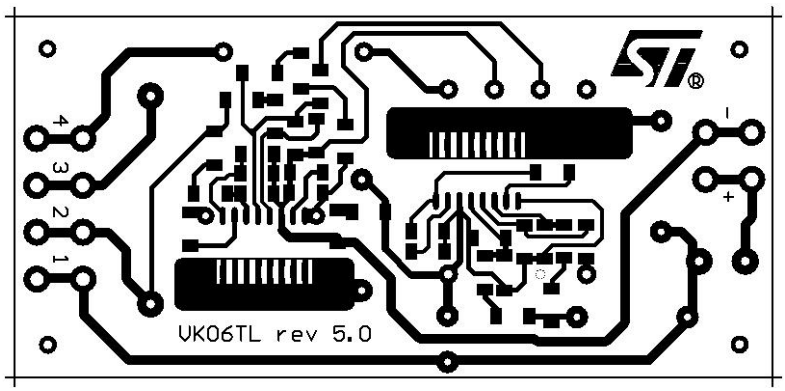
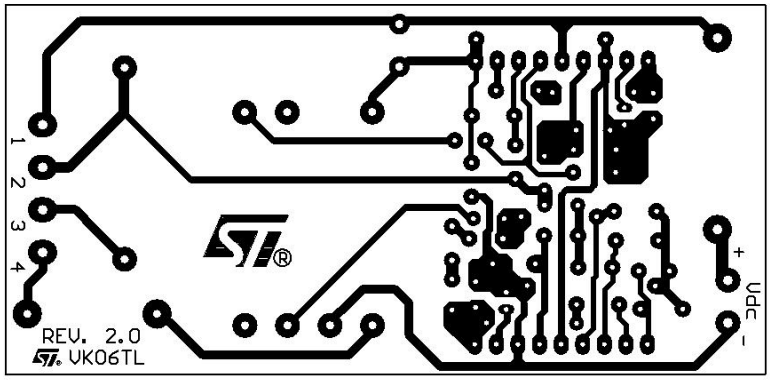


Figure 22: Through hole PCB Bottom view (not in scale)

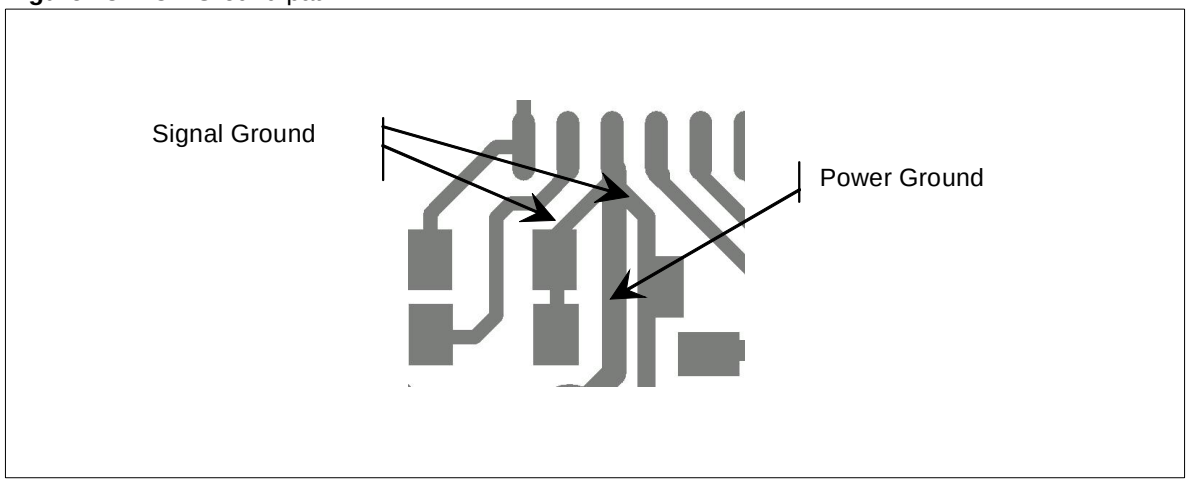


The components placement on the PCB is important and few simple rules have to be followed for its realization.

1) Frequency capacitor placement:
These components must be connected as close as possible to the CAP1 pin.

2) Ground path:
The ground paths (signal and power) must be separate in order to reduce interference on the logic part.
In figure 23 an example of this rule is shown.

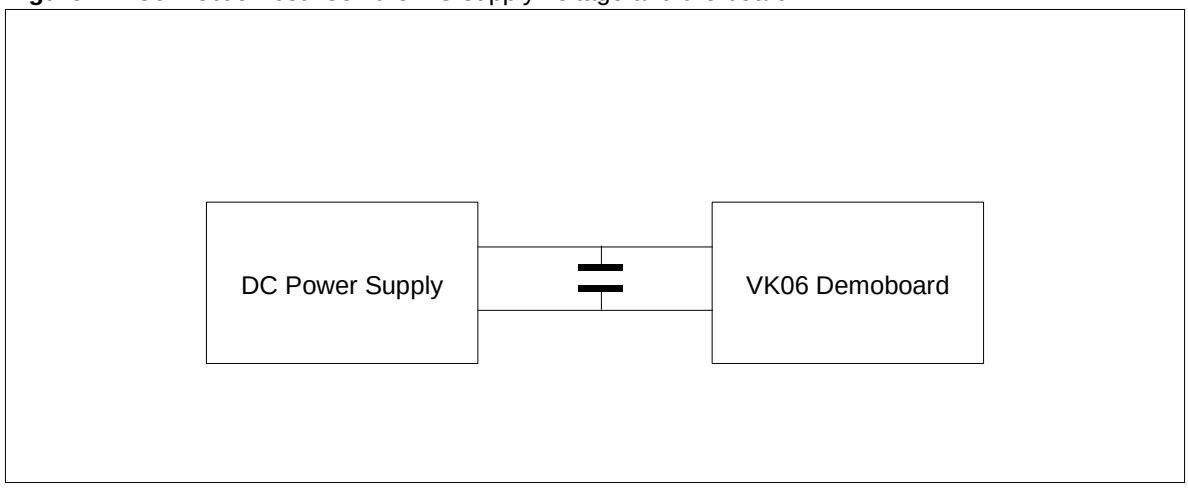
Figure 23: PCB Ground path



4.4. EXPERIMENTAL RESULTS

For the board testing it is important to connect on the input terminals an electrolytic capacitor (10µF, 450V), in order to bypass the parasitic inductance present in the connection wires between the DC supply voltage and the board (see figure 24).

Figure 24: Connection between the DC supply voltage and the board



All the measurements have been done supplying the converter with 400V DC.

4.4.1 START-UP PHASE

In figure 25 the start-up phase is shown. The voltages on the low side (LS) V_{CC} and diac pins are reported.

It is possible to notice that the V_{CC} voltage reaches its clamp value (~6.8V) before the diac strike. In figure 26 the first oscillation cycles after the diac strike are shown.

Figure 25: Start-up phase

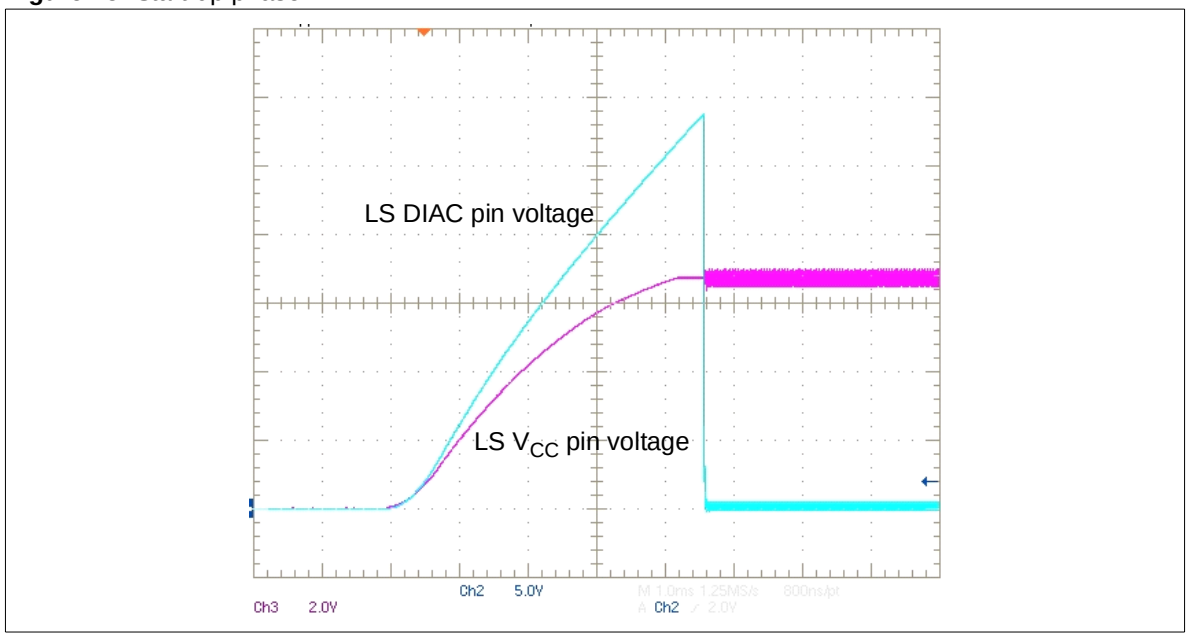
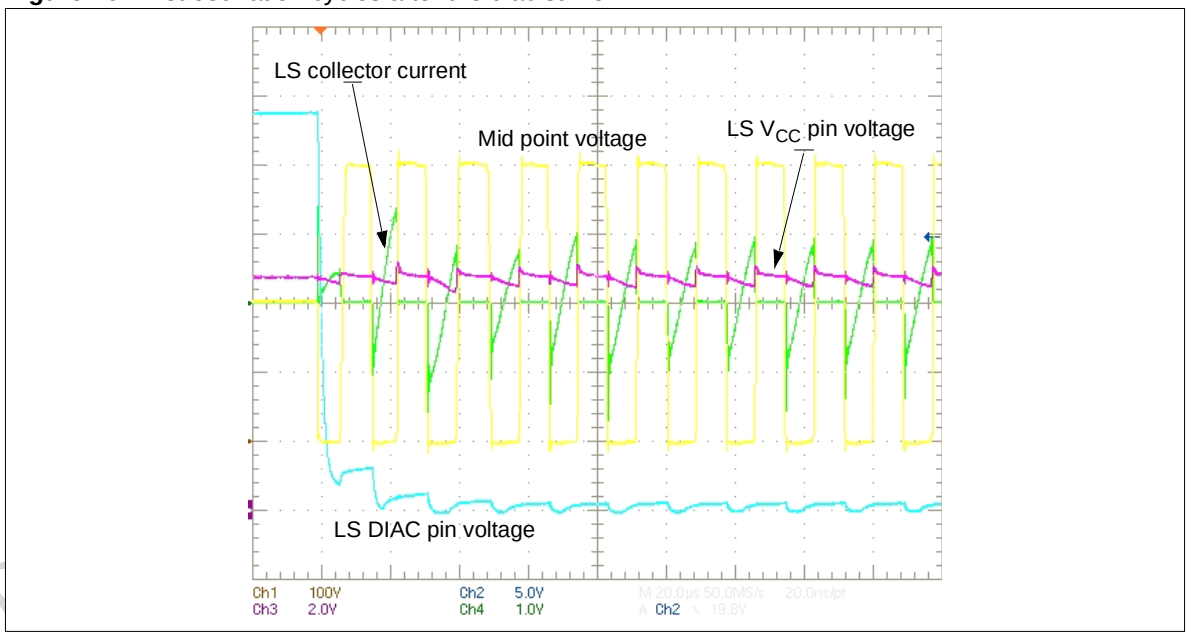


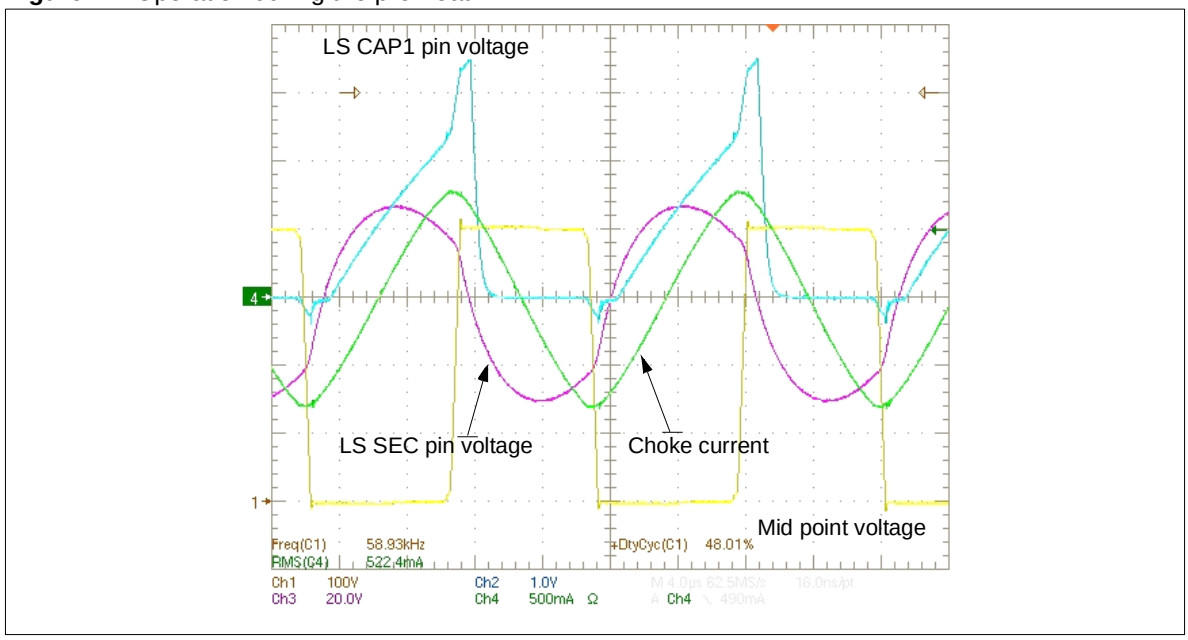
Figure 26: First oscillation cycles after the diac strike



4.4.2 PRE-HEATING PHASE

The preheating frequency has to be fixed in order to reach a current level enough to heat the cathodes without tube ignition. Figure 27 shows the main waveforms of the LS device.

Figure 27: Operation during the pre-heat

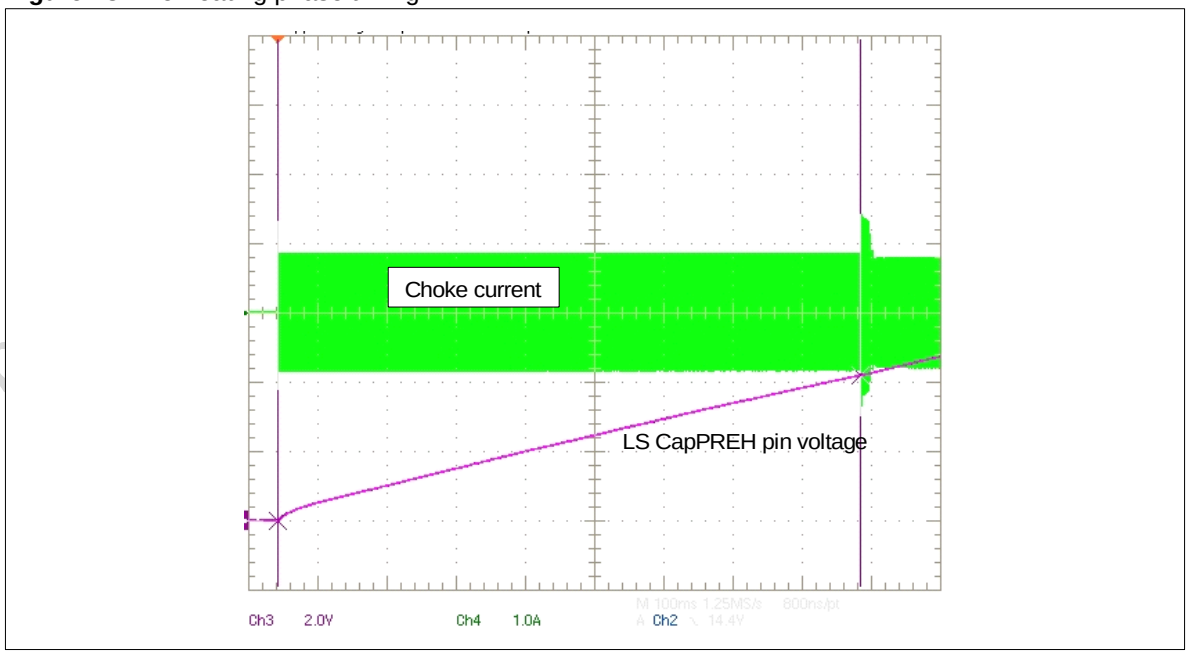


The preheating frequency is ~59KHz with a peak current of ~800mA.

Being the resonance capacitor C1= 8.2nF, during the preheat its voltage is lower than the preheating specification of a 58W T8 tube (350V peak).

Figure 28 shows the preheating timing. The choke current and the voltage on the CapPREH pin are reported. The preheating duration is ~0.84s (C7=4.7uF)

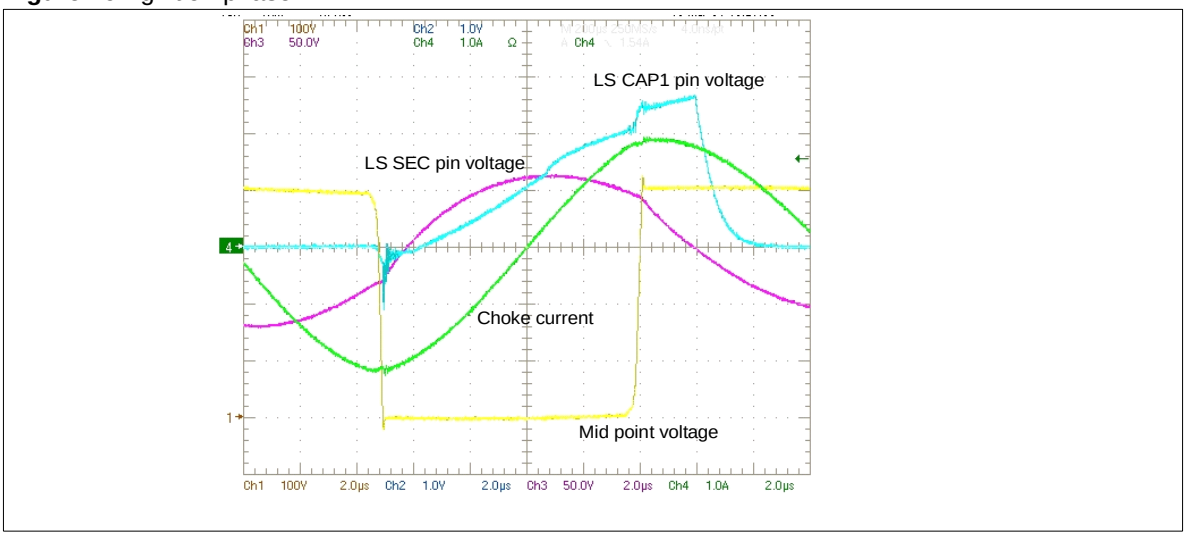
Figure 28: Pre-heating phase timing



4.4.3 IGNITION PHASE

Figure 29 shows the main waveform during the ignition phase. The peak current is limited to ~2A thanks to the overcurrent protection network made by D1, Dz1 and R6 (see figures 19 and 20). In fact as soon as the voltage on the sec pin overcomes ~40V the frequency capacitors charge becomes faster (see CAP1 waveform) anticipating the device switch-off.

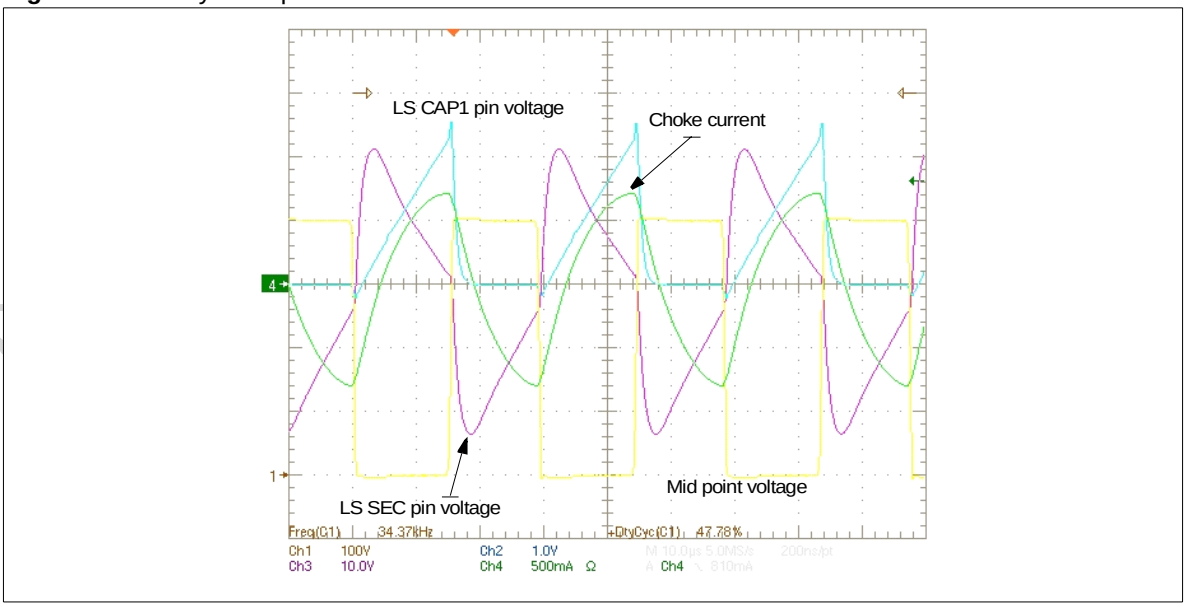
Figure 29: Ignition phase



4.4.4 STEADY STATE

Figure 30 shows the steady state phase main waveforms. The working frequency is ~34KHz with a peak current of ~700mA.

Figure 30: Steady state phase

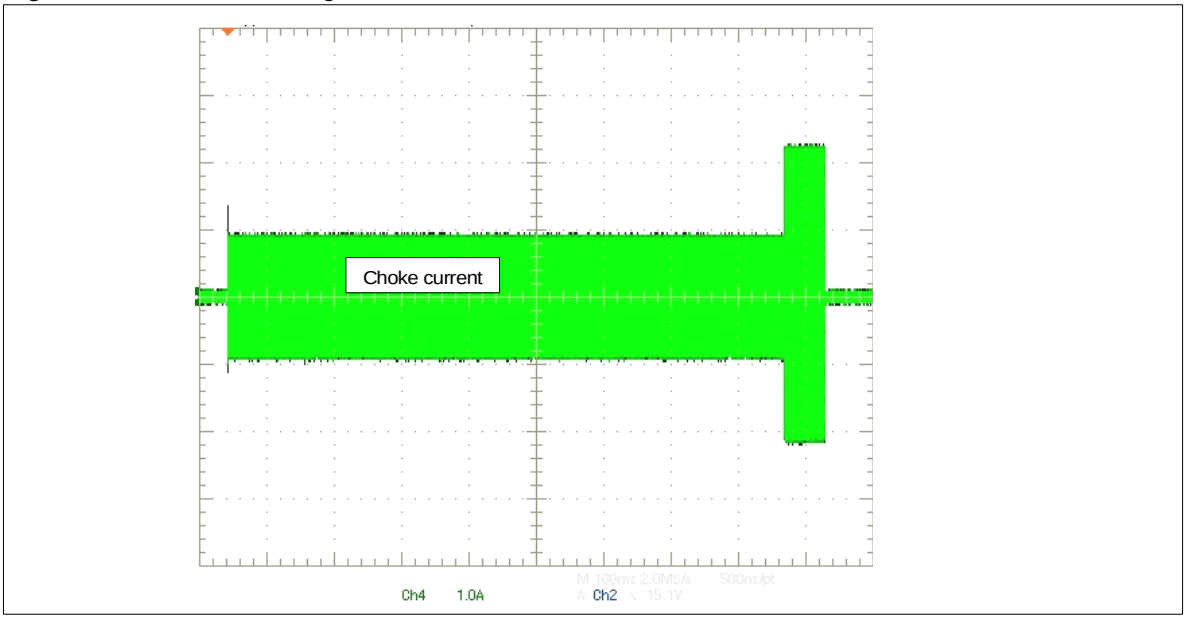


4.5 PROTECTIONS

4.5.1 End of Life

In figure 31 the timing of the EoL protection is shown.

Figure 31: End Of Life timing



The system operates as follows: after the start-up, the preheating phase starts and lasts ~0.84sec as in the normal operation. After the preheating phase the system could permanently work in free oscillation condition due to the EoL state. The protection stops the oscillation after ~50msec.

Figure 32: EoL: device turn-off

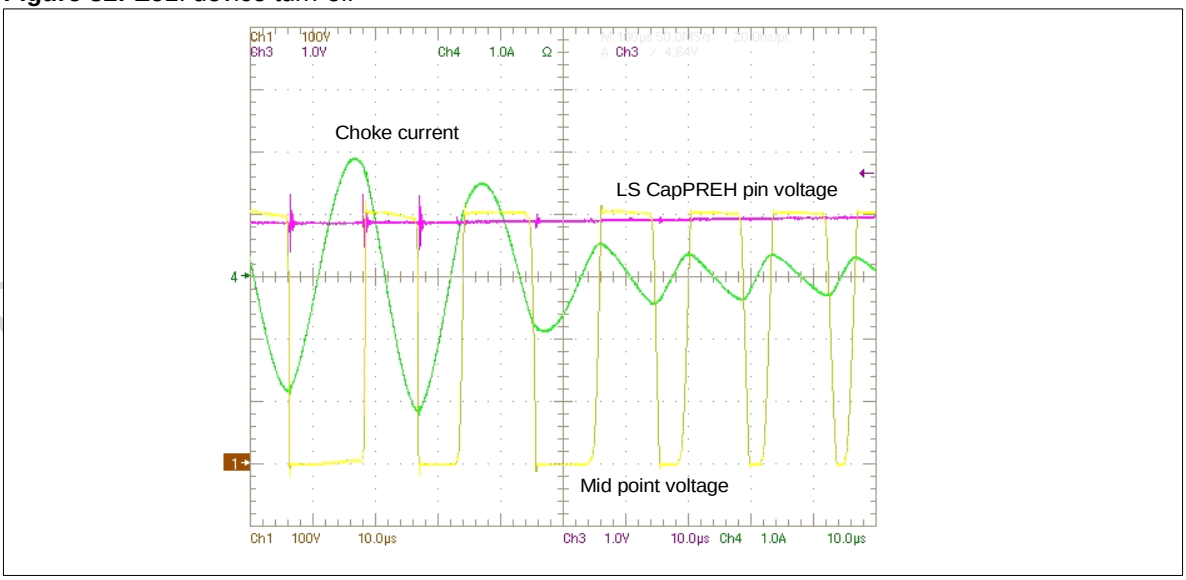


Figure 32 shows the particular of the LS device turn-off when the voltage on the LS CapPREH pin reaches the internal threshold.

4.6 THERMAL EVALUATION

The thermal analysis has been performed measuring the devices temperatures in the SMD version demoboard. The heat sink copper area copper area is ~100mm^2 for each device.

The temperature has been measured with K type thermocouples put on the top of the SO-16 packages.

The measurements have been performed at two different ambient temperatures: room temperature (about 25°C) and 50°C. The results are summarized in table 3.

Table 3: Devices temperature

$T_{ambient}$	T_{case}
25ºC	90ºC
50ºC	115ºC

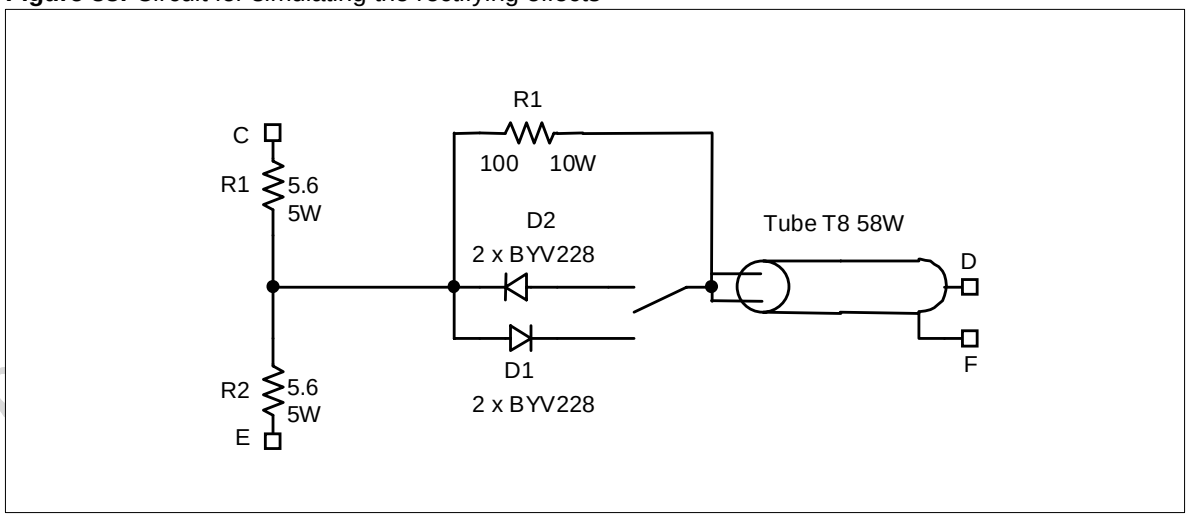
5. TUBE RECTIFICATION (not included in the reference demoboards)

Below, a network for the rectification detection is described. The dimensioning is related to a 58W T8 tube. This is an anomalous condition happening during the steady state phase causing lamp overvoltage and not overcurrent, for this reasons it is not possible to detect it by the EoL protection.

The proposed network realizes a lamp voltage sense. The timing and the device latch is realized using the same internal EoL circuit.

The circuit used to simulate the rectification condition has been realized according to E DIN IEC 61347-2-3/A1 2002-02 standard (see figure 33).

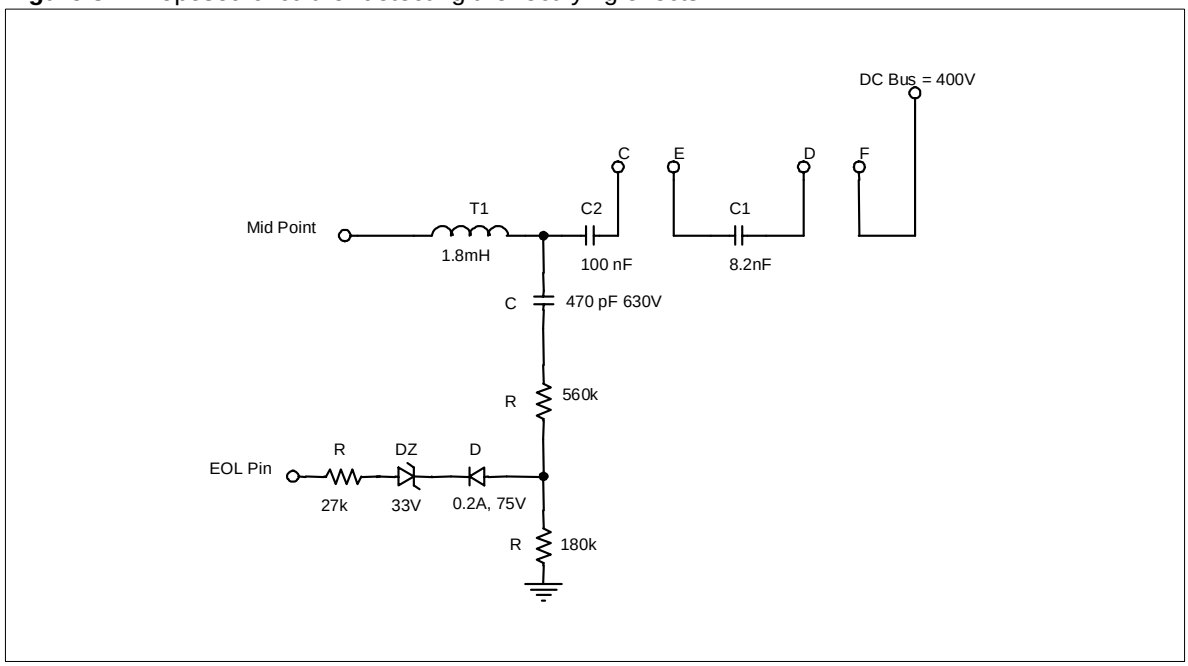
Figure 33: Circuit for simulating the rectifying effects



The points C,D,E,F must be connect to the VK06 converter output terminals.

In figure 34 the circuit used for the tube rectification detection is shown.

Figure 34: Proposed circuit for detecting the rectifying effects



The terminals C-E and D-F must be connected to the circuit of figure 33.

The rectification condition is detected monitoring the voltage across the 180kΩ resistor.

When the rectifying effects occur, the increase of the voltage across the lamp causes the increase of the voltage across the resistor R= 180kΩ over the threshold fixed by the network D-Dz-R. At that moment the EoL protection is activated.

During the preheating phase the voltage across the resistor R=180kΩ is higher than the steady state and the protection can be activated. For this reason a further circuit is needed for disabling the protection during the preheat.

6. CONVERTER FREQUENCY TOLERANCE VS. FREQUENCY CAPACITOR TOLERANCE

Following a practical example showing the variation of converter frequency versus the frequency capacitor tolerance.

The analysis has been performed in steady state condition but it is also applicable to the pre-heat.

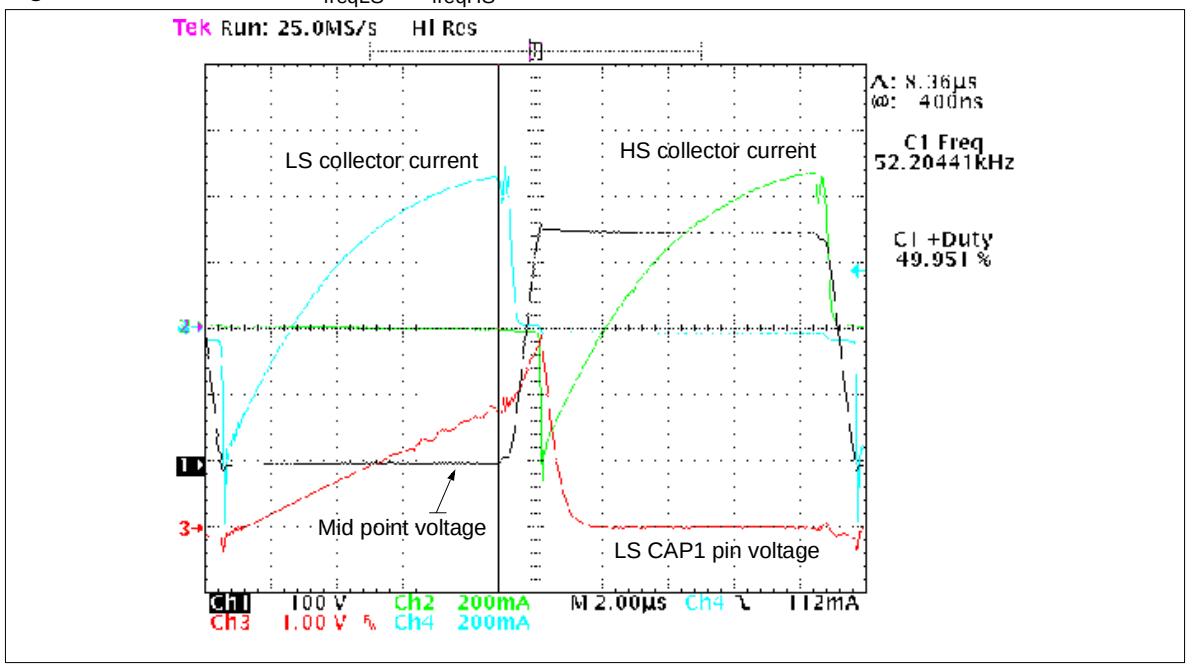
A VK06TL based prototype board with the following setting has been used:

V_{DC} bus= 350V

$C_{freqLS} = C_{freqHS}$ =C=1.22 nF (measured)

Figure 35 shows the related steady state waveforms.

Figure 35: Test condition: $C_{freqLS} = C_{freqHS}$



Following the measured parameters:

f=52.2KHz

duty cycle ≈ 50%

P=45.5W

With:

$t_{ONLS} = t_{ONHS}$ = 8.36µs

$t_{storageLS} = t_{storageHS}$ =320ns

dv/dt=920ns

According to the theoretical relationship:

t_{ON}=K*C with K=6.7µs/nF (5% internal guaranteed) (1)

The expected t_{ON} is:

t_{ON}= 6.7*1.22=8.2µs (inside 5% device tolerance)

- Experiment 1

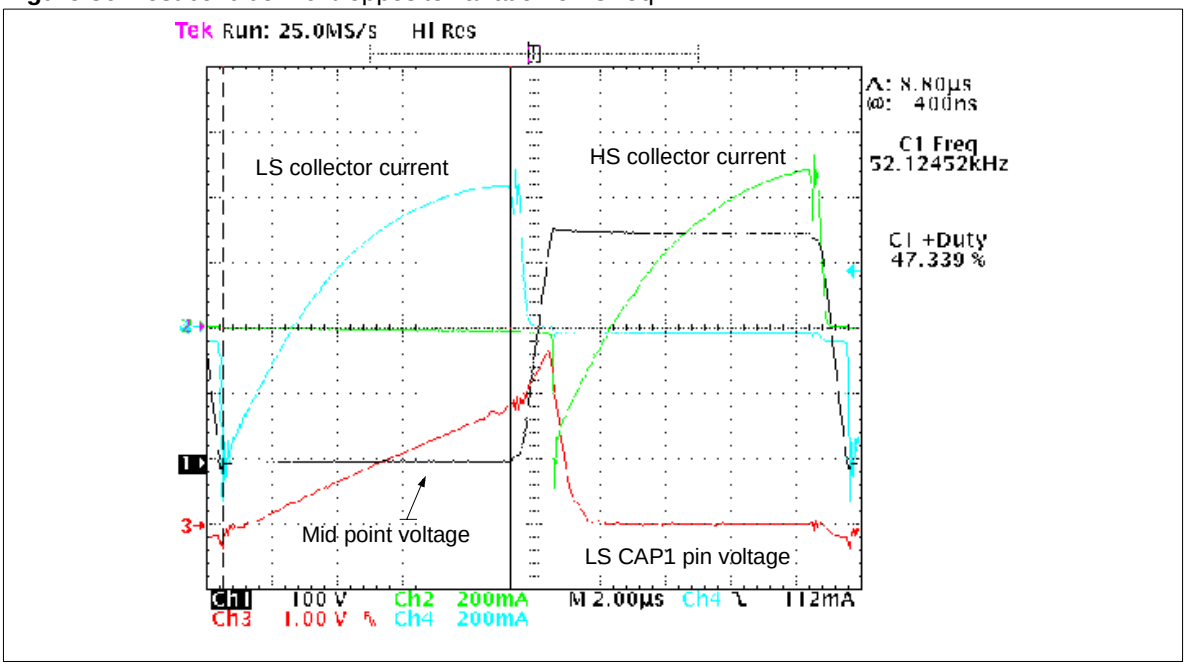
Only the frequency capacitors have been changed:

C_{freqLS}=C+6%

C_{freqHS}=C-6%

Figure 2 shows the related waveforms.

Figure 36: Test condition: 6% opposite variation on Cfreq

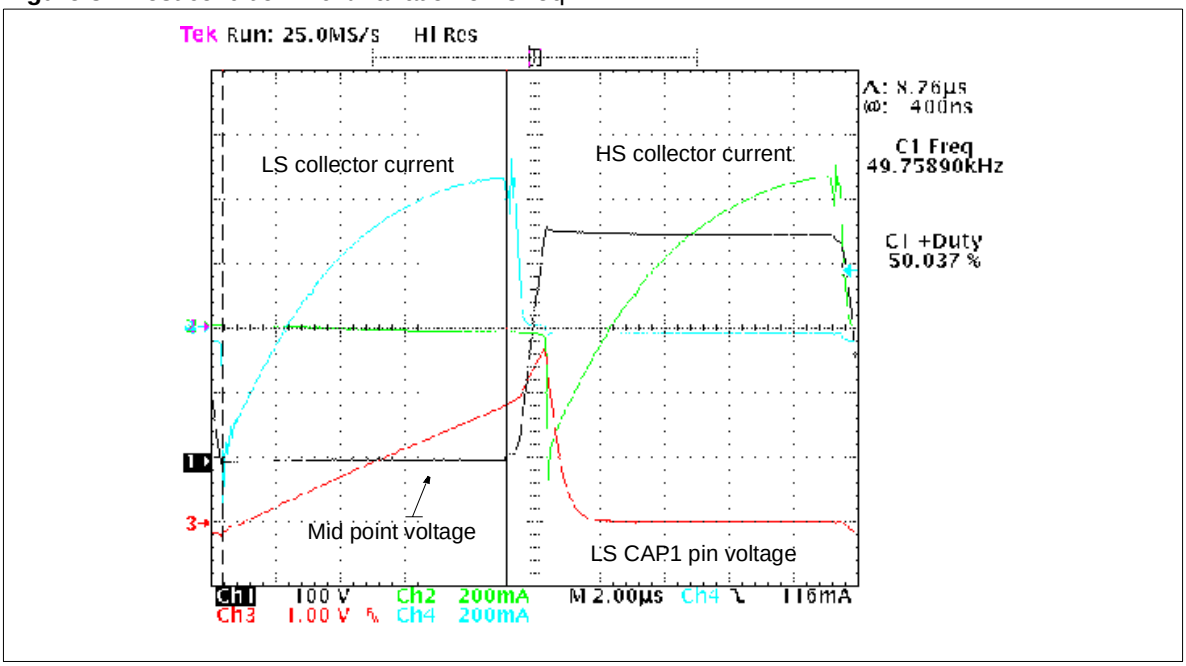


Following the measured parameters:
frequency f=52.12KHz
duty cycle ≈ 47.4%
P=45.5W
With:
t_{ONLS}=8.8µs (+6%)
t_{ONHS}=7.72µs (-6%)
$t_{storageLS}$ = $t_{storageHS}$ = 320ns
dv/dt=920ns

It means that the opposite variation of the t_{ON} causes a distortion of the duty cycle without variation on the frequency and power.

- Experiment 2
C_{freqLS}=C+6%
C_{freqHS}=C+6%
Figure 37 shows the related waveforms.

Figure 37: Test condition: +6% variation on Cfreq



Following the measured parameters:

f=49.8KHz

duty cycle ≈ 50%

P= 46.2W

With:

T_{onLS}= T_{onHS}=8.8µs (+6%)

$T_{storageLS}$= $t_{storageHS}$ =320ns

dv/dt=920ns

The frequency variation respect to the initial condition (C_{freqLS} = C_{freqHS} = 1.22 nF) is 4.6% and it is less than the capacitor tolerance (6%). The power variation is instead ~1.6%.

According to the relationship (1), the same results can be obtained if the t_{ON} variation is caused only by VK06TL internal tolerance. The worst case frequency variation will be anyway less than 5%.

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