STRUCTURE Silicon Monolithic Integrated Circuit
PRODUCTSERIES 2-ch Switching Regulator Controller

TYPE **BD9846FV**

FEATURES
- High Input-voltage (Vcc=35V)
- MOSFET-driver circuit built-in (dual circuit for step-down output)
- Built-in circuits for error amplifier reference voltage (ch1:eternal regulation is possible , ch2:1.0 V±1%)
- Over current detection circuit built-in.
- Soft-start timing adjustable

○Absolute maximum ratings (Ta=25℃)

Item	Symbol	Limits	Unit
Power Supply Voltage	Vcc	36	V
Power dissipation	Pd	812*1	mW
Output pin voltage	VOUT	Vcc-7V～Vcc	V
C5V pin voltage	VC5V	Vcc-7V～Vcc	V
Operating temperature	Topr	-40～+105	℃
Storage temperature	Tstg	-55～+150	℃
Maximum Junction temperature	Tjmax	150	℃

*1 Should be deleted by 6.5mW/℃ at Ta=25℃ or more. When mounted on a glass epoxy PCB of 70.0mm × 70.0 mm × 1.6 mm

○Recommended operating range (Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	Vcc	3.6	6.0	35	V
Output pin voltage	VOUT	C5V	-	Vcc	V
Error amplifier input voltage	VERRIN	0	-	1.6	V
Timing capacitor	CCT	47	-	3000	pF
Oscillation frequency	fosc	100	-	1500	kHz
STB input voltage	VSTB	0	-	VCC	V

○Electrical characteristics (Unless otherwise specified, Ta=25℃, VCC=6V)

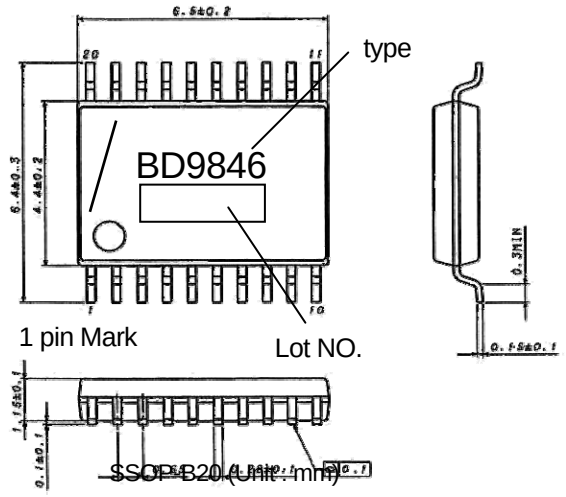
Item	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
【VREF output block】						
VREF output voltage	VREF	2.475	2.500	2.525	V	IO=0.1mA
Line regulation	Line reg.	—	1	10	mV	Vcc=3.6V→35V
Load regulation	Load reg.	—	2	10	mV	IO=0.1mA→2mA
Output max. current	IOMAX	2	13	—	mA	VREF=(typ.) ∗ 0.95

○Electrical characteristics (Unless otherwise specified, Ta=25℃, VCC=6V)

Item	Symbol	limits			Unit	Conditions
		Min.	Typ.	Max.		
【Triangular wave oscillator block】						
Oscillation frequency	fOSC	95	106	117	kHz	CCP=1800pF
Frequency variation	fDV	—	0	1	%	Vcc=3.6V→35V
【Soft-start block】						
SS pin source current	ISSSO	1.4	2	2.6	μA	SS=0.5V
SS pin sink current	ISSSI	5	12	—	mA	SS=0.5V
【Dead time adjustable circuit block】						
DT pin input bias current	IDT	—	0.1	1	μA	DT=1.75V
DT pin sink current	IDTSI	1	3.3	—	mA	DT=1.75V, (OCP+)-(OCP-)=0.5V
【UVLO block】						
Threshold voltage	VUTH	3.0	3.2	3.4	V	Vcc when rise time
Hysterisis	VUHYS	—	0.15	0.25	V	
【Error Amp block】						
NON input bias current (ch1)	Inon	−	0	1	μA	NON=1V
Non-Inverting input reference voltage(ch2)	VINV	0.99	1	1.01	V	INV=FB
Reference voltage variation (ch2)	dVinv	−	1	6	mV	Vcc=3.6V→35V
INV input bias current	IIB	—	0	1	μA	INV=1V
Open loop gain	AV	70	85	—	dB	
Output FB voltage (Hi)	VFBH	2.30	—	VREF	V	
Output FB voltage (Low)	VFBL	−	0.6	1.3	V	
Output sink current	IFBSI	0.5	1.5	−	mA	FB=1.25V , INV=1.5V
Output source current	IFBSO	50	105	−	μA	FB=1.25V , INV=0V
【PWM comparator】						
Input threshold voltage (fosc=100kHz)	Vt0	1.4	1.5	1.6	V	On duty 0%
	Vt100	1.9	2	2.1	V	On duty 100%
【Output block】						
Output ON resistance H	RONH	−	4	10	Ω	RONH=(VCC -OUT)/ Iout, Iout=0.1A
Output ON resistance L	RONL	−	3.3	10	Ω	RONL=(OUT-C5V)/ Iout, Iout=0.1A
C5V clamp voltage	VCLMP	4.5	5	5.5	V	VCLMP= VCC-C5V , VCC ＞7V
【Over current protection circuit (OCP) block】						
OCP threshold voltage	VOCPTH	0.04	0.05	0.06	V	Voltage between (OCP+)-(OCP-)
OCP-input bias current	IOCP-	−	0.1	10	μA	OCP+= VCC, OCP-= VCC-0.05V
Delay time for OCP	tdocpth	—	200	400	nS	OCP-= VCC→VCC-0.2V
Min. hold time for OCP	tdocpre	0.8	1.6	—	mS	OCP-= VCC-0.2V→VCC
【Stand-by switch block】						
Threshold voltage for each CH stop	VDTthL	1.1	1.25	1.4	V	DT Pin H/L
Stand-by mode setting voltage range	VSTBL	0	−	0.5	V	
Active setting voltage range	VSTBH	3	−	VCC	V	
STB current	ISTB	—	70	100	μA	STB=6V
【Total device】						
Stand-by current	ICCS	—	0	1	μA	STB=0V
Average current consumption	ICCA	1.5	3	6	mA	INV=0V, FB=H, DT=1.75V

※Not designed for radiation resistance.

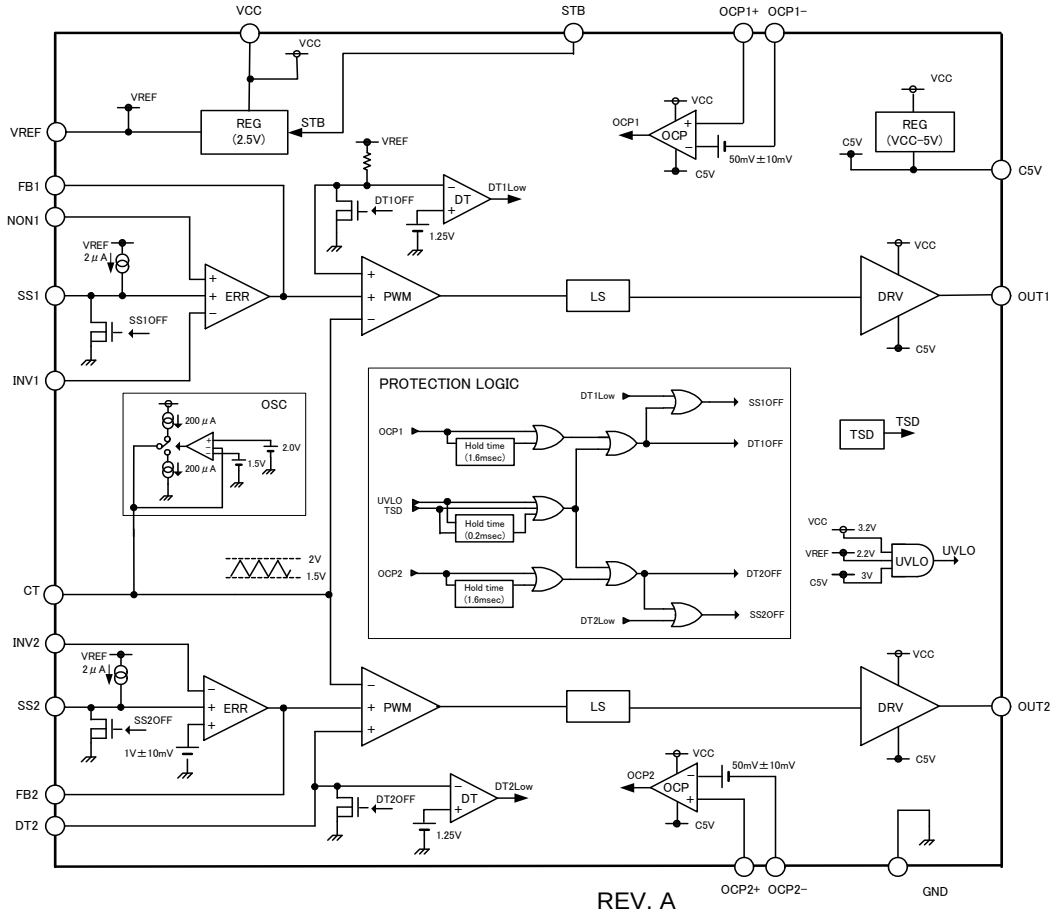
○Outline figure



○PIN No./ name / function

Pin No.	Pin name	Pin function
1	CT	External Capacitor pin for timing change
2	DT2	Dead time setting (CH2)
3	SS2	Soft-start time setting (CH2)
4	INV2	Error Amp inverting input (CH2)
5	FB2	Error Amp output (CH2)
6	GND	GROUND
7	OCP2−	Over current error amp inverting input (CH2)
8	OCP2＋	Over current error amp input (CH2)
9	C5V	Output L voltage（Vcc-5V）
10	OUT2	CH2 Output
11	OUT1	CH1 Output
12	Vcc	Power supply input
13	OCP1＋	Over current error amp input (CH1)
14	OCP1−	Over current error amp inverting input (CH1)
15	STB	Stand-by mode control
16	FB1	Error Amp output (CH1)
17	INV1	Error Amp inverting input (CH1)
18	SS1	Soft-start time setting (CH1)
19	NON1	Error Amp input (CH1)
20	VREF	Reference voltage（2.5V）output

○Block Diagram



○Operation Notes

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

3) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

5) Operation in a strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)
This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

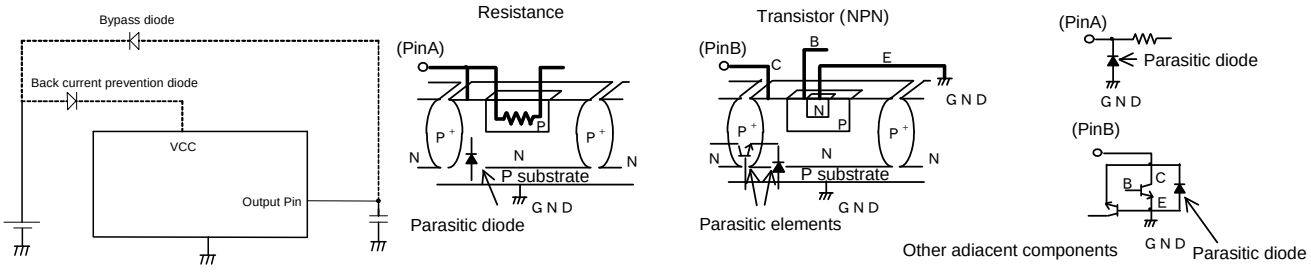
7) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

8) Common impedance
Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

9) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.
For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.

10) IC pin input
This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated.
P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when a resistor and transistor are connected to pins as shown in Fig. 10,
- ○ The P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- ○ Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



Notes

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