AP3598A

COMPACT DUAL-PHASE SYNCHRONOUS-RECTIFIED BUCK CONTROLLER

NEW PRODUCT

Description

The AP3598A is a dual-phase synchronous buck PWM controller with integrated drivers which are optimized for high performance graphic card and computer applications. The IC is capable of delivering up to 60A output current capability, supporting 12V MOSFET drivers with internal bootstrap diodes.

The dynamic output voltage could be implemented by analog method with a switching device and a resistor network. The adjustable current balance is achieved by $R_{DS(ON)}$ current sensing technique.

The AP3598A provides over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

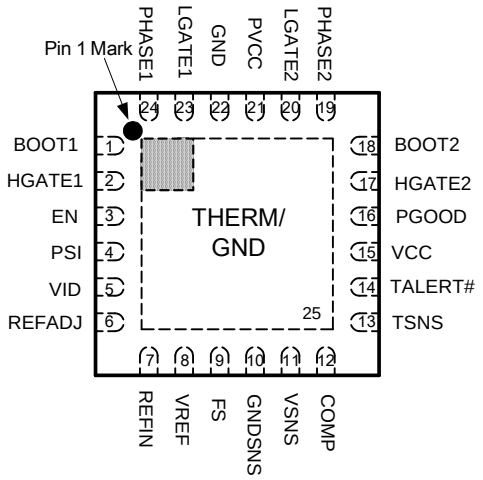
Other features include adjustable soft start, adjustable operation frequency and so on. With aforementioned functions, the IC adopts U-QFN4040-24 package.

Features

- Operate with Single Supply Voltage
- Reference Voltage Output with 1% Accuracy
- Simple Single Loop Voltage Mode Control
- 12V Bootstrapped Drivers with Internal Boot-strap Diodes
- Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing
- Adjustable Operation Frequency from 200kHz to 500kHz Per Phase
- External Compensation
- Dynamic Output Voltage Adjustment
- Adjustable Soft Start
- Built-in UV and OV Protection Function
- Built-in Over Current Protection
- Built-in Thermal Shutdown Function
- U-QFN4040-24 Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments

(Top View)



U-QFN4040-24

Applications

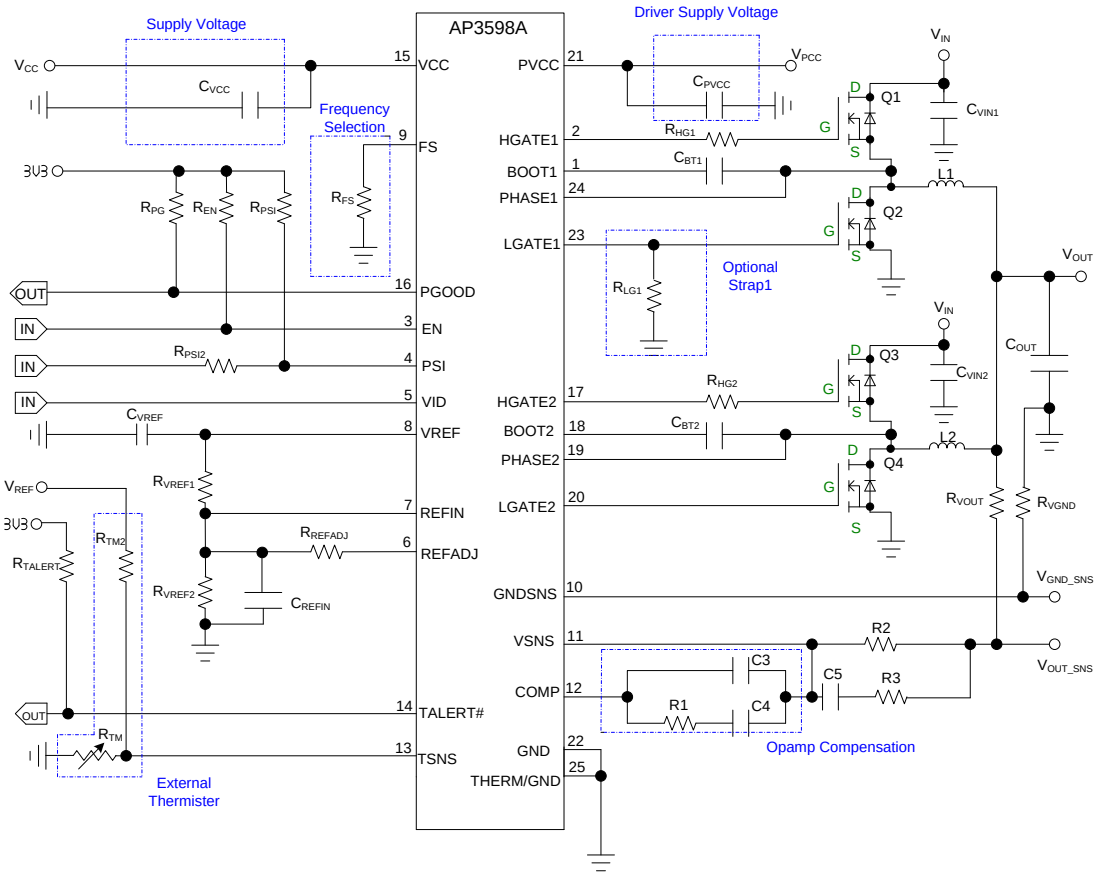
- Middle-High End Graphic Card
- Generic Desktop and Consumer Electronics

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Typical Applications Circuit



Component	Value	Unit	Component	Value	Unit	Component	Value	Unit
C_{VCC}	10	µF	R_{TALERT}	100	kΩ	C3	10	pF
C_{PVCC}	10	µF	R_{TM2}	TBD	kΩ	C4	2.2	nF
C_{VIN1}	300	µF	R_{TM}	TBD	kΩ	C5	1.5	nF
C_{VIN2}	300	µF	R_{HG1}	0	Ω	C_{OUT}	330*3	µF
R_{PG}	100	kΩ	C_{BT1}	100	nF	R_{VOUT}	0	Ω
R_{EN}	100	kΩ	R_{LG1}	Note 4	Ω	R_{VGND}	0	Ω
R_{FS}	33	kΩ	R_{HG2}	0	Ω	C_{REFIN}	0.033	µF
R_{PSI}	100	kΩ	C_{BT2}	100	nF	Q1	–	–
R_{PSI2}	0	kΩ	R1	12	kΩ	Q2	–	–
C_{VREF}	1	µF	R2	2.2	kΩ	Q3	–	–
R_{VREF1}	4.75	kΩ	R3	560	Ω	Q4	–	–
R_{VREF2}	4.22	kΩ	L1	0.36	µH	–	–	–
R_{REFADJ}	6.34	kΩ	L2	0.36	µH	–	–	–

Table 1. Component Guide

Note 4: R_{LG1} are OCP setting resisters:
5k for lower OCP threshold, I_{OCP} = 150mV/$R_{DS(ON)}$
10k for medium OCP threshold, I_{OCP} = 250mV/$R_{DS(ON)}$
>20k for disabling OCP function

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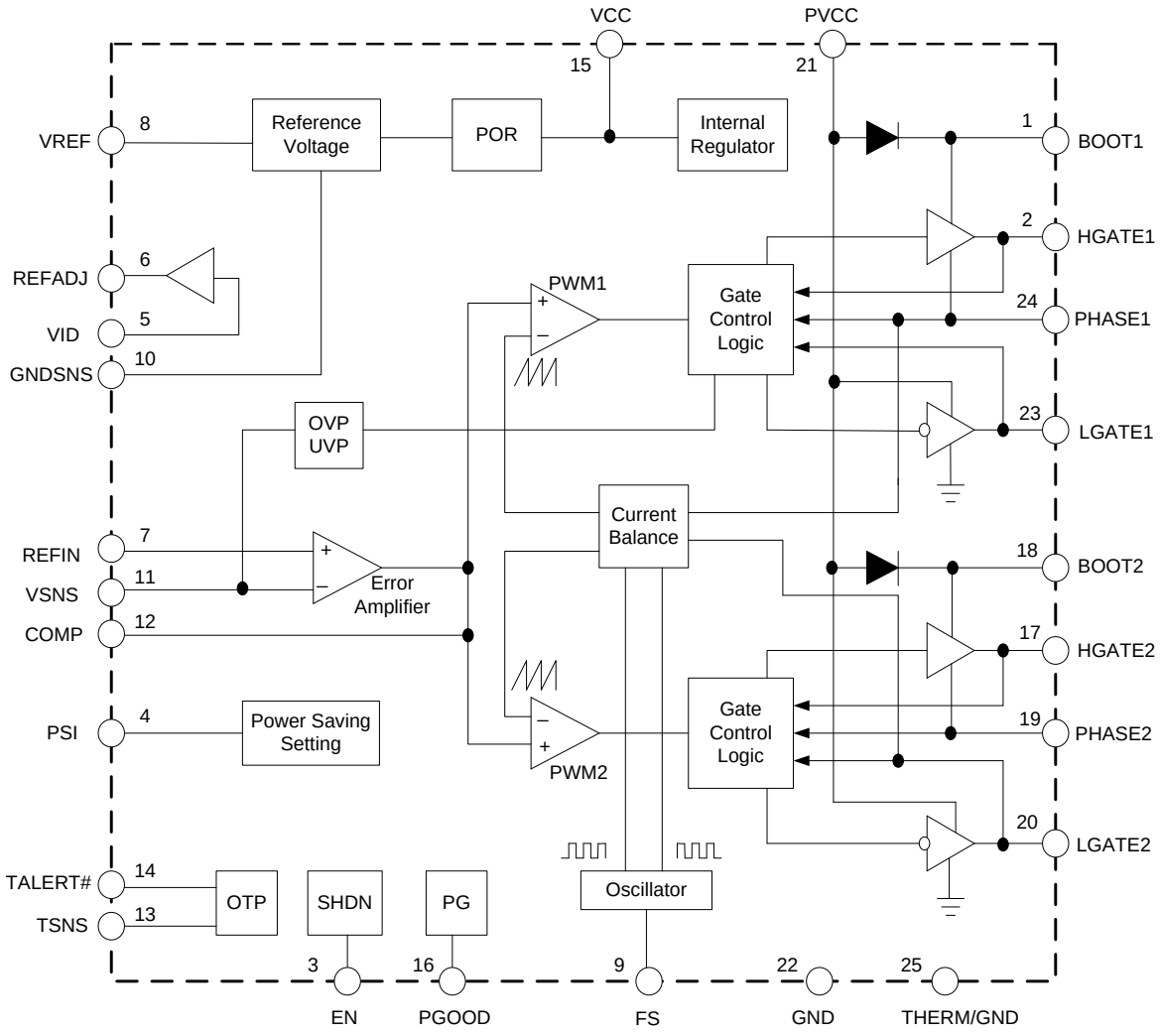
Pin Descriptions

Pin Number	Pin Name	Function
1	BOOT1	High side gate driver supply of phase 1
2	HGATE1	High side gate driver output of phase 1
3	EN	Enable input
4	PSI	Power saving interface
5	VID	Voltage ID input
6	REFADJ	Reference adjustment output
7	REFIN	External reference input
8	VREF	Output reference voltage. This is high precision voltage reference
9	FS	Frequency selection. Connect a resistor from this pin to GND to select the switching frequency
10	GNDSNS	GND sense. Negative node of the remote voltage sense
11	VSNS	V_{OUT} sense. Positive node of the remote differential voltage sense
12	COMP	Compensation. Use this pin in combination with VSNS to compensate the feedback loop of the converter
13	TSNS	Temperature sensing input
14	TALERT#	Thermal alert. Active low open drain output
15	VCC	Supply voltage
16	PGOOD	Open drain power good output
17	HGATE2	High side gate driver output of phase 2
18	BOOT2	High side gate driver supply of phase 2
19	PHASE2	Switch node of phase 2
20	LGATE2	Low side gate driver output of phase 2
21	PVCC	Driver supply voltage
22	GND	Ground. Must be connected to GND on PCB
23	LGATE1	Low side gate driver output of phase 1
24	PHASE1	Switch node of phase 1
25	THERM/GND	Thermal connection to the PCB. Must be connected to GND on PCB

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Functional Block Diagram



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Absolute Maximum Ratings (Note 5)

Symbol	Parameter	Rating		Unit
V_{CC}, V_{PCC}	VCC, PVCC Pin Voltage	-0.3 to 15		V
V_{PHASE1}, V_{PHASE2}	PHASE to GND Voltage	<200ns	-5 to 32	V
		>200ns	-0.3 to 26	
V_{BOOT1_PHASE1}, V_{BOOT2_PHASE2}	BOOT to PHASE Voltage	-0.3 to 15		V
V_{BOOT1}, V_{BOOT2}	BOOT to GND Voltage	<200ns	-0.3 to 42	V
		>200ns	-0.3 to 30	
V_{HGATE1}, V_{HGATE2}	HGATE to PHASE Voltage	<200ns	-5 to V_{BOOT_PHASEx}+5	V
		>200ns	-0.3 to V_{BOOT_PHASEx}+0.3	
V_{LGATE1}, V_{LGATE2}	LGATE to GND Voltage	<200ns	-5 to V_{IN}+5	V
		>200ns	-0.3 to V_{IN}+0.3	
–	Other Input, Output or I/O Pin Voltage	0 to 6		V
θ_{JA}	Thermal Resistance	40		°C/W
P_D	Power Dissipation (T_A = +25°C)	2.5		W
T_J	Operating Junction Temperature Range	-40 to +150		°C
T_{STG}	Storage Temperature	-65 to +150		°C
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260		°C
–	ESD(Machine Model)	200		V
–	ESD(Human Body Model)	2000		V

Note 5: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}, V_{PCC}	Supply Input Voltage	4.5	13.2	V
V_{OUT}	Output Voltage	0.3	2	V
T_A	Operating Ambient Temperature	-40	+85	°C

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Electrical Characteristics (V_{CC} = 12V, V_{PCC} = 12V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
I_{CC}	Supply Current	HGATE and LGATE Open, Switching	–	5	–	mA
I_{CC_Q}	Quiescent Supply Current	No Switching	–	4	–	mA
I_{SHDN}	Shutdown Supply Current	Shutdown	–	4	–	mA
POR						
V_{CCRTH}	Under Voltage Lockout Threshold for VCC	–	3.9	4.1	4.3	V
V_{CCHYS}	Hysteresis for VCC	–	–	0.4	–	V
V_{PCCRTH}	Under Voltage Lockout Threshold for PVCC	–	3.9	4.1	4.3	V
V_{PCCHYS}	Hysteresis for PVCC	–	–	0.4	–	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage Accuracy	I_{REF} = 100μA, T_A = +25°C	1.98	2.00	2.02	V
		I_{REF} = 100μA, T_A = 0 to +150°C	1.97	–	2.03	
ΔV_{REF}	Reference Voltage Load Regulation	I_{REF} = 0 to 2mA	-5	–	5	mV
I_{REF}	VREF Maximum Output Current	–	10	–	–	mA
ERROR AMPLIFIER						
A_O	Open Loop DC Gain	Guaranteed by design	70	80	–	dB
G_{BW}	Gain-Bandwidth Product	C_{LOAD} = 5pF, Guaranteed by design	–	20	–	MHz
SR	Slew Rate	Guaranteed by design	15	20	–	V/μs
I_{COMP}	Maximum Current (Sink and Source)	V_{COMP} = 1.6V	1.5	2.0	–	mA
FREQUENCY SETTING						
V_{FS}	FS Voltage	R_{FS} = 33kΩ	–	1	–	V
–	Switching Frequency Setting Range	–	200	–	500	kHz
f_{OSC}	Free Run Switching Frequency	R_{FS} = 33kΩ	270	300	330	kHz
Δf_{OSC}	Switching Frequency Accuracy	f_{OSC} = 200kHz to 500kHz	-15	–	15	%
OSCILLATOR						
–	Maximum Duty Cycle	–	35	40	–	%
–	Minimum Duty Cycle	–	–	0	–	%
ΔV_{OSC}	Ramp Amplitude	V_{CC} = 12V	–	3.5	–	V
ENABLE FUNCTION						
V_{ENIH}	Enable High Threshold	–	1.4	–	–	V
V_{ENIL}	Enable Low Threshold	–	–	–	0.6	V

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Electrical Characteristics (Cont. V_{CC} = 12V, V_{PCC} = 12V, T_A = +25ºC, unless otherwise specified.)

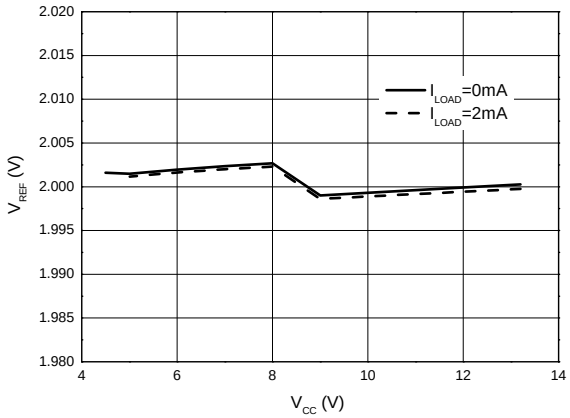
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER SAVING INTERFACE						
V_{PSIH}	Power Saving Interface High Threshold	Dual Phase with FCCM	1.5	–	–	V
V_{PSIL}	Power Saving Interface Low Threshold	Single Phase with DCM	–	–	0.4	V
V_{PSIM}	Power Saving Interface Intermediate Threshold	Single Phase with FCCM	0.8	–	1.1	V
POWER GOOD						
t_{PG_DLY}	Delay Time for PGOOD from High to Low	–	–	10	–	µs
R_{PG}	Internal Power Good Pull Low Resistance	–	–	–	150	Ω
GATE DRIVER						
I_{HG_SRC}	Upper Gate Sourcing Current	V_{BOOTx}-V_{PHASEx} = 6V	–	1.2	–	A
R_{HG_SNK}	Upper Gate Sinking Resistance	V_{UGATEx}-V_{PHASEx} = 0.1V I_{UGATEx} = 100mA	–	2	–	Ω
I_{LG_SRC}	Lower Gate Sourcing Current	V_{CC}-V_{LGATEx} = 6V	–	1.2	–	A
R_{LG_SNK}	Lower Gate Sinking Resistance	V_{LGATEx} = 0.1V I_{LGATEx} = 100mA	–	1.4	–	Ω
V_{BOOT}	Boot Diode Forward Voltage	V_{PCC}-V_{BOOT}, I_{BOOT} = 20mA	–	0.8	–	V
PROTECTION						
V_{UVP}	Output Under Voltage Protection Threshold	–	–	–	0.5* V_{OUT}	V
t_{UVP}	Delay Time for UVP Triggered	–	–	50	–	µs
V_{OVP}	Output Over Voltage Protection Threshold	–	1.4* V_{OUT}	–	–	V
t_{OVP}	Delay Time for OVP Triggered	–	–	50	–	µs
I_{OCSET}	LGATE OC Setting Current	–	–	21.5	–	µA
–	Built-in Maximum OCP Voltage	–	–	0.35	–	V
THERMAL PROTECTION						
T_{SD}	Thermal Shutdown Threshold	–	+150	+160	+170	ºC
$T_{ALERT\#}$	Minimum Thermal Alert Threshold	–	+120	+130	+140	ºC
V_{TSNS}	Temperature Sense Threshold	–	–	1.00	–	V
PWM-VID DYNAMIC VOLTAGE CONTROL						
V_{IH}	Logic High Level	–	1.5	–	–	V
V_{IL}	Logic Low Level	–	–	–	0.4	V
V_{ID}	VID Voltage in High-Z Mode	–	–	1.1	–	V
CURRENT BALANCE						
I_{OFS}	Current Balance Sense Offset	–	–	0	–	µA

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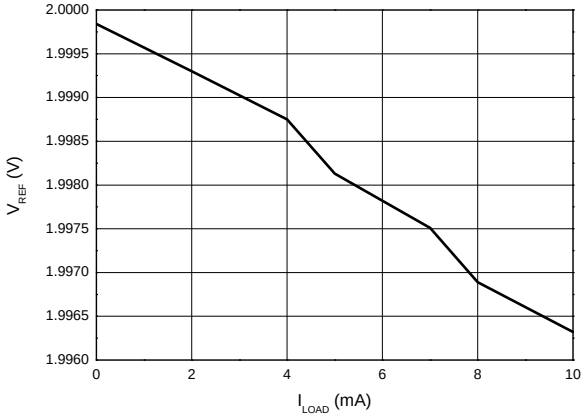
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Performance Characteristics

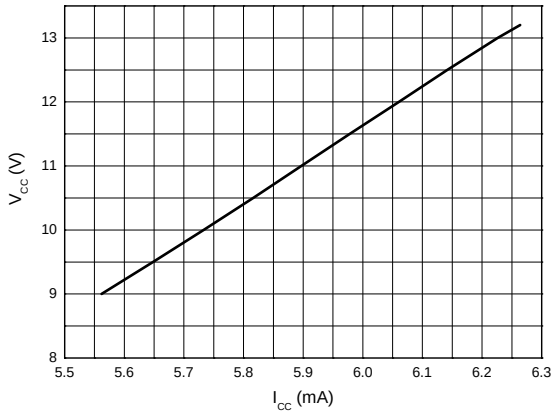
V_{REF} Line Regulation



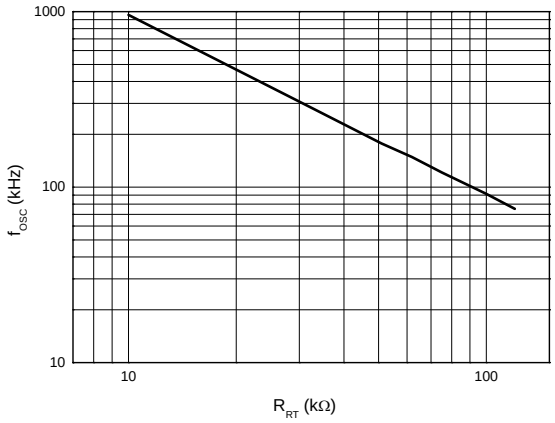
V_{REF} Load Regulation



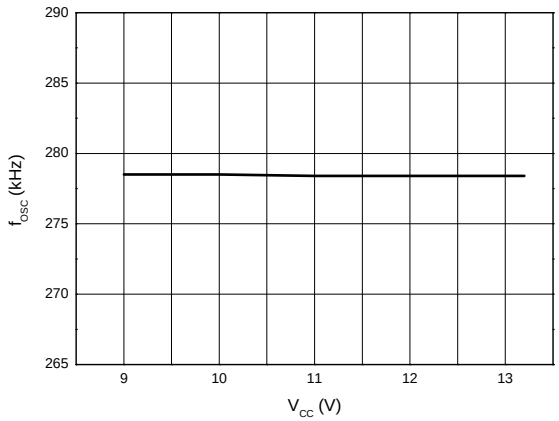
V_{CC} vs. I_{CC}



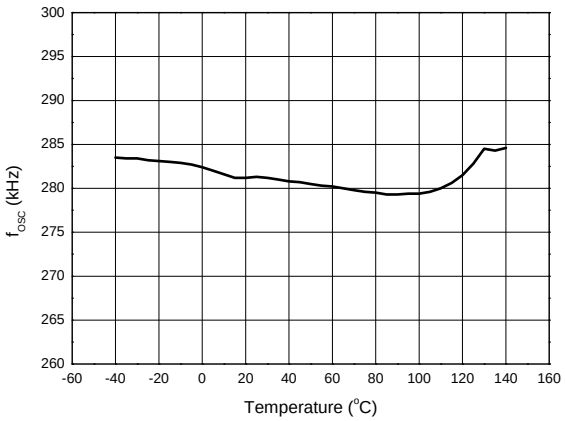
f_{OSC} vs. R_{RT}



f_{OSC} vs. V_{CC}



f_{OSC} vs. Temperature

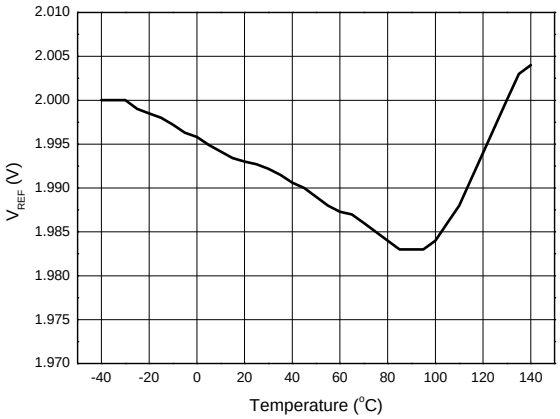


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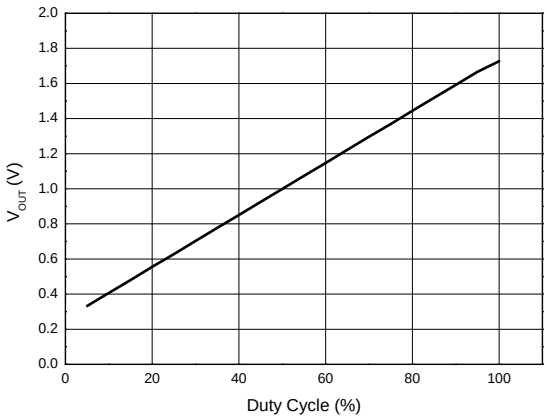
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Performance Characteristics (Cont.)

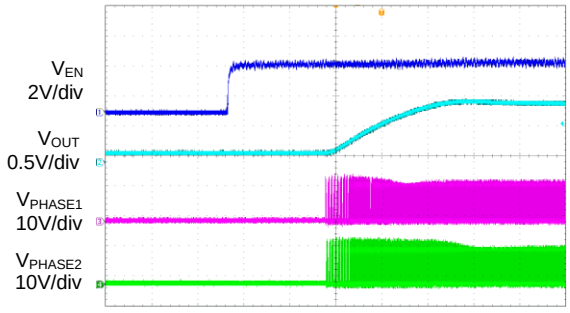
V_{REF} vs. Temperature



V_{OUT} vs. Duty Cycle

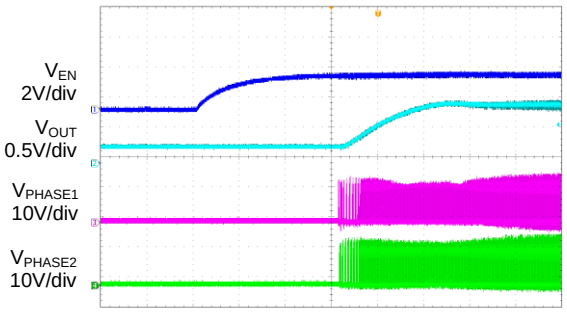


EN On Waveform
(V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=0A)



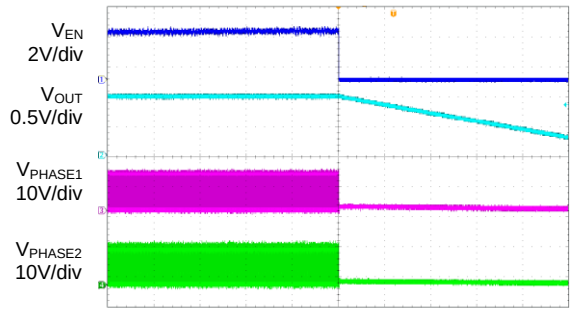
Time 400µs/div

EN On Waveform
(V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=60A)



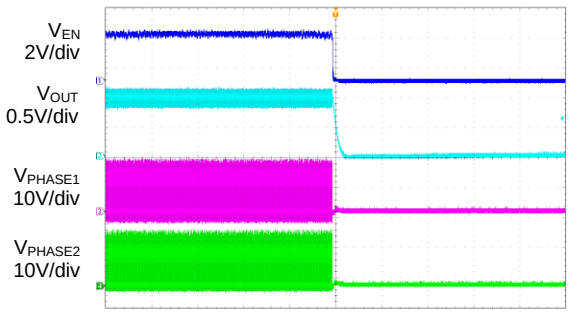
Time 400µs/div

EN Off Waveform
(V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=0A)



Time 400µs/div

EN Off Waveform
(V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=60A)



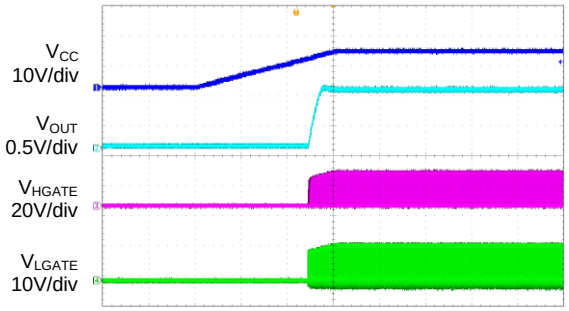
Time 400µs/div

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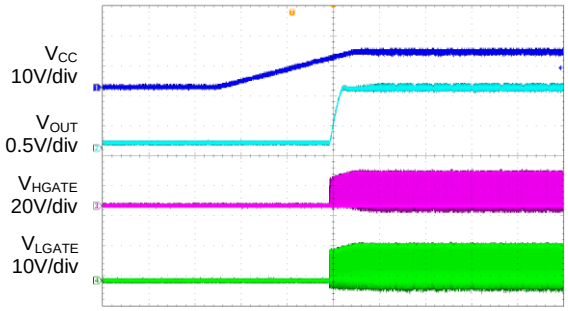
Performance Characteristics (Cont.)

Power On Waveform
(V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=0A)



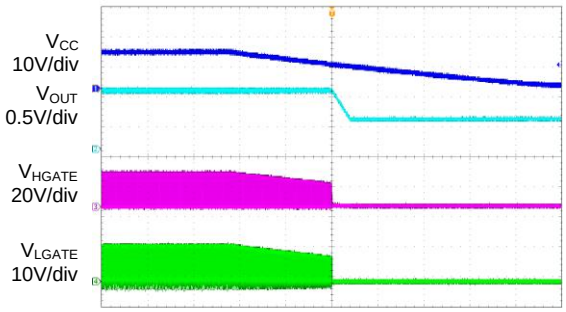
Time 4ms/div

Power On Waveform
(V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=60A)



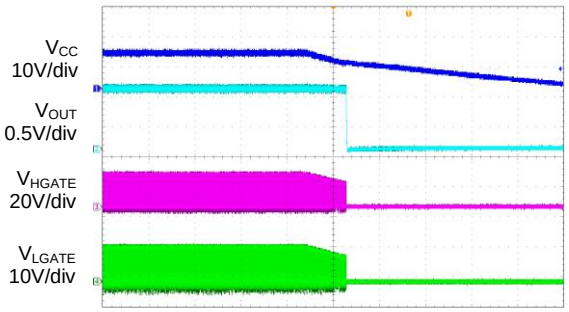
Time 4ms/div

Power Off Waveform
(V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=0A)



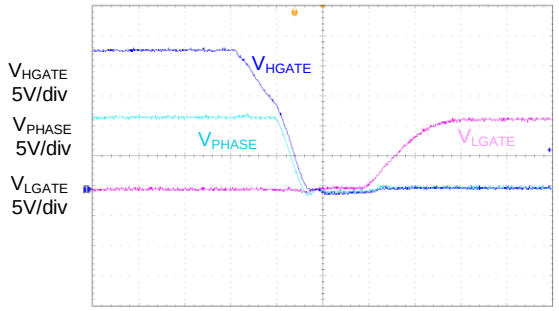
Time 4ms/div

Power Off Waveform
(V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=60A)



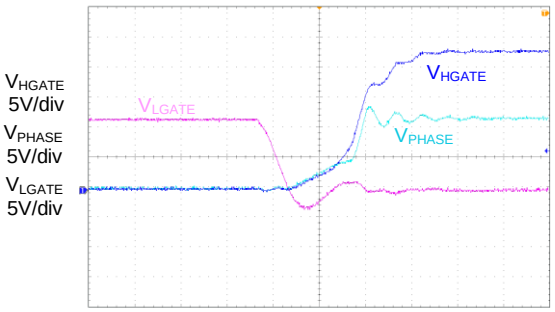
Time 4ms/div

Dead Time 1



Time 40ns/div

Dead Time 2



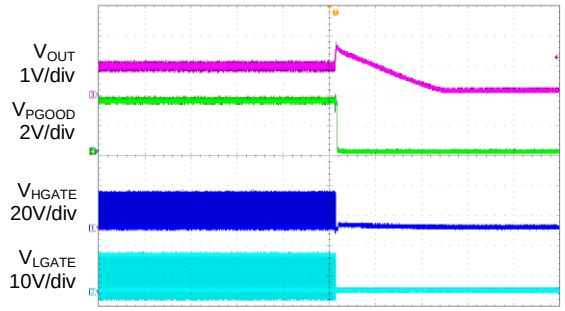
Time 40ns/div

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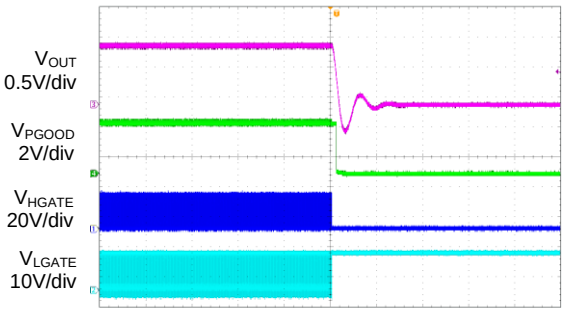
Performance Characteristics (Cont.)

Under Voltage Protection
(V_{IN}=12V, V_{OUT}=1.0V)



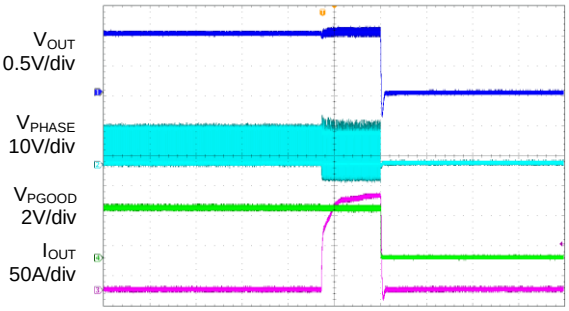
Time 400µs/div

Over Voltage Protection
(V_{IN}=12V, V_{OUT}=1.0V)



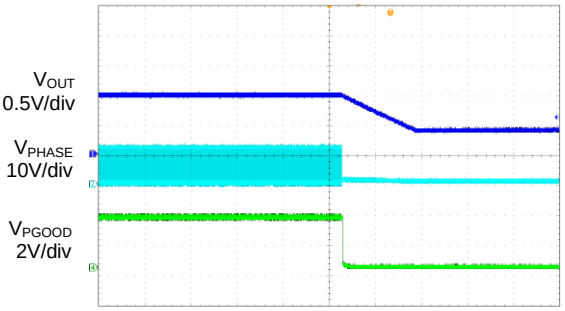
Time 400µs/div

Over Current Protection
(V_{IN}=12V, V_{OUT}=1.0V)



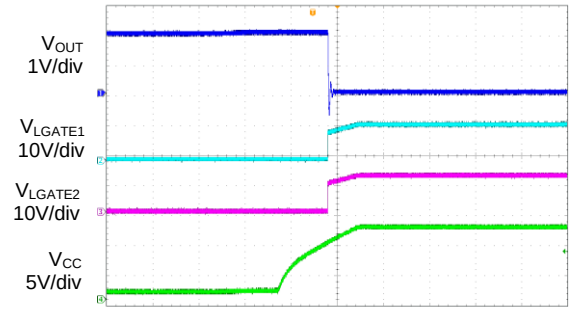
Time 2ms/div

Over Temperature Protection
(V_{IN}=12V, V_{OUT}=1.0V)



Time 400µs/div

Pre-bias Start-up
(V_{IN}=12V, V_{OUT}=2V before Power On)



Time 4ms/div

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Application Information

1. Overview

The AP3598A is a dual-phase synchronous-rectified buck controller designed to deliver high quality output voltage for high power applications. The IC is capable of delivering up to 60A output current with embedded bootstrapped drivers that support 12V+12V driver capability. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to the reference input that is dynamically adjustable by external voltage divider. The adjustable current balance is achieved by $R_{DS(ON)}$ current sensing technique.

The AP3598A features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation frequency, and quick response to step load transient. With aforementioned functions, the AP3598A provides customer a compact, high efficiency, well-protected and cost effective solution. It uses U-QFN4040-24 package.

2. Power On Reset

A Power On Reset (POR) circuitry continuously monitors the supply voltage at VCC and PVCC pin. Once the rising POR threshold is exceeded, the AP3598A sets itself to active state and is ready to accept chip enable command. The rising POR threshold is typically 4.1V.

3. Soft Start

The AP3598A initiates its soft start cycle when EN is released from ground once the POR is granted.

Slew rate of voltage transition at REFIN and output voltage VSNS during soft start and V_{REFIN} jumping is controlled by the capacitor connected to the REFIN pin. This reduces inrush current to charge/discharge the large output capacitors during soft start and VID changing, and prevents OCP, OVP, UVP false trigger.

4. Pre-Bias Function

The AP3598A features pre-bias start-up capability. If the output voltage is pre-biased voltage, which makes VSNS voltage higher than reference voltage REFIN. The error amplifier keeps COMP voltage lower than the valley of the sawtooth waveform and makes PWM comparators output low until the ramping REFIN voltage catches up the output voltage.

The AP3598A keeps both upper and lower MOSFETS off until the first pulse takes place.

5. Chip Oscillator Frequency Programming

A resistor R_{FS} connected to FS pin programs the oscillator frequency as:

$$f_{OSC} = \frac{10000}{R_{FS}(k\Omega)}(kHz)$$

Figure 1 shows the relationship between oscillation frequency and R_{FS}.

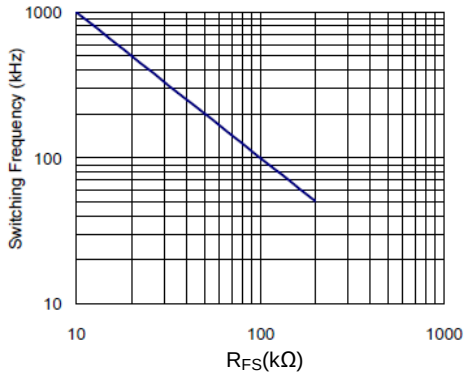


Figure 1. Switching Frequency vs. R_{FS}

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6. Current Balance

The AP3598A extracts phase currents for current balance by parasitic on-resistance of the lower switches when turned on as shown in Figure 2.

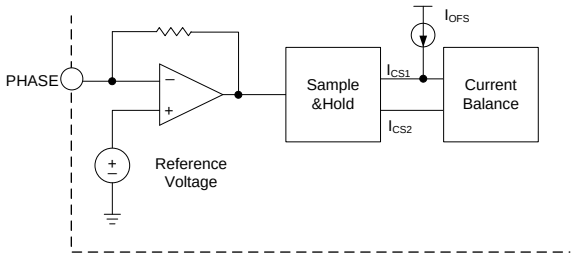


Figure 2. $R_{DS(ON)}$ Current Sensing Scheme

The GM amplifier senses the voltage drop across the lower switch and converts it into current signal when it turns on. The sampled and held current is expressed as:

$$I_{CSX} = I_{LX} \times R_{DS(ON)} \times 10^{-3} + 12\mu A$$

Where I_{LX} is the phase x current in Ampere, $R_{DS(ON)}$ is the on-resistance of low side MOSFET (Ω), 12μA is a constant current to compensate the offset voltage of the current sensing circuit.

The AP3598A tunes the duty cycle of each channel for current balance according to the sensed inductor current signals as shown in Figure 3. If the current of channel 1 is smaller than the current of channel 2, the AP3598A increases the duty cycle of the corresponding phase to increase its phase current accordingly, vice versa.

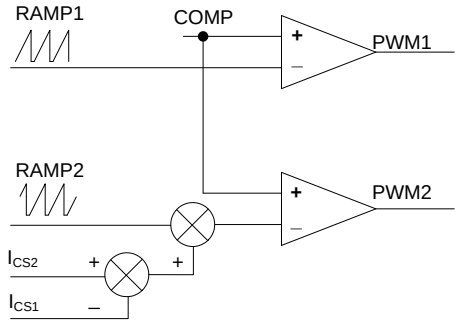


Figure 3. Current Balance Scheme of AP3598A

7. Power Saving Interface (PSI)

This is a multilevel input to support Power Saving features. The AP3598A supports dual phase with FCCM and single phase with DCM and FCCM.

Mode	Descriptions
DCM	Discontinuous Conduction Mode decreases the switching frequency to improve the efficiency at light load
FCCM	Forced Continuous Conduction Mode does not change the switching frequency when the inductor current goes to negative at light load. This mode is used to disable Power Saving features

Table 2. Description of Operating Modes

As shown in Table 2, an input high voltage (>1.5V) will set the controller to dual phase with FCCM mode; an input of intermediate level (between 0.8V and 1.1V) will set the controller to single phase with FCCM mode; an input low voltage will set the controller to single phase with DCM mode.

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8. Short Circuit Protection (SCP)

The AP3598A has over current (OCP) and output under voltage protection (UVP) functions.

8.1 OCP function

The AP3598A detects voltage drop across the lower MOSFET (PHASE voltage) of Channel 1 for over current protection when it is turned on. If PHASE voltage is lower than the user programmable voltage V_{OCP}, the AP3598A asserts OCP and shuts down the converter. The V_{OCP} level is as shown in Table 3. The over current I_{OCP} can be calculated according to the on-resistance of the lower MOSFET used.

$$I_{OCP} = -\frac{V_{OCP}}{R_{DS(ON)}}$$

–	>20kΩ	10kΩ	5kΩ
V_{OCP} (mV)	No OCP	250	150

Table 3. OCP Level Selection

A resistor R_{OCSET} connected from LGATE1 pin sets the OCP threshold value V_{OCSET} when Startup. An internal current source I_{OCSET} (21.5μA typically), flowing through R_{OCSET} determines to select the V_{OCP} level, which can be calculated using the following equation:

$$V_{OCSET} = I_{OCSET} \times R_{OCSET}$$

If V_{OCSET} is lower than 150mV, V_{OCP} will be set to 150mV; If V_{OCSET} is between 350mV and 150mV, V_{OCP} will be set to 250mV; If V_{OCSET} is higher than 350mV, V_{OCP} will be disabled.

Because the $R_{DS(ON)}$ of MOSFET increases with temperature, it is necessary to take this thermal effect into consideration in calculating OCP point.

8.2 UVP Function

The output voltage V_{SNS} is also monitored for under voltage protection. The UV threshold is set at 0.3V. The under voltage protection has 50μs triggered delay. When UVP is triggered, both high side and low side are shutdown immediately.

OCP and UVP are latched function, the AP3598A can power off, and then power on or EN reset to restart again.

9. Over Voltage Protection (OVP)

The output voltage V_{SNS} is continuously monitored for over voltage protection. When it is larger than 1.5 times as setting, the OVP function is triggered. The over voltage protection has 50μs triggered delay. When OVP is triggered, LGATE will go high and UGATE will go low to discharge the output capacitor.

10. Power Good

The PGOOD pin output is an open drain MOSFET. The output is pulled low when the AP3598A shuts down. It is recommended to use a pull-up resistor between the values of 3kΩ and 100kΩ to a voltage source that is 5V or less. The PGOOD is in a valid state once the V_{CC} voltage is greater than 1.2V.

11. Thermal Shutdown

The AP3598A implements an internal thermal shutdown to protect itself if the junction temperature exceeds T_J.

TSNS is the external thermistor temperature sensing input.

TALERT# is an active low open drain output warning signal to indicate when either the controller has reached 80% percent of T_{JMAX} or MOSFET has reached its threshold through the external thermistor.

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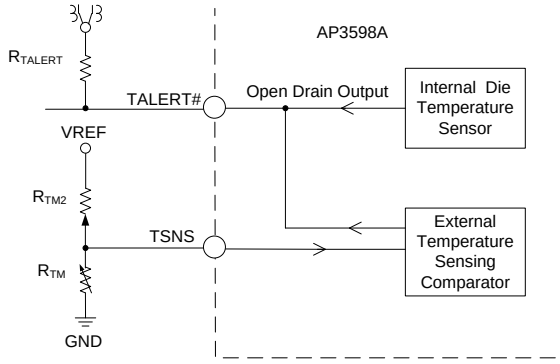


Figure 4. Thermal Alert and Temperature Sense

12. PWM-VID Dynamic Voltage Control

PWM-VID is a single-wire dynamic voltage control circuit driven by the pulse width modulation method. This circuit reduces the device pin count and enables a wide dynamic voltage range.

The PWM-VID duty cycle determines the variable output voltage at REFIN, as shown in Figure 5. V_{MIN} is the zero percent duty cycle voltage value. V_{MAX} is the one hundred percent duty cycle voltage value. The resolution of each voltage step (V_{STEP}) is determined by the number of available steps (N_{MAX}) and the selection of the dynamic voltage range (V_{MAX}-V_{MIN}). N is the number of steps at a specific V_{OUT}. N/N_{MAX} ratio is equal to the duty cycle. The dynamic voltage VID frequency (f_{SWVID}) is determined by the unit pulse width (t_U) and the available step number N_{MAX} (t_{VID} = t_U*N_{MAX}, f_{VID} = 1/ t_{VID}). t_U is programmable.

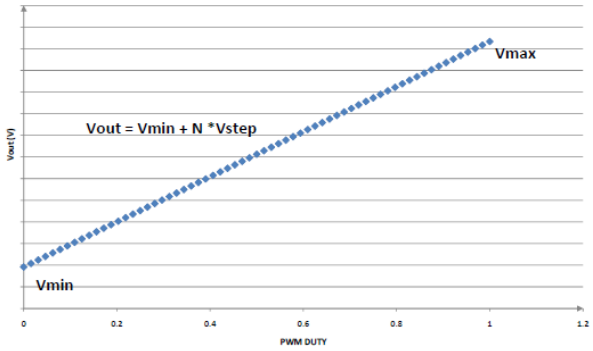


Figure 5. Dynamic Output

V_{STEP}, N_{MAX}, V_{MIN}, and V_{MAX} are variables that determine V_{OUT}. N_{MAX} is limited by the unit pulse width and the minimum VID frequency.

The dynamic voltage output could be implemented by the analog method with a switching device and a resistor network. A buffer is used as the switching device to create dynamic output. Resistor network sets the minimum offset voltage.

12.1 Circuit Diagram

Figure 6 shows the analog circuit diagram for the PWM-VID dynamic voltage control. The buffer requires a stable, high precision voltage reference (V_{REF}) for the linear output. The dynamic range of the circuit is determined by the resistor selection. Resistor R_{REFADJ} and capacitor C_{REFIN} function as a filter for the PWM signal, and will affect the ripple voltage and the slew rate at the output (REFIN) during voltage transitions.

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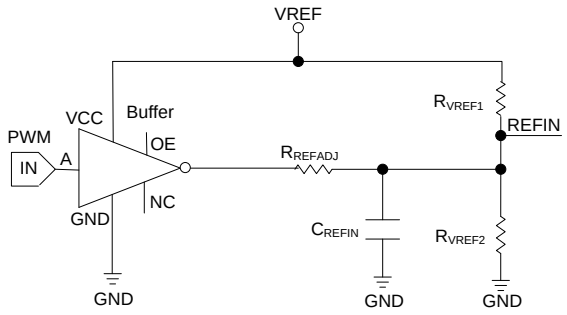


Figure 6. PWM-VID Analog Circuit Diagram

Spec Description	Output Voltage Equation
N_{MAX}: Total available voltage step number	–
N: The step number of the specific V_{OUT}, N/N_{MAX} ratio equals duty cycle	–
V_{MAX}: The output voltage of REFIN at one hundred percent duty cycle	$V_{REF} \times \frac{R_{VREF2}}{R_{VREF2} + (R_{VREF1} \parallel R_{REFADJ})}$
V_{MIN}: The output voltage of REFIN at zero percent duty cycle	$V_{REF} \times \frac{R_{VREF2} \parallel R_{REFADJ}}{R_{VREF1} + (R_{VREF2} \parallel R_{REFADJ})}$
V_{STEP}: The resolution of the voltage step	$\frac{V_{MAX} - V_{MIN}}{N_{MAX}}$
V_{OUT}: The output voltage at REFIN	$V_{MIN} + N \times V_{STEP}$
f_{SWVID}: The dynamic voltage VID frequency	$\frac{1}{t_U \times N_{MAX}}$

Table 4. REFIN Dynamic Range

There will be some ripple voltage at REFIN due to the nature of the PWM and filter. The error amplifier at REFIN will be able to tolerate a reasonable amount of Ripple Voltage.

12.2 Integrating the Buffer

Figure 7 shows a dynamic voltage control circuit with the integrated buffer. This defines the implementation of the VID and REFADJ functions.

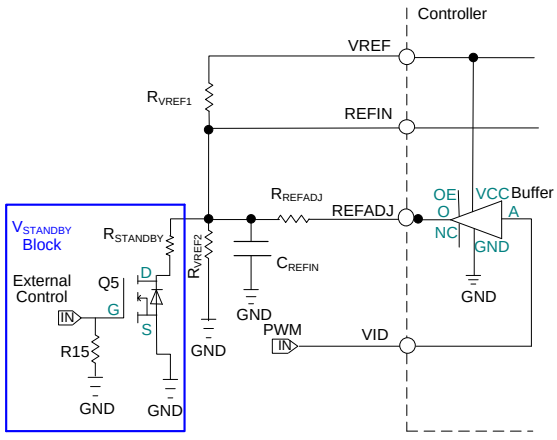


Figure 7. Integrated Buffer Circuit

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12.3 Timing Diagram

Figure 8 contains the details of the timing diagram. After VCC powers up, the controller generates the V_{REF}. REFIN settles at V_{BOOT} before the GPU drives the VID pin. After the GPU powers up, V_{BOOT} control will be pulled low by software. At the same time the VID is driven by a PWM signal, moving REFIN into the normal operating mode. When the GPU is going to standby, software will tri-state VID and V_{BOOT} control, and an external control will enable $R_{STANDBY}$.

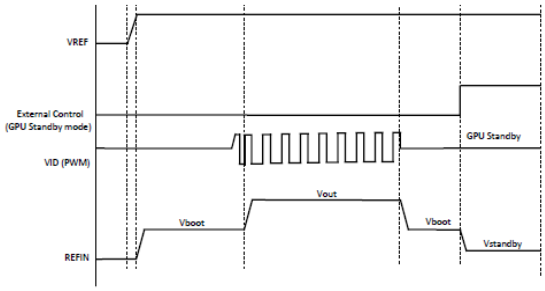


Figure 8. Time Diagram

12.4 Standby Mode

Standby mode keeps the GPU in a low voltage state (in the range of 0.3V) for the quick recovery. As the GPU steps into the standby mode, the resistor $R_{STANDBY}$ and the switch Q6 (parallel to the R_{VREF2} and R_{BOOT}) set the standby voltage. The accuracy of the reference voltage in the standby mode could be reduced from the normal operating mode. Refer to Figure 9 for the illustration of the standby voltage.

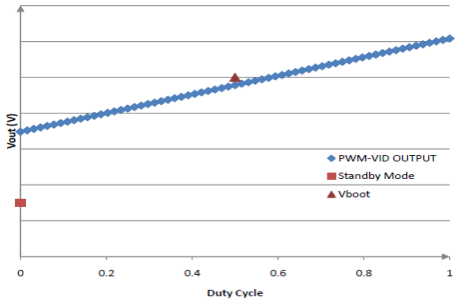


Figure 9. Illustration for Standby Mode and Adjustable V_{BOOT} Setting

12.5 Voltage Waveform and Propagation Delay

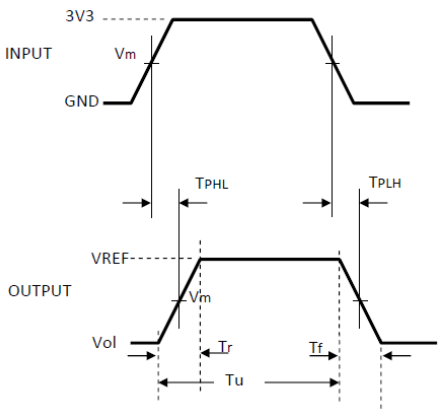


Figure 10. The Behavior of the Buffer

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12.6 Electrical Characteristics

Parameters	Sym	Min	Typ	Max	Unit	Notes
Buffer Supply Voltage	–	–	V_{REF}	–	V	–
Unit Pulse Width	t_U	–	27	–	ns	Configurable
Buffer Output Rise Time	t_R	–	5	–	ns	–
Buffer Output Fall Time	t_F	–	5	–	ns	–
Rising and Falling Edge Delay	Δt	–	–	0.5	ns	$\Delta t=\lvert t_R-t_F\rvert$
Propagation Delay	t_{PD}	–	10	–	ns	$t_{PD}=t_{PHL}=t_{PLH}$
Propagation Delay Error	Δt_{PD}	–	–	0.5	ns	$\Delta t_{PD}=t_{PHL}-t_{PLH}$
Upper Resister	R_{VREF1}	–	4.75	–	kΩ	–
Lower Resister	R_{VREF2}	–	4.22	–	kΩ	–
Filter Resister	R_{REFADJ}	–	6.34	–	kΩ	–
Boot Mode Resister	R_{BOOT}	–	–	–	kΩ	Project Specific
Standby Mode Resister	$R_{STANDBY}$	–	1.07	–	kΩ	–
Filter Capacitor	C_{REFIN}	–	0.033	–	μF	–

13. PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, VSNS, and V_{OUT} should be added. The compensation network is shown in Figure 14. The output LC filters consist of the output inductors and output capacitors. For two-phase convertor, when assuming that $V_{IN1} = V_{IN2} = V_{IN}$, L1 = L2 = L, the transfer function of the LC filter is given by:

$$Gain_{LC} = \frac{1 + s \times R_{ESR} \times C_{OUT}}{s^2 \times (1/2) L \times C_{OUT} + s \times R_{ESR} \times C_{OUT} + 1}$$

The poles and zero of the transfer functions are:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{(1/2) L \times C_{OUT}}}$$

$$f_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

The f_{LC} is the double-pole frequency of the two-phase LC filters, and f_{ESR} is the frequency of the zero introduced by the ESR of the output capacitors.

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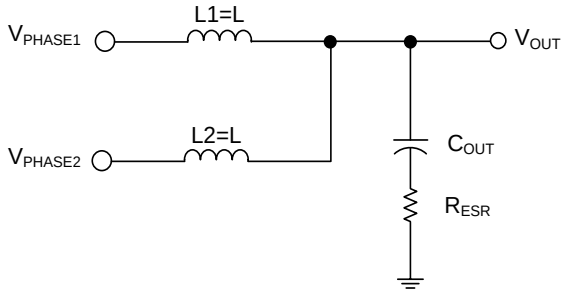


Figure 11. The Output LC Filter

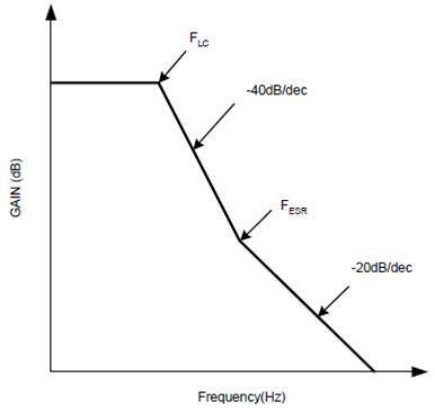


Figure 12. Frequency Response of the LC Filters

The PWM modulator is shown in Figure 13. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$Gain_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

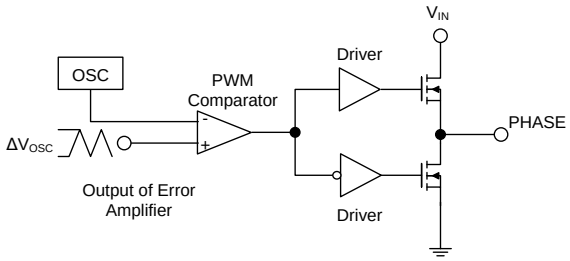


Figure 13. The PWM Modulator

The compensation network is shown in Figure 14. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

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$$Gain_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1} // (R2 + \frac{1}{sC2})}{R1 // (R3 + \frac{1}{sC3})} = \frac{R1 + R3}{R1 \times R3 \times C1} \times \frac{(s + \frac{1}{R2 \times C2}) \times \{s + \frac{1}{(R1 + R3) \times C3}\}}{s(s + \frac{C1 + C2}{R2 \times C1 \times C2}) \times (s + \frac{1}{R3 \times C3})}$$

The pole and zero frequencies of the transfer function are:

$$f_{Z1} = \frac{1}{2 \times \pi \times R2 \times C2}$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C3}$$

$$f_{P1} = \frac{1}{2 \times \pi \times R2 \times (\frac{C1 \times C2}{C1 + C2})}$$

$$f_{P2} = \frac{1}{2 \times \pi \times R3 \times C3}$$

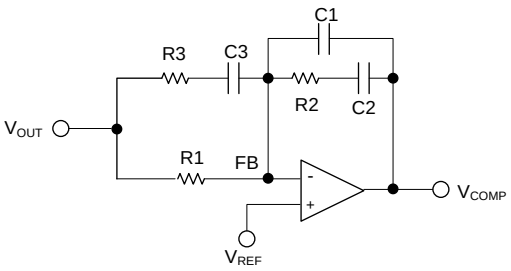


Figure 14. Compensation Network

The closed loop gain of the converter can be written as:

$$Gain_{LC} \times Gain_{PWM} \times Gain_{AMP}$$

Figure 15 shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines will give a compensation similar to the curve plotted. A stable closed loop has a -20dB/decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1kΩ and 5kΩ.

2. Select the desired zero crossover frequency.

$$f_O = (1/5 \sim 1/10) \times f_{SW}$$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{f_O}{f_{LC}} \times R1$$

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3. Place the first zero f_{Z1} before the output LC filter double pole frequency f_{LC}.

$$f_{Z1} = 0.75 \times f_{LC}$$

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times f_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency f_{ESR}:

$$f_{P1} = f_{ESR}$$

Calculate the C1 by the following equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times f_{ESR} - 1}$$

5. Set the second pole f_{P2} at the half of the switching frequency and also set the second zero f_{Z2} at the output LC filter double pole f_{LC}. The compensation gain should not exceed the error amplifier open loop gain. Check the compensation gain at f_{P2} with the capabilities of the error amplifier.

$$f_{P2} = 0.5 \times f_{SW}$$
$$f_{Z2} = f_{LC}$$

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{f_{SW}}{2 \times f_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times f_{SW}}$$

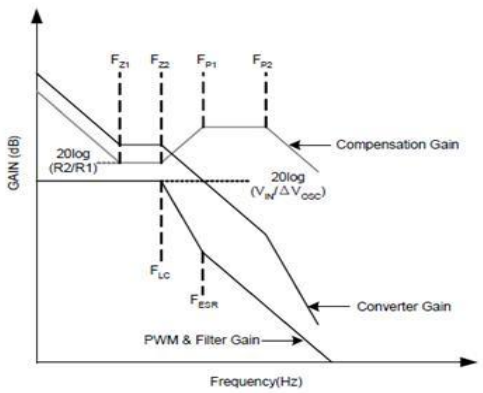


Figure 15. Converter Gain and Frequency

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14. Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = V_{OUT} / V_{IN}$$

For two-phase converter, the inductor value (L) determines the sum of the two inductor ripple current, ΔI_{P-P}, and affects the load transient response. Higher inductor value reduces the output capacitors' ripple current and induces lower output ripple voltage. The ripple current can be approximated by:

$$\Delta I_{P-P} = \frac{V_{IN} - 2V_{OUT}}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where f_{SW} is the switching frequency of the regulator.

Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (f_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

15. Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must be considered too.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change.

For getting same load transient response, the output capacitance of two-phase converter only needs to be around half of output capacitance of single-phase converter.

Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

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16. Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. For two-phase converter, the RMS current of the bulk input capacitor is roughly calculated as the following equation:

$$I_{RMS} = \frac{I_{OUT}}{2} \times \sqrt{2D \times (1-2D)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount design, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.

17. MOSFET Selection

The AP3598A requires two N-Channel power MOSFETs on each phase. These should be selected based upon $R_{DS(ON)}$, gate supply requirements and thermal management requirements.

In high current applications, the MOSFET power dissipation, package selection, and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss.

The conduction losses are the largest component of power dissipation for both the high-side and the low-side MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the high-side MOSFET has switching losses since the low-side MOSFETs body diode or an external Schottky rectifier across the lower MOSFET clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage current transitions and do not adequately model power loss due to the reverse-recovery of the low-side MOSFET body diode. The gate-charge losses are dissipated by AP3598A and don't heat the MOSFETs. However, large gate-charge increases the switching interval t_{SW}, which increases the high-side MOSFET switching losses. Ensure that all MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$P_{HIGH\text{-}SIDE} = I_{OUT}^2 \times (1+T_C) \times R_{DS(ON)} \times D + 0.5 \times I_{OUT} \times V_{IN} \times t_{SW} \times f_{SW}$

$P_{LOW\text{-}SIDE} = I_{OUT}^2 \times (1+T_C) \times (R_{DS(ON)}) \times (1-D)$

Where I_{OUT} is the load current, T_C is the temperature dependency of $R_{DS(ON)}$, f_{SW} is the switching frequency, t_{SW} is the switching interval, D is the duty cycle.

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The $(1+T_C)$ term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

18. Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator.

With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike.

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Application Information (Cont.)

Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Figure 16 illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed close together. Below is a checklist for your layout:

1. Keep the switching nodes (HGATEx, LGATEx, BOOTx, and PHASEx) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.

2. The signals going through theses traces have both high dv/dt and high dI/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (HGATEx and LGATEx) should be short and wide.

3. Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and PHASEx nodes) can get better heat sinking.

4. For experiment result of accurate current sensing, the current sensing components are suggested to place close to the inductor part. To avoid the noise interference, the current sensing trace should be away from the noisy switching nodes.

5. Decoupling capacitors, the resistor-divider, and the boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor as close as possible to the drain of the high-side MOSFET). The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads.

6. The input capacitor's ground should be close to the grounds of the output capacitors and the low-side MOSFET.

7. Locate the resistor-divider close to the VREF and REFIN pins to minimize the high impedance trace. In addition, VSNS pin traces can't be close to the switching signal traces (HGATEx, LGATEx, BOOTx, and PHASEx).

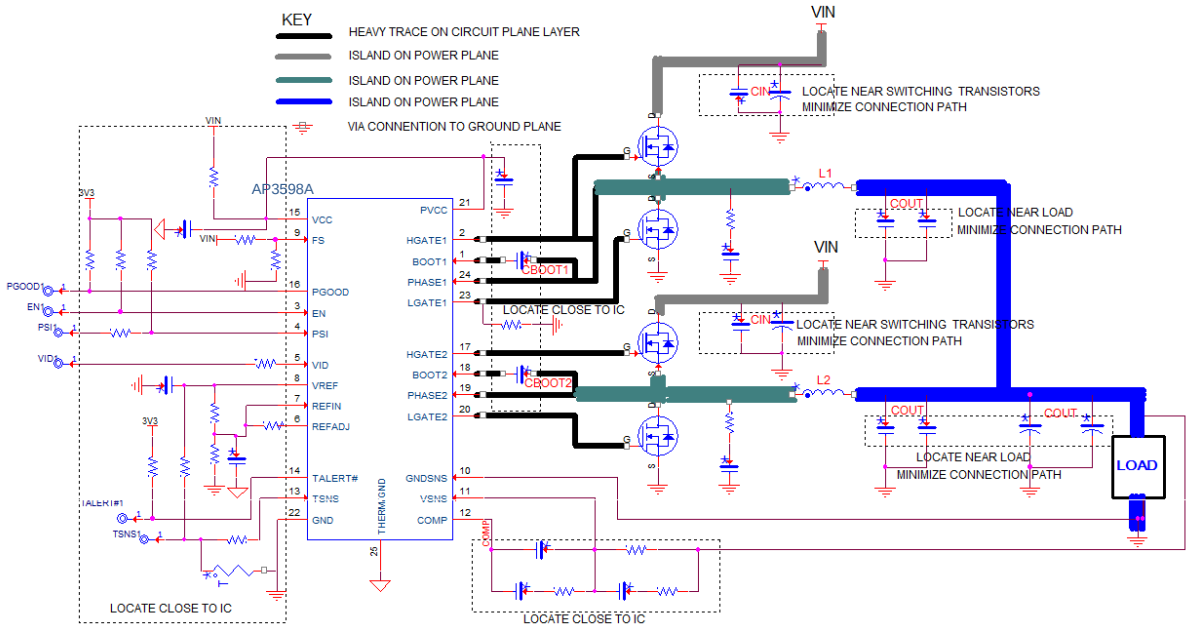
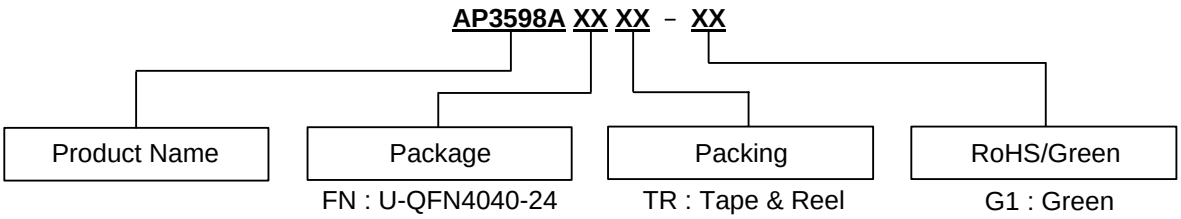


Figure 16. The Layout of AP3598A

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Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing
U-QFN4040-24	-40 to +85°C	AP3598AFNTR-G1	B3F	5000/Tape & Reel

Marking Information

(Top View)



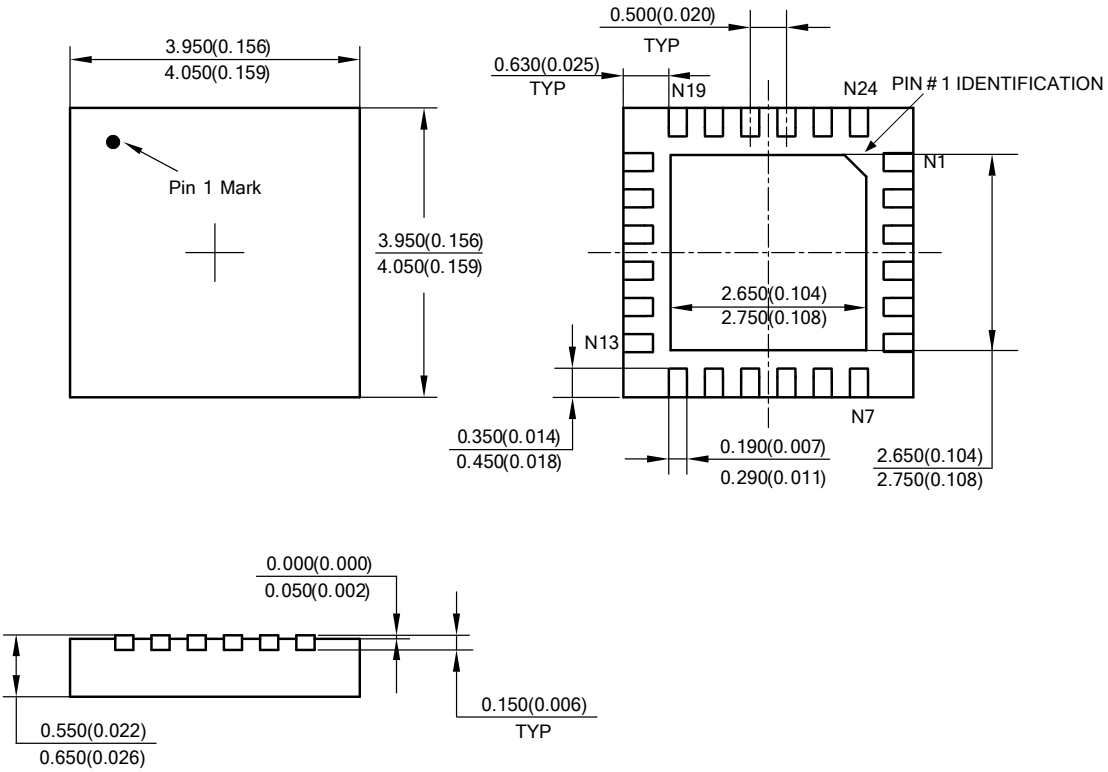
First Line: Logo and Marking ID
Second and Third Lines: Date Code
Y: Year
WW: Work Week of Molding
M: Assembly House Code
XX: 7th and 8th Digits of Batch No.

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Package Outline Dimensions (All dimensions in mm(inch).)

(1) Package Type: U-QFN4040-24 (Type B)

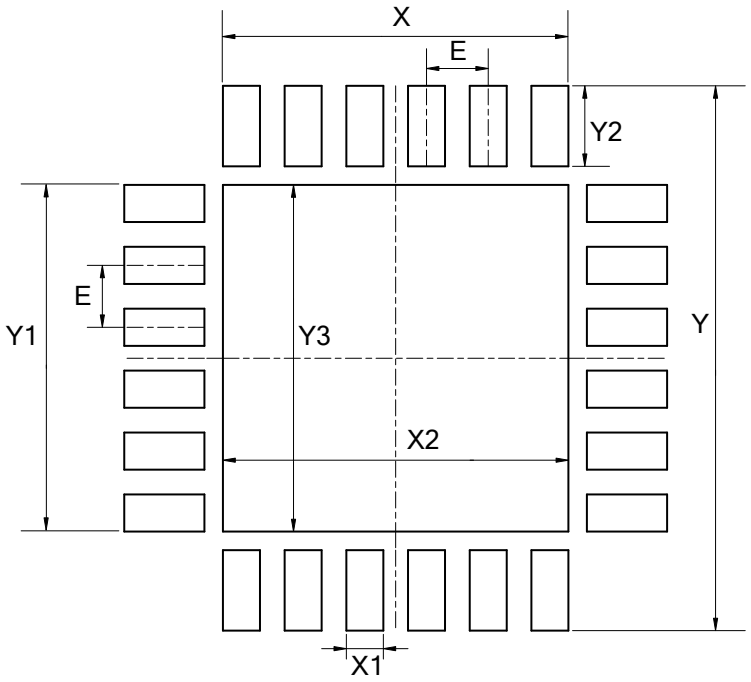


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Suggested Pad Layout

(1) Package Type: U-QFN4040-24 (Type B)



Dimensions	X=Y1 (mm)/(inch)	Y (mm)/(inch)	X1 (mm)/(inch)	Y2 (mm)/(inch)
Value	2.840/0.112	4.300/0.169	0.340/0.013	0.600/0.024
Dimensions	X2=Y3 (mm)/(inch)	E (mm)/(inch)	–	–
Value	2.800/0.110	0.500/0.020	–	–

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