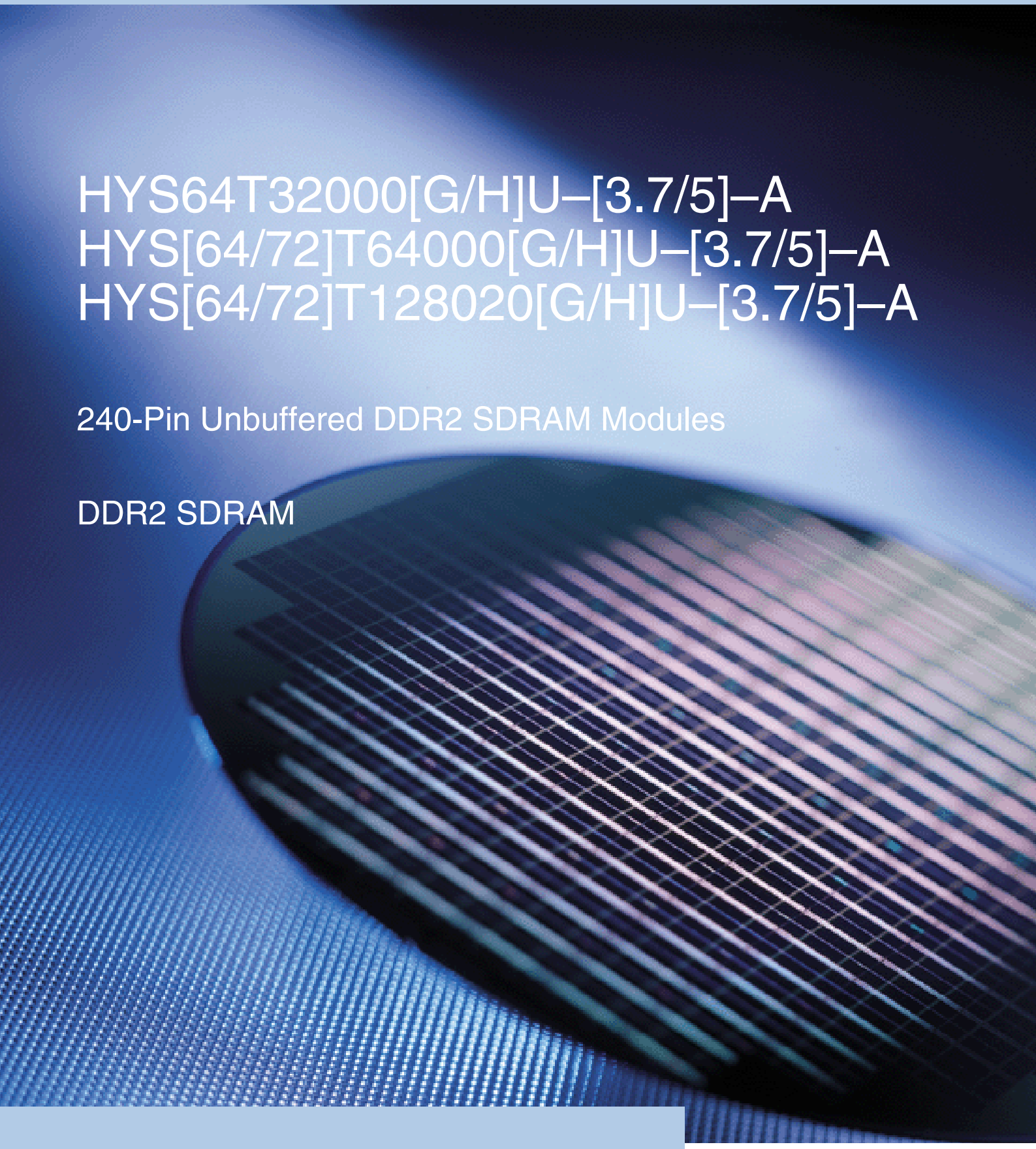
HYS64T32000[G/H]U–[3.7/5]–A
HYS[64/72]T64000[G/H]U–[3.7/5]–A
HYS[64/72]T128020[G/H]U–[3.7/5]–A

240-Pin Unbuffered DDR2 SDRAM Modules

DDR2 SDRAM



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HYS64T32000[G/H]U–[3.7/5]–A
HYS[64/72]T64000[G/H]U–[3.7/5]–A
HYS[64/72]T128020[G/H]U–[3.7/5]–A

240-Pin Unbuffered DDR2 SDRAM Modules

DDR2 SDRAM

Memory Products

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Page	Subjects (major changes since last revision)
all	New template
chapter 5	add currents
all	updated timings

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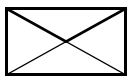

Table of Contents

1 Overview

This chapter gives an overview of the 1.8 V 240-pin Unbuffered DDR2 SDRAM Modules, 256 MByte, 512 MByte & 1 GByte ECC and non-ECC Modules and describes its main characteristics.

1.1 Features

- 240-pin ECC and Non-ECC Unbuffered 8-Byte Dual-In-Line DDR2 SDRAM Module for PC, Workstation and Server main memory applications
- One rank 32M x 64, 64M x 64, 64M x 72 and two ranks 128M × 64 and 128M x 72 organization
- JEDEC standard Double Data Rate 2 Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- 256 ,512 MByte and 1GByte modules built with 512Mb DDR2 SDRAMs in 60-ball (P–TFBGA–60) and 84-ball FBGA (P–TFBGA–84) chipsize packages
- Programmable $\overline{\text{CAS}}$ Latencies (3, 4 & 5), Burst Length (8 & 4) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor: 133.35 mm x 30,00 mm (MO-237)
- Based on JEDEC standard reference card layouts Raw Card “A”, “B” & “C”

Table 1 Performance

Speed Grade Indicator	–5	–-3.7	Unit
Component Speed Grade	DDR2–400	DDR2–533	—
Module Speed Grade	PC2–3200	PC2–4200	—
Max. Clock Frequency @ CL = 3	200	200	MHz
Max. Clock Frequency @ CL = 4 & 5	200	266	MHz

1.2 Description

The INFINEON HYS[64/72]Txxxx0[G/H]U module family are low profile Unbuffered DIMM modules with 30,0 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 32M x 64 (256MB), 64M x 64 (512MB) and 128M x 64 (1024MB) and as ECC-modules in 64M x 72 (512MB) and 128M x 72 (1024MB) organisation and density, intended for mounting into 240 pin connector sockets.

The memory array is designed with 512Mb Double Data Rate (DDR2) Synchronous DRAMs for ECC and Non-ECC applications. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Table 2 Ordering Information

Product Type	Compliance Code	Description	SDRAM Technology
PC2-3200			
HYS64T32000GU–5–A	256MB 1R×16 PC2–3200U–333–11–C0	1 Rank, Non-ECC	512 Mbit (×16)
HYS64T64000GU–5–A	512MB 1R×8 PC2–3200U–333–11–A0	1 Rank, Non-ECC	512 Mbit (×8)
HYS72T64000GU–5–A	512MB 1R×8 PC2–3200E–333–11–A0	1 Rank, ECC	512 Mbit (×8)
HYS64T128020GU–5–A	1GB 2R×8 PC2–3200U–333–11–B0	2 Ranks, Non-ECC	512 Mbit (×8
HYS72T128020GU–5–A	1GB 2R×8 PC2–3200E–333–11–B0	2 Ranks, ECC	512 Mbit (×8)
			green Product
HYS64T32000HU–5–A	256MB 1R×16 PC2–3200U–333–11–C0	1 rank, Non-ECC	512 Mbit (×16)
HYS64T64000HU–5–A	512MB 1R×8 PC2–3200U–333–11–A0	1 rank, Non-ECC	512 Mbit (×8)
HYS72T64000HU–5–A	512MB 1R×8 PC2–3200E–333–11–A0	1 rank, ECC	512 Mbit (×8)
HYS64T128020HU–5–A	1GB 2R×8 PC2–3200U–333–11–B0	2 ranks, Non-ECC	512 Mbit (×8)
HYS72T128020HU–5–A	1GB 2R×8 PC2–3200E–333–11–B0	2 ranks, ECC	512 Mbit (×8)
PC2–4200			
HYS64T32000GU–3.7–A	256MB 1R×16 PC2–4200U–444–11–C0	1 rank, Non-ECC	512 Mbit (×16)
HYS64T64000GU–3.7–A	512MB 1R×8 PC2–4200U–444–11–A0	1 rank, Non-ECC	512 Mbit (×8)
HYS72T64000GU–3.7–A	512MB 1R×8 PC2–4200E–444–11–A0	1 rank, ECC	512 Mbit (×8)
HYS64T128020GU–3.7–A	1GB 2R×8 PC2–4200U–444–11–B0	2 ranks, Non-ECC	512 Mbit (×8
HYS72T128020GU–3.7–A	1GB 2R×8 PC2–4200E–444–11–B0	2 ranks, ECC	512 Mbit (×8)
			green Product
HYS64T32000HU–3.7–A	256MB 1R×16 PC2–4200U–444–11–C0	1 rank, Non-ECC	512 Mbit (×16)
HYS72T64000HU–3.7–A	512MB 1R×8 PC2–4200E–444–11–A0	1 rank, ECC	512 Mbit (×8)
HYS64T64000HU–3.7–A	512MB 1R×8 PC2–4200U–444–11–A0	1 rank, Non-ECC	512 Mbit (×8)
HYS64T128020HU–3.7–A	1GB 2R×8 PC2–4200U–444–11–B0	2 ranks, Non-ECC	512 Mbit (×8)
HYS72T128020HU–3.7–A	1GB 2R×8 PC2–4200E–444–11–B0	2 ranks, ECC	512 Mbit (×8)

Note:

1. *All part numbers end with a place code, designating the silicon die revision. Example: HYS72T64000GU–5-A, indicating Rev. A dice are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see section 8 of this datasheet.*
2. *The Compliance Code is printed on the module label and describes the speed grade, f.e. “PC2-4200U-44410-C”, where 4200U means Unbuffered DIMM modules with 4.26 GB/sec Module Bandwidth and “44410” means CAS latency = 4, trcd latency = 4 and trp latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card “C”.*

Table 3 Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/columns bits	Raw Card
256 MB	32M ×64	1	Non-ECC	4	13/2/10	C
512 MB	64M ×64	1	Non-ECC	8	14/2/10	A
512 MB	64M ×72	1	ECC	9	14/2/10	A
1 GB	2 × 64M ×72	2	Non-ECC	16	14/2/10	B
1 GB	2 × 64M ×72	2	ECC	18	14/2/10	B

Table 4 Components on Modules[1)]

Part Number	DIMM Density	DRAM components reference datasheet	DRAM Density	DRAM Organisation
HYS64T32000GU	256 MB	HYB18T512160AC	512 Mbit	32M ×16
HYS64T32000HU[2)]	256 MB	HYB18T512160AF[2)]	512 Mbit	32M ×16
HYS64T64000GU	512 MB	HYB18T512800AC	512 Mbit	64Mb ×8
HYS64T64000HU[2)]	512 MB	HYB18T512800AF[2)]	512 Mbit	64Mb ×8
HYS72T64000GU	512 MB	HYB18T512800AC	512 Mbit	64Mb ×8
HYS72T64000HU[2)]	512 MB	HYB18T512800AF[2)]	512 Mbit	64Mb ×8
HYS64T128020GU	1 GB	HYB18T1G800AC	512 Mbit	64Mb ×8
HYS64T128020HU[2)]	1 GB	HYB18T1G800AF[2)]	512 Mbit	64Mb ×8
HYS72T128020GU	1 GB	HYB18T1G800AC	512 Mbit	64Mb ×8
HYS72T128020HU[2)]	1 GB	HYB18T1G800AF[2)]	512 Mbit	64Mb ×8

1) For a detailed description of all functionalities of the DRAM components on these modules see the referenced component datasheet.

2) Green Product

1.3 Pin Configuration

The pin configuration of the Unbuffered DDR2 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1** for non-ECC modules (×64) and **Figure 2** for ECC modules (×72).

Table 5 Pin Configuration of UDIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	**Clock Signals 2:0**
137	CK1	I	SSTL	
220	CK2	I	SSTL	
186	$\overline{CK0}$	I	SSTL	**Complement Clock Signals 2:0**
138	$\overline{CK1}$	I	SSTL	
221	$\overline{CK2}$	I	SSTL	
52	CKE0	I	SSTL	**Clock Enable Rank 0**
171	CKE1	I	SSTL	**Clock Enable Rank 1** *Note: 2 Ranks module*
	NC	NC	—	*Note: 1 Rank module*
Control Signals				
193	$\overline{S0}$	I	SSTL	**Chip Select Rank 0**
76	$\overline{S1}$	I	SSTL	**Chip Select Rank 1** *Note: 2 Ranks module*
	NC	NC	—	*Note: 1 Rank module*
192	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
74	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
73	$\overline{WE}$	I	SSTL	**Write Enable**
Address Signals				
71	BA0	I	SSTL	**Bank Address Bus 1:0**
190	BA1	I	SSTL	
54	BA2	I	SSTL	**Bank Address Bus 2** *Note: greater than 512Mb DDR2 SDRAMS*
	NC	NC	—	*Note: less than 1Gb DDR2 SDRAMS*
188	A0	I	SSTL	**Address Bus 12:0**
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	

Table 5 Pin Configuration of UDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
70	A10	I	SSTL	**Address Bus 12:0**
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module and 512M ×4/×8*
	NC	NC	—	*Note:* *1. Module based on 1 Gbit ×16* *2. Module based on 512 Mbit ×16 or smaller*
174	A14	I	SSTL	**Address Signal 14** *Note: Modules based on 2 Gbit*
	NC	NC	—	*Note: Modules based on 1 Gbit or smaller*
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	

Table 5 Pin Configuration of UDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
39	DQ26	I/O	SSTL	**Data Bus 63:0**
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	
206	DQ39	I/O	SSTL	
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	
98	DQ48	I/O	SSTL	
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	

Table 5 Pin Configuration of UDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
Check Bit Signal				
42	CB0	I/O	SSTL	**Check Bit 0** *Note: ECC type module only*
	NC	NC	—	*Note: Non-ECC module*
43	CB1	I/O	SSTL	**Check Bit 1** *Note: ECC type module only*
	NC	NC	—	*Note: Non-ECC module*
48	CB2	I/O	SSTL	**Check Bit 2** *Note: ECC type module only*
	NC	NC	—	*Note: Non-ECC module*
49	CB3	I/O	SSTL	**Check Bit 3** *Note: ECC type module only*
	NC	NC	—	*Note: Non-ECC module*
161	CB4	I/O	SSTL	**Check Bit 4** *Note: ECC type module only*
	NC	NC	—	*Note: Non-ECC module*
162	CB5	I/O	SSTL	**Check Bit 5** *Note: ECC type module only*
	NC	NC	—	*Note: Non-ECC module*
167	CB6	I/O	SSTL	**Check Bit 6** *Note: ECC type module only*
	NC	NC	—	*Note: Non-ECC module*
168	CB7	I/O	SSTL	**Check Bit 7** *Note: ECC type module only*
	NC	NC	—	*Note: Non-ECC module*
Data Strobe Bus				
7	DQS0	I/O	SSTL	**Data Strobe Bus 8:0** *Note: See block diagram for corresponding DQ signals*
16	DQS1	I/O	SSTL	
28	DQS2	I/O	SSTL	
37	DQS3	I/O	SSTL	
84	DQS4	I/O	SSTL	
93	DQS5	I/O	SSTL	
105	DQS6	I/O	SSTL	
114	DQS7	I/O	SSTL	
45	DQS8	I/O	SSTL	
6	$\overline{\text{DQS0}}$	I/O	SSTL	**Complement Data Strobe Bus 8:0** *Note: See block diagram for corresponding DQ signals*
15	$\overline{\text{DQS1}}$	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	

Table 5 Pin Configuration of UDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
92	$\overline{\text{DQS5}}$	I/O	SSTL	**Complement Data Strobe Bus 8:0**
104	$\overline{\text{DQS6}}$	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
46	$\overline{\text{DQS8}}$	I/O	SSTL	
Data Mask Signals				
125	DM0	I	SSTL	**Data Mask Bus 8:0**
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock**
119	SDA	I/O	OD	**Serial Bus Data**
239	SA0	I	CMOS	**Slave Address Select Bus 2:0**
240	SA1	I	CMOS	
101	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage**
238	V_{DDSPD}	PWR	—	**EEPROM Power Supply**
51,56,62,72,75,78,170,175,181, 191,194	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
53,59,64,67,69,172,178,184,187 189,197	V_{DD}	PWR	—	**Power Supply**
2,5,8,11,14,17,20,23,26,29,32, 35,38,41,44,47,50,65,66,79,82, 85,88,91,94,97,100,103,106, 109,112,115,118,121,124,127, 130,133,136,139,142,145,148, 151,154,157,160,163,166,169, 198,201,204,207,210,213,216, 219,222,225,228,231,234,237	V_{SS}	GND	—	**Ground Plane**
Other Pins				
195	ODT0			**On-Die Termination Control 0**
77	ODT1			**On-Die Termination Control 1**
	NC	NC	—	*Note: 1 Rank modules*
18,19,55,68,102,126,135,147, 156,165,173,203,212, 224,233	NC	NC	—	**Not connected** *Note: Pins not connected on Infineon UDIMMs*

Table 6 Abbreviations for Buffer Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 7 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

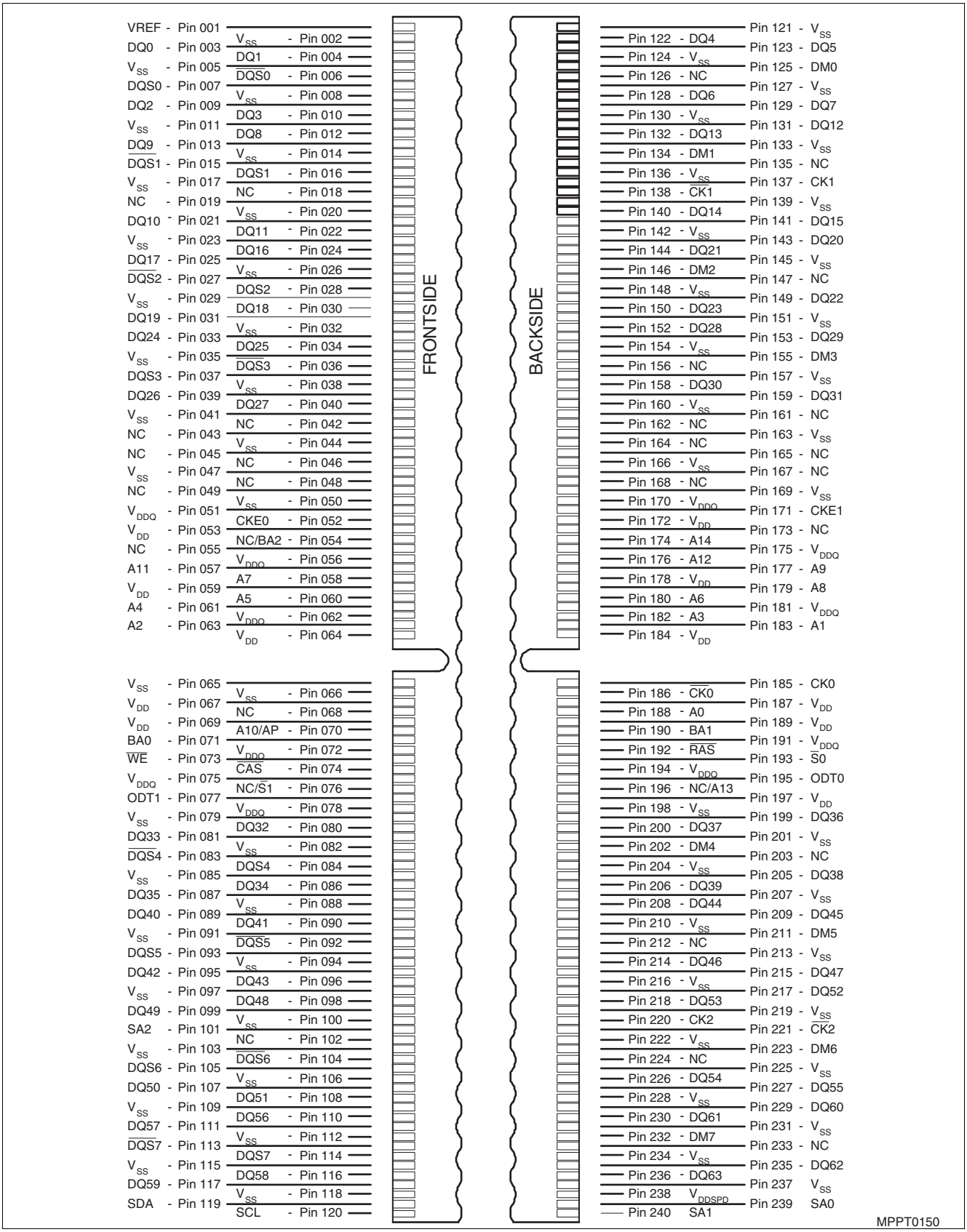

Figure 1 Pin Configuration UDIMM ×64 (240 Pin)

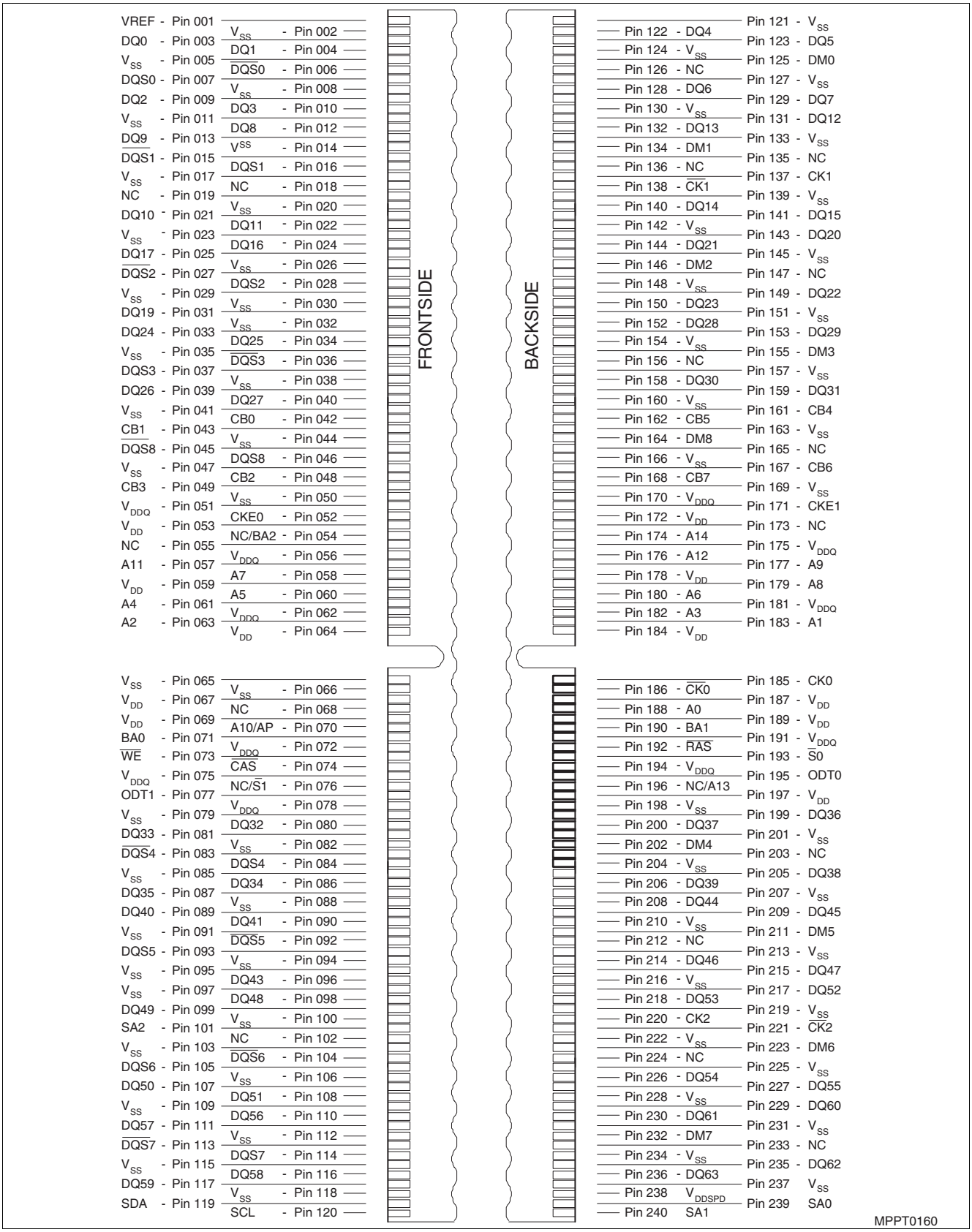

Figure 2 Pin Configuration UDIMM ×72 (240 Pin)

Table 8 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0-CKn, $\overline{CK}$0-$\overline{CK}$n	I	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0-CKEn	I	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down Mode or the Self Refresh Mode.
$\overline{S0}$-$\overline{Sn}$	I	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I	Active Low	When sampled at the cross point of the rising edge of CK,and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0-BAn	I	—	Selects internal SDRAM memory bank
ODT0-ODTn	I	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register.
A[9:0], A10/AP, A[12:11]	I	—	During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ[63:0]	I/O	—	Data Input/Output pins
DM[8:0]	I	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[8:0], $\overline{DQS}$[8:0]	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to V_{SS} through a 20 ohm to 10 Kohm resistor and DDR2 SDRAM mode registers programmed appropriately.
V_{DD}, V_{DDSPD}, V_{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
SDA	I/O	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to to V_{DDSPD} on the motherboard to act as a pull-up.
SCL	I	—	This signal is used to clock data into and out of the SPD EEPROM.
SA0-SAn	I	—	Address pins used to select the Serial Presence Detect base address.

2 Block Diagrams

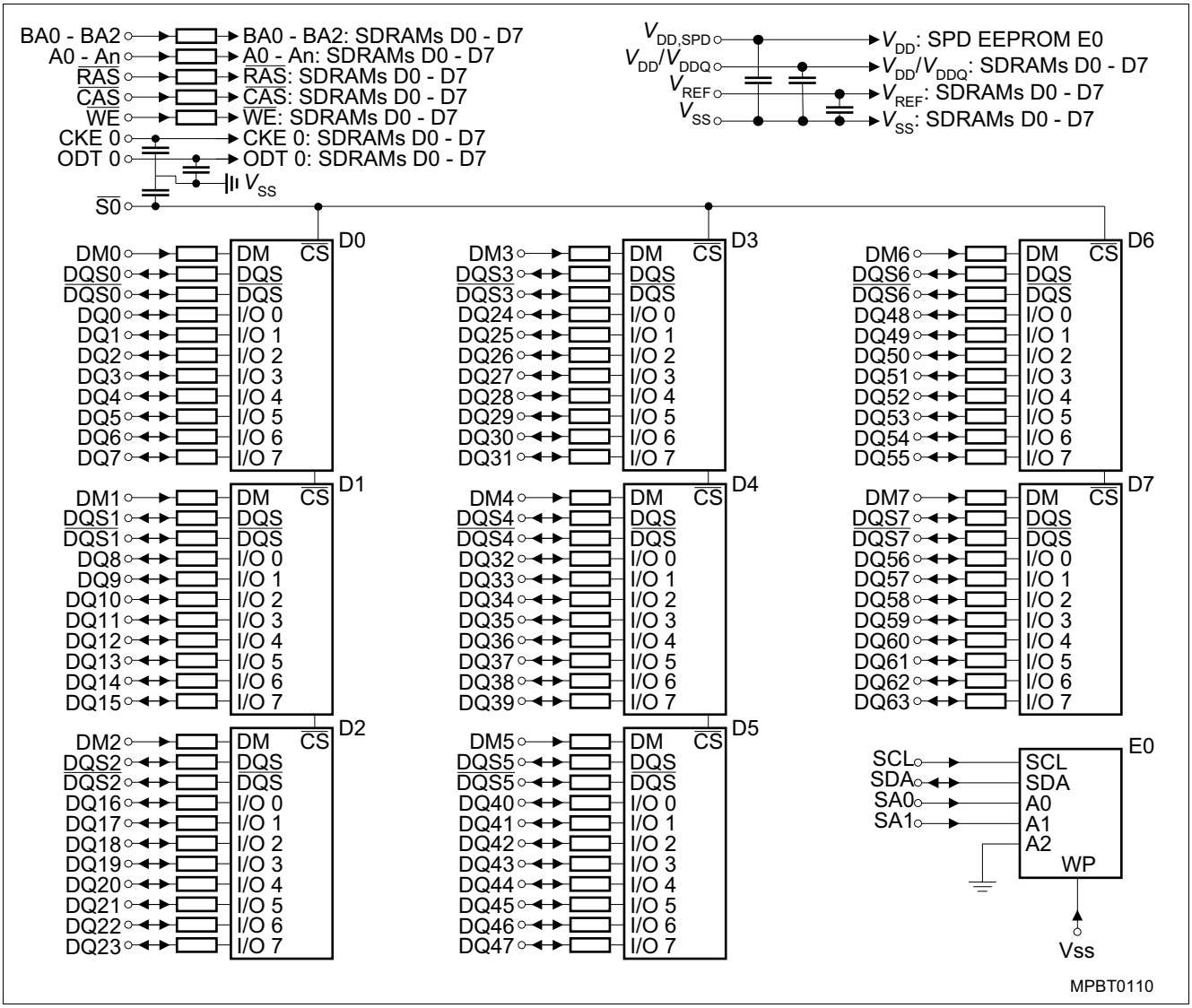

Figure 3 Block Diagram Raw Card A UDIMM (×64, 1 Rank, ×8)

Note

1. *DQ,DQS,$\overline{DQS}$,DM resistors are 22 Ω ± 5 %*
2. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ω ± 5 %*
3. *ODT,CKE,$\overline{S}$ capacitors are 24 pF*
4. *All $\overline{CK}$ lines have resistor termination between CK an $\overline{CK}$.*

Table 9 Clock Signal Loads

Clock Input	SDRAMs	Note
CK0,CKO	2	
CK1,CK1	3	
CK2,CK3	3	

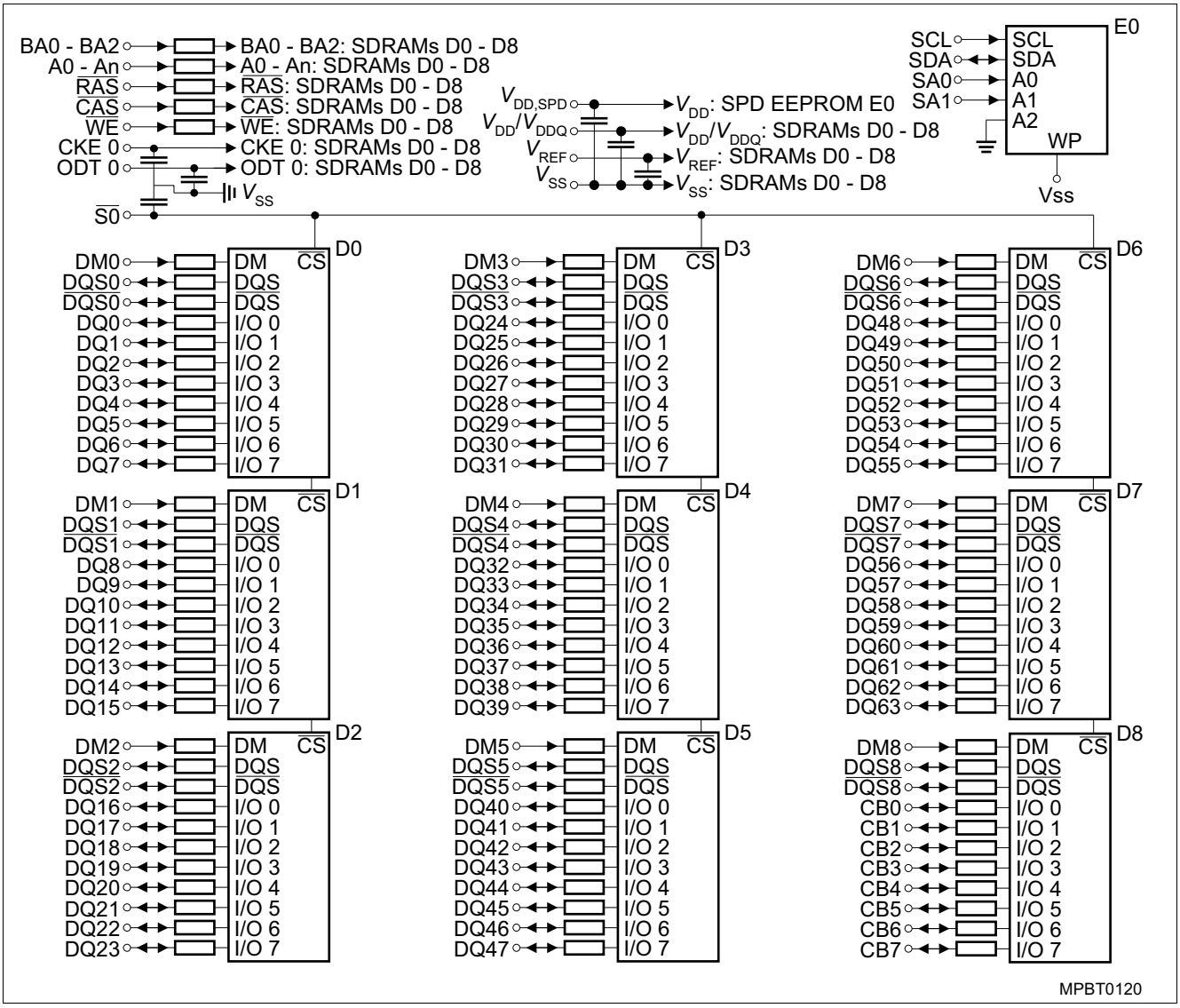

Figure 4 Block Diagram Raw Card A UDIMM (×72, 1 Rank, ×8)

Note

1. *DQ,DQS,$\overline{DQS}$,DM,CB resistors are 22 Ω ± 5 %*
2. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ω ± 5 %*
3. *ODT,CKE,$\overline{S}$ capacitors are 24 pF*
4. *All CK lines have resistor termination between CK an $\overline{CK}$.*

Table 10 Clock Signal Loads

Clock Input	SDRAMs	Note
CK0,$\overline{CK0}$	3	1)
CK1,$\overline{CK1}$	3	
CK2,CK3	3	

1) 2 SDRAMS for CK0 in case of non-ECC

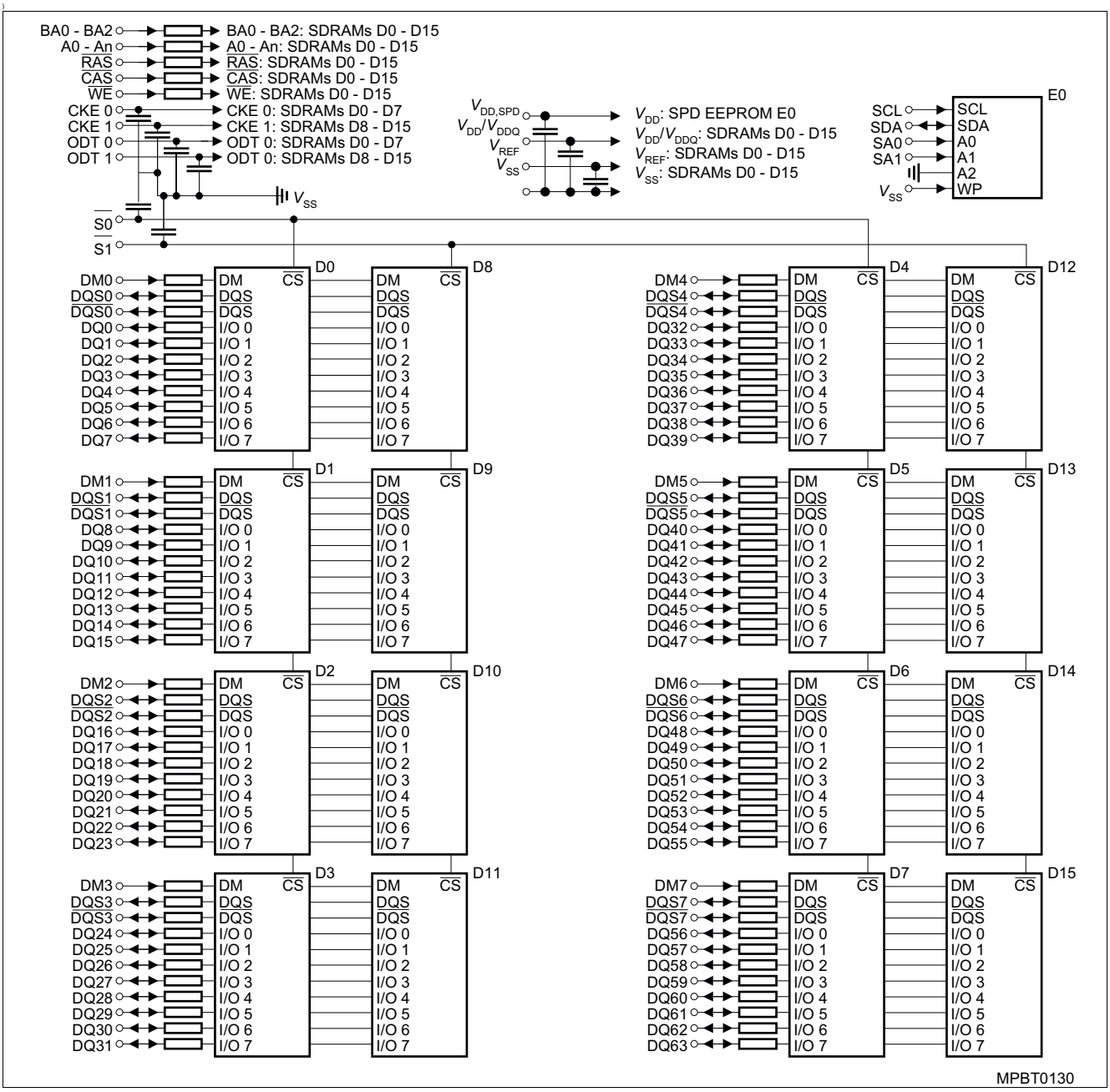

Figure 5 Block Diagram Raw Card B UDIMM (×64, 1 Rank, ×8)

Note

1. *DQ,DQS,$\overline{DQS}$,DM,CB resistors are 22 Ω ± 5 %*
2. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 7.5 Ω ± 5 %*
3. *ODT,CKE,$\overline{S}$ capacitors are 24 pF*
4. *All CK lines have resistor termination between CK an $\overline{CK}$.*

Table 11 Clock Signal Loads

Clock Input	SDRAMs	Note
CK0,$\overline{CK0}$	4	
CK1,$\overline{CK1}$	6	
CK2,CK3	6	

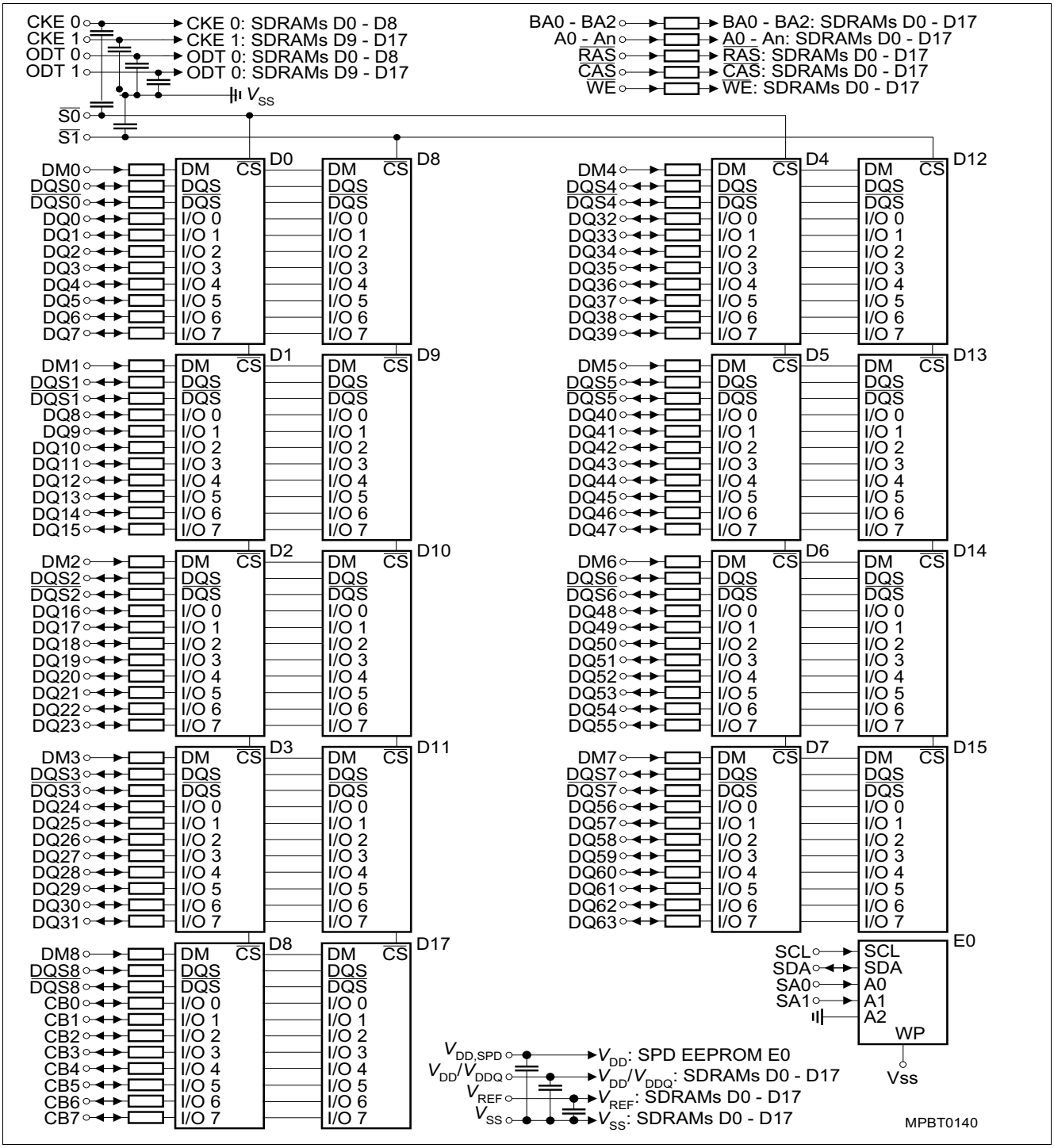

Figure 6 Block Diagram Raw Card B UDIMM (×72, 1 Rank, ×8)

Note:

1. *DQ,DQS,$\overline{DQS}$,DM,CB resistors are 22 Ω ± 5 %*
2. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 7.5 Ω ± 5 %*
3. *ODT,CKE,$\overline{S}$ capacitors are 24 pF*
4. *All $\overline{CK}$ lines have resistor termination between CK an $\overline{CK}$.*

Table 12 Clock Signal Loads

Clock Input	SDRAMs	Note
CK0,$\overline{CK0}$	6	
CK1,$\overline{CK1}$	6	
CK2,CK3	6	

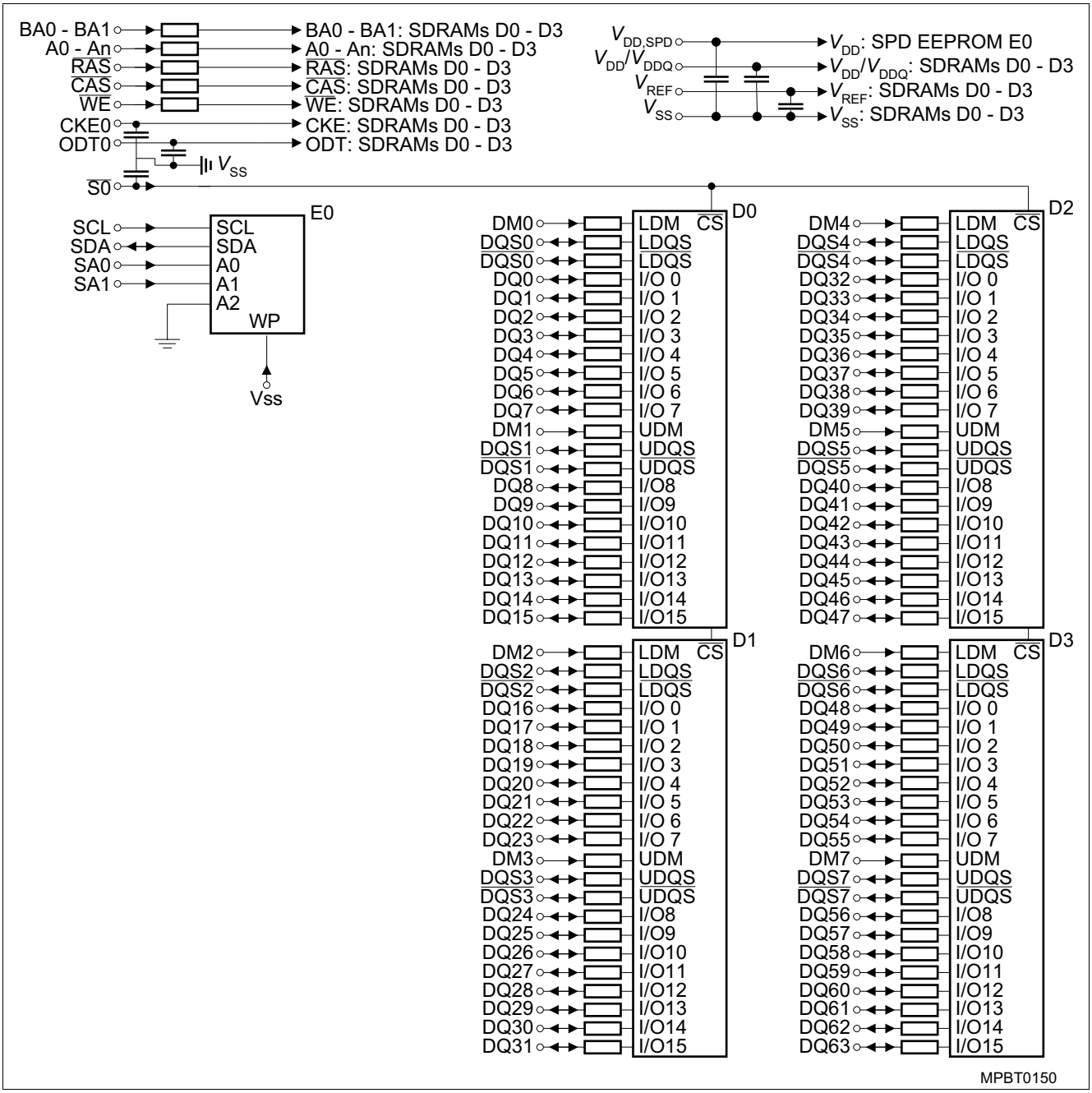

Figure 7 Block Diagram Raw Card C UDIMM (×64, 1Rank, ×16)

Note

1. *DQ, DQS, DM resistors are 22 Ω ± 5 %*
2. *BAn, An, RAS, CAS, WE resistors are 10 Ω ± 5 %*

3 Electrical Characteristics

3.1 Operating Conditions

Table 13 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V
Voltage on $V_{DD\,Q}$ relative to V_{SS}	V_{DDQ}	– 0.5	2.3	
Storage temperature range	T_{HSTG}	-55	+100	°C
Storage Humidity (without condensation)	H_{STG}	5	95	%

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 14 Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DIMM Module Operating Temperature Range (ambient)	T_{OPR}	0	+55	°C	
DRAM Component Case Temperature Range	T_{CASE}	0	+95	°C	1)2)3)4)
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	

1) *DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2.*

2) *Within the DRAM Component Case Temperature range all DRAM specification will be supported.*

3) *Above 85°C DRAM case temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs.*

4) *Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85°C case temperature before initiating self-refresh operation.*

Table 15 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	-
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
EEPROM Supply Voltage	V_{DDSPD}	1.7	–	3.6	V	
DC Input Logic High	$V_{IH\,(DC)}$	V_{REF} + 0.125	–	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\,(DC)}$	– 0.30	–	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5		5	µA	3)

1) *Under all conditions, V_{DDQ} must be less than or equal to V_{DD}*

2) *Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.*

3) *Voltage for pin connector under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all othe pins at 0 V. Current is per pin*

4 I_{DD} Specifications and Conditions

Table 16 I_{DD} Measurement Conditions[1)2)]

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CKmin.}$, $t_{RC} = t_{RCmin.}$, $t_{RAS} = t_{RASmin.}$, CKE is HIGH, CS is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CKmin.}$, $t_{RC} = t_{RCmin.}$, $t_{RAS} = t_{RASmin.}$, $t_{RCD} = t_{RCDmin.}$,AL = 0, CL = $CL_{min.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Power-Down Current All banks open; $t_{CK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to “0” (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $_{tCK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to “1” (Slow Power-down Exit);	$I_{DD3P(1)}$
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD4R}
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{RFCmin.}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 16 I_{DD} Measurement Conditions[1)2)] (cont'd)

Parameter	Symbol
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET = Low. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V

2) For details and notes see the relevant INFINEON component data sheet

Table 17 I_{DD} Specification

Product Type	HYS64T32000GU-3.7-A HYS64T32000HU-3.7-A	HYS64T64000GU-3.7-A HYS64T64000HU-3.7-A	HYS72T64000GU-3.7-A HYS72T64000HU-3.7-A	HYS64T128020GU-3.7-A HYS64T128020HU-3.7-A	HYS72T128020GU-3.7-A HYS72T128020HU-3.7-A	Unit	Notes
Organization	**256MB**	**512MB**	**512MB**	**1GB**	**1GB**		
	×64	**×64**	**×72**	**×64**	**×72**		
	1 Rank	**1 Rank**	**1 Rank**	**2 Ranks**	**2 Ranks**		
	–3.7	**–3.7**	**–3.7**	**–3.7**	**–3.7**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	320	520	585	552	621	mA	1)
I_{DD1}	360	600	675	632	711	mA	1)
I_{DD2P}	16	32	36	64	72	mA	1)
I_{DD2F}	160	320	360	640	720	mA	1)
I_{DD2Q}	120	240	270	480	540	mA	1)
$I_{DD3P(MRS=0)}$	64	128	144	256	288	mA	1)
$I_{DD3P(MRS=1)}$	20	40	45	80	90	mA	1)
I_{DD3N}	160	320	360	640	720	mA	1)
I_{DD4R}	400	720	810	752	846	mA	1)
I_{DD4W}	440	760	855	792	891	mA	1)
I_{DD5B}	520	1040	1170	1072	1206	mA	1)
I_{DD5D}	24	48	54	96	108	mA	1)
I_{DD6}	16	32	36	64	72	mA	1)
I_{DD7}	880	1120	1260	1152	1296	mA	1)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

Table 18 I_{DD} Specification

Product Type	HYS64T32000GU-5-A HYS64T32000HU-5-A	HYS64T64000GU-5-A HYS64T64000HU-5-A	HYS72T64000GU-5-A HYS72T64000HU-5-A	HYS64T128020GU-5-A HYS64T128020HU-5-A	HYS72T128020GU-5-A HYS72T128020HU-5-A	Unit	Notes
Organization	**256MB**	**512MB**	**512MB**	**1GB**	**1GB**		
	×64	**×64**	**×72**	**×64**	**×72**		
	1 Rank	**1 Rank**	**1 Rank**	**2 Ranks**	**2 Ranks**		
	–5	**–5**	**–5**	**–5**	**–5**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	280	440	495	472	531	mA	1)
I_{DD1}	300	480	540	512	576	mA	1)
I_{DD2P}	16	32	36	64	72	mA	1)
I_{DD2F}	128	256	288	512	576	mA	1)
I_{DD2Q}	100	200	225	400	450	mA	1)
$I_{DD3P(MRS=0)}$	52	104	117	208	234	mA	1)
$I_{DD3P(MRS=1)}$	20	40	45	80	90	mA	1)
I_{DD3N}	140	280	315	560	630	mA	1)
I_{DD4R}	340	560	630	592	666	mA	1)
I_{DD4W}	360	600	675	632	711	mA	1)
I_{DD5B}	480	960	1080	992	1116	mA	1)
I_{DD5D}	24	48	54	96	108	mA	1)
I_{DD6}	16	32	36	64	72	mA	1)
I_{DD7}	840	1040	1170	1072	1206	mA	1)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

4.1 I_{DD} Test Conditions

For testing the I_{DD} parameters, the following timing parameters are used:

Table 19 I_{DD} Measurement Test Conditions

Parameter		Symbol	-5	-3.7	Unit
			PC2-3200	PC2-4200	
			3-3-3	4-4-4	
CAS Latency		C_{Lmin}	3	4	t_{CK}
Clock Cycle Time		t_{CKmin}	5	3.75	ns
Active to Read or Write delay		t_{RCDmin}	15	15	ns
Active to Active / Auto-Refresh command period		t_{RCmin}	55	60	ns
Active bank A to Active bank B command delay	x8 [1]	t_{RRDmin}	7.5	7.5	ns
	x16 [2]	t_{RRDmin}	10	10	ns
Active to Precharge Command		t_{RASmin}	40	45	ns
Precharge Command Period		t_{RPmin}	15	15	ns
Auto-Refresh to Active / Auto-Refresh command period		t_{RFCmin}	105	105	ns
Average periodic Refresh interval		t_{REFI}	7.8	7.8	µs

1) For modules based on x8 components

2) For modules based on x16 components

4.2 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a “week” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tristate or driving 0 or 1, as long a ODT is enabled during a given period of time.

Table 20 ODT current per terminated pin:

		EMRS(1) State	min.	typ.	max.	Unit
Enabled ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	A6 = 0, A2 = 1	5	6	7.5	mA/DQ
		A6 = 1, A2 = 0	2.5	3	3.75	mA/DQ
Active ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	A6 = 0, A2 = 1	10	12	15	mA/DQ
		A6 = 1, A2 = 0	5	6	7.5	mA/DQ

Note: For power consumption calculations the ODT duty cycle has to be taken into account

5 Electrical Characteristics & AC Timings

5.1 AC Timing Parameter by Speed Grade (Component level data, for reference only)

Table 21 AC Timing - Absolute Specifications –5 / –3.7

Symbol	Parameter	–5		–3.7		Unit	Notes
		DDR2–400		DDR2–533			
		min.	max.	min.	max.		
t_{AC}	DQ output access time from CK/$\overline{CK}$	– 600	+ 600	-500	+500	ps	1)
t_{CCD}	$\overline{CAS}$ A to $\overline{CAS}$ B Command Period	2	-	2	-	t_{CK}	1)
t_{CH}	CK, $\overline{CK}$ high-level width	0.45	0.55	0.45	0.55	t_{CK}	1)
t_{CK}	Clock cycle time	5000	8000	5000	8000	ps	1)2)
		5000	8000	3750	8000	ps	1)3)
t_{CKE}	CKE minimum high and low pulse width	3	-	3	-	t_{CK}	1)
t_{CL}	CK, $\overline{CK}$ low-level width	0.45	0.55	0.45	0.55	t_{CK}	1)
t_{DAL}	Auto precharge write recovery + precharge time	WR+t_{RP}	-	WR+t_{RP}	-	t_{CK}	1)
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops low	t_{IS}+t_{CK}+t_{IH}	-	t_{IS}+t_{CK} +t_{IH}	-	ns	1)
t_{DH}	DQ and DM input hold time	400	-	350	-	ps	1)4)
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	0.35	-	t_{CK}	1)
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$	– 500	+ 500	–450	+450	ps	1)
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	t_{CK}	1)
t_{DQSS}	Write command to 1st DQS latching transition	WL - 0.25	WL +0.25	WL -0.25	WL +0.25	t_{CK}	1)
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)	-	350	-	300	ps	1)
t_{DS}	DQ and DM input setup time	400	-	350	-	ps	1)4)
t_{DSH}	DQS falling edge hold time from CLK (write cycle)	0.2	-	0.2	-	t_{CK}	1)
t_{DSS}	DQS falling edge to CLK setup time (write cycle)	0.2	-	0.2	-	t_{CK}	1)
t_{HP}	Clock Half Period	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})			1)
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$	-	t_{ACmax}	-	t_{ACmax}	ps	1)
t_{IH}	Address and control input hold time	600	-	600	-	ps	1)4)
t_{IPW}	Control and Addr. input pulse width (each input)	0.6	-	0.6	-	t_{CK}	1)
t_{IS}	Address and control input setup time	600	-	600	-	ps	1)4)
$t_{LZ(DQ)}$	DQ low-impedance from CK / $\overline{CK}$	2*t_{ACmin}	t_{ACmax}	2*t_{ACmin}	t_{ACmax}	ps	1)
$t_{LZ(DQS)}$	DQS low-impedance from CK / $\overline{CK}$	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ps	1)
t_{MRD}	Mode register set command cycle time	2	-	2	-	t_{CK}	1)
t_{OIT}	OCD drive mode output delay	0	12	0	12	ns	1)
t_{RAS}	Active to Precharge command	40	70000	45	70000	ns	1)
t_{RC}	Active to Active/Auto-refresh command period	55	-	60	-	ns	1)
t_{RCD}	Active to Read or Write delay (with and without Auto-Precharge) delay	15	-	15	-	ns	1)

Table 21 AC Timing - Absolute Specifications –5 / –3.7

Symbol	Parameter		–5		–3.7		Unit	Notes
			DDR2–400		DDR2–533			
			min.	max.	min.	max.		
t_{REFI}	Average Periodic Refresh Interval	0°C - 85°C	-	7.8	-	7.8	µs	1)
		85°C - 95°C	-	3.9	-	3.9		1)
t_{RFC}	Auto-refresh to Active/Auto-refresh command period		105	-	105	-	ns	1)
t_{RP}	Precharge command period		15	-	15	-	ns	1)
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	t_{CK}	1)
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	t_{CK}	1)
t_{RRD}	Active bank A to Active bank B command	x8 (1k page size)	7.5	-	7.5	-	ns	1)
		x16 (2k page size)	10	-	10	-	ns	1)
t_{RTP}	Internal read to precharge command delay		7.5	-	7.5	-	ns	1)
								1)
t_{QH}	Data Output hold time from DQS		t_{HP} - t_{QHS}	-	t_{HP}-t_{QHS}	-		1)
t_{QHS}	Data hold skew factor		-	450	-	400	ps	1)
t_{WPRE}	Write preamble		0.25	-	0.25	-	t_{CK}	1)
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	t_{CK}	1)
t_{WR}	Write recovery time		15	-	15	-	ns	1)
t_{WTR}	Internal write to read command delay		10	-	7.5	-	ns	1)
t_{XARD}	Exit power down to any valid command (other than NOP or Deselect)		2	-	2	-	t_{CK}	1)
t_{XARDS}	Exit active power-down mode to read command (slew exit, lower power)		6 - AL	-	6 - AL	-	t_{CK}	1)
t_{XP}	Exit precharge power-down to any valid command (other than NOP or Deselect)		2	-	2	-	t_{CK}	1)
t_{XSNR}	Exit Self-Refresh to non-read command		t_{RFC} + 10	-	t_{RFC} + 10	-	ns	1)5)
t_{XSRD}	Exit Self-Refresh to read command		200	-	200	-	t_{CK}	1)6)

1) For details and notes see the relevant INFINEON component datasheet

2) CL = 3

3) CL = 4 & 5

4) Timing definition and values for t_{IS}, t_{IH}, t_{DS} and t_{DH} may change due to actual JEDEC work. This may also effect the SPD code for these parameters

5) 0 °C ≤ T_{CASE} ≤ 85 °C

6) 85 °C < T_{CASE} ≤ 95 °C

Table 22 ODT AC Electrical Characteristics and Operating Conditions (all speed bins)

Symbol	Parameter / Condition		min.	max.	Unit
t_{ANPD}	ODT to Power Down Mode Entry Latency		3	-	t_{CK}
t_{AOF}	ODT turn-off		t_{AC}(min)	t_{AC}(max) + 0.6 ns	ns
t_{AOFD}	ODT turn-off delay		2.5	2.5	t_{CK}
t_{AOFPD}	ODT turn-off delay (Power-Down Modes)		t_{AC}(min) + 2 ns	2.5 t_{CK} + t_{AC}(max) + 1 ns	ns
t_{AON}	ODT turn-on	DDR2-400/533	t_{AC}(min)	t_{AC}(max) + 1 ns	ns
t_{AOND}	ODT turn-on delay		2	2	t_{CK}
t_{AONPD}	ODT turn-on (Power-Down Modes)		t_{AC}(min) + 2 ns	2 t_{CK} + tAC(max) + 1 ns	ns
t_{AXPD}	ODT Power Down Exit Latency		8	-	t_{CK}

6 SPD Codes

Table 23 SPD Codes for HYS[64/72]T[32/64]000GU–3.7–A

Product Type		**HYS64T32000GU–3.7–A**	**HYS64T64000GU–3.7–A**	**HYS72T64000GU–3.7–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–4200U–444**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0E	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60
6	Data Width	40	40	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	3D	3D
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	50
11	Error Correction Support (non-ECC, ECC)	00	00	02
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	08	08
14	Error Checking SDRAM Width	00	00	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	Not used	00	00	00
20	DIMM Type Information	02	02	02
21	DIMM Attributes	00	00	00
22	Component Attributes	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	3D	3D
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50	50
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60	60

Table 23 SPD Codes for HYS[64/72]T[32/64]000GU–3.7–A (cont'd)

Product Type		**HYS64T32000GU–3.7–A**	**HYS64T64000GU–3.7–A**	**HYS72T64000GU–3.7–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–4200U–444**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
27	$t_{RP.min}$ [ns]	3C	3C	3C
28	$t_{RRD.min}$ [ns]	28	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	25	25	25
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	37	37	37
34	$t_{DS.min}$ [ns]	10	10	10
35	$t_{DH.min}$ [ns]	22	22	22
36	$t_{WR.min}$ [ns]	3C	3C	3C
37	$t_{WTR.min}$ [ns]	1E	1E	1E
38	$t_{RTP.min}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80
44	$t_{DQSQ.max}$ [ns]	1E	1E	1E
45	$t_{QHS.max}$ [ns]	28	28	28
46	PLL Relock Time	00	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	53	51	51
48	Psi(T-A) DRAM	72	78	78
49	ΔT_0 (DT0)	52	3E	3E
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	2B	2E	2E
51	ΔT_{2P} (DT2P)	1D	1E	1E
52	ΔT_{3N} (DT3N)	1D	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	23	24	24
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	17	17

Table 23 SPD Codes for HYS[64/72]T[32/64]000GU–3.7–A (cont'd)

Product Type		**HYS64T32000GU–3.7–A**	**HYS64T64000GU–3.7–A**	**HYS72T64000GU–3.7–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–4200U–444**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
55	ΔT_{4R} (DT4R) / $\Delta T_{4R4W\ S}$ Sign (DT4R4W)	36	34	34
56	ΔT_{5B} (DT5B)	1C	1E	1E
57	ΔT_{7} (DT7)	30	20	20
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	11	11	11
63	Checksum of Bytes 0-62	B9	CF	E1
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	37
74	Product Type, Char 2	34	34	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34
78	Product Type, Char 6	30	30	30
79	Product Type, Char 7	30	30	30
80	Product Type, Char 8	30	30	30
81	Product Type, Char 9	47	47	47
82	Product Type, Char 10	55	55	55
83	Product Type, Char 11	33	33	33
84	Product Type, Char 12	2E	2E	2E
85	Product Type, Char 13	37	37	37
86	Product Type, Char 14	41	41	41
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20

Table 23 SPD Codes for HYS[64/72]T[32/64]000GU–3.7–A (cont'd)

Product Type		**HYS64T32000GU–3.7–A**	**HYS64T64000GU–3.7–A**	**HYS72T64000GU–3.7–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–4200U–444**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx
99 -127	Not Used	00	00	00
128-255	BLANK	FF	FF	FF

Table 24 SPD Codes HYS[64/72]T128020GU–3.7–A

Product Type		**HYS64T128020GU–3.7–A**	**HYS72T128020GU–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	3D
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	04	04
18	Supported CAS Latencies	38	38
19	Not used	00	00
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	3D
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60

Table 24 SPD Codes HYS[64/72]T128020GU–3.7–A (cont'd)

Product Type		**HYS64T128020GU–3.7–A**	**HYS72T128020GU–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
27	$t_{RP.min}$ [ns]	3C	3C
28	$t_{RRD.min}$ [ns]	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D
31	Module Density per Rank	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	25	25
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	37	37
34	$t_{DS.min}$ [ns]	10	10
35	$t_{DH.min}$ [ns]	22	22
36	$t_{WR.min}$ [ns]	3C	3C
37	$t_{WTR.min}$ [ns]	1E	1E
38	$t_{RTP.min}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	00	00
41	$t_{RC.min}$ [ns]	3C	3C
42	$t_{RFC.min}$ [ns]	69	69
43	$t_{CK.max}$ [ns]	80	80
44	$t_{DQSQ.max}$ [ns]	1E	1E
45	$t_{QHS.max}$ [ns]	28	28
46	PLL Relock Time	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51
48	Psi(T-A) DRAM	78	78
49	ΔT_0 (DT0)	3E	3E
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	2E	2E
51	ΔT_{2P} (DT2P)	1E	1E
52	ΔT_{3N} (DT3N)	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	24	24
54	$\Delta T_{3P.slow}$ (DT3P slow)	17	17

Table 24 SPD Codes HYS[64/72]T128020GU–3.7–A (cont'd)

Product Type		**HYS64T128020GU–3.7–A**	**HYS72T128020GU–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
55	ΔT_{4R} (DT4R) / $\Delta T_{4R4W\ S}$ Sign (DT4R4W)	34	34
56	ΔT_{5B} (DT5B)	1E	1E
57	ΔT_{7} (DT7)	20	20
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	ΔT_{PLL} (DTPLL)	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00
62	SPD Revision	11	11
63	Checksum of Bytes 0-62	D0	E2
64	JEDEC ID Code of Infineon (1)	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	31	31
77	Product Type, Char 5	32	32
78	Product Type, Char 6	38	38
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	47	47
83	Product Type, Char 11	55	55
84	Product Type, Char 12	33	33
85	Product Type, Char 13	2E	2E
86	Product Type, Char 14	37	37
87	Product Type, Char 15	41	41
88	Product Type, Char 16	20	20

Table 24 SPD Codes HYS[64/72]T128020GU–3.7–A (cont'd)

Product Type		**HYS64T128020GU–3.7–A**	**HYS72T128020GU–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	2x	2x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95	Module Serial Number (1)	xx	xx
96	Module Serial Number (2)	xx	xx
97	Module Serial Number (3)	xx	xx
98	Module Serial Number (4)	xx	xx
99 -127	Not Used	00	00
128-255	BLANK	FF	FF

Table 25 SPD Codes for HYS[64/72]T[32/64]000HU–3.7–A

Product Type		**HYS64T32000HU–3.7–A**	**HYS64T64000HU–3.7–A**	**HYS72T64000HU–3.7–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–4200U–444**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0E	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60
6	Data Width	40	40	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	3D	3D
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	50
11	Error Correction Support (non-ECC, ECC)	00	00	02
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	08	08
14	Error Checking SDRAM Width	00	00	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	Not used	00	00	00
20	DIMM Type Information	02	02	02
21	DIMM Attributes	00	00	00
22	Component Attributes	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	3D	3D
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50	50
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60	60
27	$t_{RP.min}$ [ns]	3C	3C	3C

Table 25 SPD Codes for HYS[64/72]T[32/64]000HU–3.7–A (cont'd)

Product Type		**HYS64T32000HU–3.7–A**	**HYS64T64000HU–3.7–A**	**HYS72T64000HU–3.7–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–4200U–444**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
28	$t_{RRD.min}$ [ns]	28	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	25	25	25
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	37	37	37
34	$t_{DS.min}$ [ns]	10	10	10
35	$t_{DH.min}$ [ns]	22	22	22
36	$t_{WR.min}$ [ns]	3C	3C	3C
37	$t_{WTR.min}$ [ns]	1E	1E	1E
38	$t_{RTP.min}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80
44	$t_{DQSQ.max}$ [ns]	1E	1E	1E
45	$t_{QHS.max}$ [ns]	28	28	28
46	PLL Relock Time	00	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	53	51	51
48	Psi(T-A) DRAM	72	78	78
49	ΔT_0 (DT0)	52	3E	3E
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	2B	2E	2E
51	ΔT_{2P} (DT2P)	1D	1E	1E
52	ΔT_{3N} (DT3N)	1D	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	23	24	24
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	17	17
55	ΔT_{4R} (DT4R) / $\Delta T_{4R4W\ S}$ Sign (DT4R4W)	36	34	34

Table 25 SPD Codes for HYS[64/72]T[32/64]000HU–3.7–A (cont'd)

Product Type		**HYS64T32000HU–3.7–A**	**HYS64T64000HU–3.7–A**	**HYS72T64000HU–3.7–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–4200U–444**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
56	ΔT_{5B} (DT5B)	1C	1E	1E
57	ΔT_{7} (DT7)	30	20	20
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	11	11	11
63	Checksum of Bytes 0-62	B9	CF	E1
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	37
74	Product Type, Char 2	34	34	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34
78	Product Type, Char 6	30	30	30
79	Product Type, Char 7	30	30	30
80	Product Type, Char 8	30	30	30
81	Product Type, Char 9	48	48	48
82	Product Type, Char 10	55	55	55
83	Product Type, Char 11	33	33	33
84	Product Type, Char 12	2E	2E	2E
85	Product Type, Char 13	37	37	37
86	Product Type, Char 14	41	41	41
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20

Table 25 SPD Codes for HYS[64/72]T[32/64]000HU–3.7–A (cont'd)

Product Type		**HYS64T32000HU–3.7–A**	**HYS64T64000HU–3.7–A**	**HYS72T64000HU–3.7–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–4200U–444**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx
99 -127	Not Used	00	00	00
128-255	BLANK	FF	FF	FF

Table 26 SPD Codes for HYS[64/72]T128020HU–3.7–A

Product Type		HYS64T128020HU–3.7–A	HYS72T128020HU–3.7–A
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	3D
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	04	04
18	Supported CAS Latencies	38	38
19	Not used	00	00
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	3D
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	50	50
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60

Table 26 SPD Codes for HYS[64/72]T128020HU–3.7–A (cont'd)

Product Type		**HYS64T128020HU–3.7–A**	**HYS72T128020HU–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
27	$t_{RP.min}$ [ns]	3C	3C
28	$t_{RRD.min}$ [ns]	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D
31	Module Density per Rank	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	25	25
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	37	37
34	$t_{DS.min}$ [ns]	10	10
35	$t_{DH.min}$ [ns]	22	22
36	$t_{WR.min}$ [ns]	3C	3C
37	$t_{WTR.min}$ [ns]	1E	1E
38	$t_{RTP.min}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	00	00
41	$t_{RC.min}$ [ns]	3C	3C
42	$t_{RFC.min}$ [ns]	69	69
43	$t_{CK.max}$ [ns]	80	80
44	$t_{DQSQ.max}$ [ns]	1E	1E
45	$t_{QHS.max}$ [ns]	28	28
46	PLL Relock Time	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51
48	Psi(T-A) DRAM	78	78
49	ΔT_0 (DT0)	3E	3E
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	2E	2E
51	ΔT_{2P} (DT2P)	1E	1E
52	ΔT_{3N} (DT3N)	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	24	24
54	$\Delta T_{3P.slow}$ (DT3P slow)	17	17

Table 26 SPD Codes for HYS[64/72]T128020HU–3.7–A (cont'd)

Product Type		**HYS64T128020HU–3.7–A**	**HYS72T128020HU–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
55	ΔT_{4R} (DT4R) / $\Delta T_{4R4W\,S}$ Sign (DT4R4W)	34	34
56	ΔT_{5B} (DT5B)	1E	1E
57	ΔT_{7} (DT7)	20	20
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	ΔT_{PLL} (DTPLL)	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00
62	SPD Revision	11	11
63	Checksum of Bytes 0-62	D0	E2
64	JEDEC ID Code of Infineon (1)	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	31	31
77	Product Type, Char 5	32	32
78	Product Type, Char 6	38	38
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	48	48
83	Product Type, Char 11	55	55
84	Product Type, Char 12	33	33
85	Product Type, Char 13	2E	2E
86	Product Type, Char 14	37	37
87	Product Type, Char 15	41	41
88	Product Type, Char 16	20	20

Table 26 SPD Codes for HYS[64/72]T128020HU–3.7–A (cont'd)

Product Type		**HYS64T128020HU–3.7–A**	**HYS72T128020HU–3.7–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–4200U–444**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	2x	2x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95	Module Serial Number (1)	xx	xx
96	Module Serial Number (2)	xx	xx
97	Module Serial Number (3)	xx	xx
98	Module Serial Number (4)	xx	xx
99 -127	Not Used	00	00
128-255	BLANK	FF	FF

Table 27 SPD Codes for HYS[64/72]T32000GU–5–A

Product Type		**HYS64T32000GU–5–A**	**HYS64T64000GU–5–A**	**HYS72T64000GU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0E	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60
6	Data Width	40	40	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	60	60	60
11	Error Correction Support (non-ECC, ECC)	00	00	02
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	08	08
14	Error Checking SDRAM Width	00	00	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	Not used	00	00	00
20	DIMM Type Information	02	02	02
21	DIMM Attributes	00	00	00
22	Component Attributes	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	50	50	50
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	60	60	60
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60	60
27	$t_{RP.min}$ [ns]	3C	3C	3C

Table 27 SPD Codes for HYS[64/72]T32000GU–5–A (cont'd)

Product Type		**HYS64T32000GU–5–A**	**HYS64T64000GU–5–A**	**HYS72T64000GU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
28	$t_{RRD.min}$ [ns]	28	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	35	35	35
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	47	47	47
34	$t_{DS.min}$ [ns]	15	15	15
35	$t_{DH.min}$ [ns]	27	27	27
36	$t_{WR.min}$ [ns]	3C	3C	3C
37	$t_{WTR.min}$ [ns]	28	28	28
38	$t_{RTP.min}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80
44	$t_{DQSQ.max}$ [ns]	23	23	23
45	$t_{QHS.max}$ [ns]	2D	2D	2D
46	PLL Relock Time	00	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51	51
48	Psi(T-A) DRAM	72	78	78
49	ΔT_0 (DT0)	42	32	32
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	23	24	24
51	ΔT_{2P} (DT2P)	1D	1E	1E
52	ΔT_{3N} (DT3N)	19	1B	1B
53	$\Delta T_{3P.fast}$ (DT3P fast)	1C	1E	1E
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	17	17
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} S Sign (DT4R4W)	2E	28	28
56	ΔT_{5B} (DT5B)	1A	1B	1B

Table 27 SPD Codes for HYS[64/72]T32000GU–5–A (cont'd)

Product Type		**HYS64T32000GU–5–A**	**HYS64T64000GU–5–A**	**HYS72T64000GU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
57	ΔT_7 (DT7)	2D	1E	1E
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	11	11	11
63	Checksum of Bytes 0-62	0B	23	35
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2- 8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	37
74	Product Type, Char 2	34	34	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34
78	Product Type, Char 6	30	30	30
79	Product Type, Char 7	30	30	30
80	Product Type, Char 8	30	30	30
81	Product Type, Char 9	47	47	47
82	Product Type, Char 10	55	55	55
83	Product Type, Char 11	35	35	35
84	Product Type, Char 12	41	41	41
85	Product Type, Char 13	20	20	20
86	Product Type, Char 14	20	20	20
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	2x	2x

Table 27 SPD Codes for HYS[64/72]T32000GU–5–A (cont'd)

Product Type		**HYS64T32000GU–5–A**	**HYS64T64000GU–5–A**	**HYS72T64000GU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx
99 -127	Not Used	00	00	00
128-255	BLANK	FF	FF	FF

Table 28 SPD Codes for HYS[64/72]T128020GU–5–A

Product Type		**HYS64T128020GU–5–A**	**HYS72T128020GU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E

Table 28 SPD Codes for HYS[64/72]T128020GU–5–A (cont'd)

Product Type		**HYS64T128020GU–5–A**	**HYS72T128020GU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	60	60
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	04	04
18	Supported CAS Latencies	38	38
19	Not used	00	00
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	50	50
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	60	60
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60
27	$t_{RP.min}$ [ns]	3C	3C
28	$t_{RRD.min}$ [ns]	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D
31	Module Density per Rank	80	80

Table 28 SPD Codes for HYS[64/72]T128020GU–5–A (cont'd)

Product Type		**HYS64T128020GU–5–A**	**HYS72T128020GU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	35	35
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	47	47
34	$t_{DS.min}$ [ns]	15	15
35	$t_{DH.min}$ [ns]	27	27
36	$t_{WR.min}$ [ns]	3C	3C
37	$t_{WTR.min}$ [ns]	28	28
38	$t_{RTP.min}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	00	00
41	$t_{RC.min}$ [ns]	3C	3C
42	$t_{RFC.min}$ [ns]	69	69
43	$t_{CK.max}$ [ns]	80	80
44	$t_{DQSQ.max}$ [ns]	23	23
45	$t_{QHS.max}$ [ns]	2D	2D
46	PLL Relock Time	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51
48	Psi(T-A) DRAM	78	78
49	ΔT_0 (DT0)	32	32
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	24	24
51	ΔT_{2P} (DT2P)	1E	1E
52	ΔT_{3N} (DT3N)	1B	1B
53	$\Delta T_{3P.fast}$ (DT3P fast)	1E	1E
54	$\Delta T_{3P.slow}$ (DT3P slow)	17	17
55	ΔT_{4R} (DT4R) / $\Delta T_{4R4W\ S}$ Sign (DT4R4W)	28	28
56	ΔT_{5B} (DT5B)	1B	1B
57	ΔT_7 (DT7)	1E	1E
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00

Table 28 SPD Codes for HYS[64/72]T128020GU–5–A (cont'd)

Product Type		**HYS64T128020GU–5–A**	**HYS72T128020GU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
60	ΔT_{PLL} (DTPLL)	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00
62	SPD Revision	11	11
63	Checksum of Bytes 0-62	24	36
64	JEDEC ID Code of Infineon (1)	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	31	31
77	Product Type, Char 5	32	32
78	Product Type, Char 6	38	38
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	47	47
83	Product Type, Char 11	55	55
84	Product Type, Char 12	35	35
85	Product Type, Char 13	41	41
86	Product Type, Char 14	20	20
87	Product Type, Char 15	20	20
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	2x	2x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx

Table 28 SPD Codes for HYS[64/72]T128020GU–5–A (cont'd)

Product Type		**HYS64T128020GU–5–A**	**HYS72T128020GU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
94	Module Manufacturing Date Week	xx	xx
95	Module Serial Number (1)	xx	xx
96	Module Serial Number (2)	xx	xx
97	Module Serial Number (3)	xx	xx
98	Module Serial Number (4)	xx	xx
99 -127	Not Used	00	00
128-255	BLANK	FF	FF

Table 29 SPD Codes for HYS[64/72]T[32/64]000HU–5–A

Product Type		**HYS64T32000HU–5–A**	**HYS64T64000HU–5–A**	**HYS72T64000HU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0D	0E	0E
4	Number of Column Addresses	0A	0A	0A
5	DIMM Rank and Stacking Information	60	60	60

Table 29 SPD Codes for HYS[64/72]T[32/64]000HU–5–A (cont'd)

Product Type		**HYS64T32000HU–5–A**	**HYS64T64000HU–5–A**	**HYS72T64000HU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
6	Data Width	40	40	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	60	60	60
11	Error Correction Support (non-ECC, ECC)	00	00	02
12	Refresh Rate and Type	82	82	82
13	Primary SDRAM Width	10	08	08
14	Error Checking SDRAM Width	00	00	08
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	Not used	00	00	00
20	DIMM Type Information	02	02	02
21	DIMM Attributes	00	00	00
22	Component Attributes	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	50	50	50
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	60	60	60
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60	60
27	$t_{RP.min}$ [ns]	3C	3C	3C
28	$t_{RRD.min}$ [ns]	28	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D
31	Module Density per Rank	40	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	35	35	35
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	47	47	47
34	$t_{DS.min}$ [ns]	15	15	15

Table 29 SPD Codes for HYS[64/72]T[32/64]000HU–5–A (cont'd)

Product Type		**HYS64T32000HU–5–A**	**HYS64T64000HU–5–A**	**HYS72T64000HU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
35	$t_{DH.min}$ [ns]	27	27	27
36	$t_{WR.min}$ [ns]	3C	3C	3C
37	$t_{WTR.min}$ [ns]	28	28	28
38	$t_{RTP.min}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80
44	$t_{DQSQ.max}$ [ns]	23	23	23
45	$t_{QHS.max}$ [ns]	2D	2D	2D
46	PLL Relock Time	00	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51	51
48	Psi(T-A) DRAM	72	78	78
49	ΔT_0 (DT0)	42	32	32
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	23	24	24
51	ΔT_{2P} (DT2P)	1D	1E	1E
52	ΔT_{3N} (DT3N)	19	1B	1B
53	$\Delta T_{3P.fast}$ (DT3P fast)	1C	1E	1E
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	17	17
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} S Sign (DT4R4W)	2E	28	28
56	ΔT_{5B} (DT5B)	1A	1B	1B
57	ΔT_7 (DT7)	2D	1E	1E
58	Psi(ca) PLL	00	00	00
59	Psi(ca) REG	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00
62	SPD Revision	11	11	11
63	Checksum of Bytes 0-62	0B	23	35

Table 29 SPD Codes for HYS[64/72]T[32/64]000HU–5–A (cont'd)

Product Type		**HYS64T32000HU–5–A**	**HYS64T64000HU–5–A**	**HYS72T64000HU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	36	36	37
74	Product Type, Char 2	34	34	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	33	36	36
77	Product Type, Char 5	32	34	34
78	Product Type, Char 6	30	30	30
79	Product Type, Char 7	30	30	30
80	Product Type, Char 8	30	30	30
81	Product Type, Char 9	48	48	48
82	Product Type, Char 10	55	55	55
83	Product Type, Char 11	35	35	35
84	Product Type, Char 12	41	41	41
85	Product Type, Char 13	20	20	20
86	Product Type, Char 14	20	20	20
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95	Module Serial Number (1)	xx	xx	xx
96	Module Serial Number (2)	xx	xx	xx
97	Module Serial Number (3)	xx	xx	xx
98	Module Serial Number (4)	xx	xx	xx

Table 29 SPD Codes for HYS[64/72]T[32/64]000HU–5–A (cont'd)

Product Type		**HYS64T32000HU–5–A**	**HYS64T64000HU–5–A**	**HYS72T64000HU–5–A**
Organization		**256 MB**	**512 MB**	**512 MB**
		×64	**×64**	**×72**
		1 Rank (×16)	**1 Rank (×8)**	**1 Rank (×8)**
Label Code		**PC2–3200U–333**		
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
99 -127	Not Used	00	00	00
128-255	BLANK	FF	FF	FF

Table 30 SPD Codes for HYS[64/72]T128020HU–5–A

Product Type		**HYS64T128020HU–5–A**	**HYS72T128020HU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0E	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	60	60

Table 30 SPD Codes for HYS[64/72]T128020HU–5–A (cont'd)

Product Type		**HYS64T128020HU–5–A**	**HYS72T128020HU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	04	04
18	Supported CAS Latencies	38	38
19	Not used	00	00
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	50	50
24	t_{AC} SDRAM @ CL_{max} -1 [ns]	60	60
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{max} -2 [ns]	60	60
27	$t_{RP.min}$ [ns]	3C	3C
28	$t_{RRD.min}$ [ns]	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D
31	Module Density per Rank	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	35	35
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	47	47
34	$t_{DS.min}$ [ns]	15	15
35	$t_{DH.min}$ [ns]	27	27
36	$t_{WR.min}$ [ns]	3C	3C
37	$t_{WTR.min}$ [ns]	28	28
38	$t_{RTP.min}$ [ns]	1E	1E

Table 30 SPD Codes for HYS[64/72]T128020HU–5–A (cont'd)

Product Type		**HYS64T128020HU–5–A**	**HYS72T128020HU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	00	00
41	$t_{RC.min}$ [ns]	3C	3C
42	$t_{RFC.min}$ [ns]	69	69
43	$t_{CK.max}$ [ns]	80	80
44	$t_{DQSQ.max}$ [ns]	23	23
45	$t_{QHS.max}$ [ns]	2D	2D
46	PLL Relock Time	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51
48	Psi(T-A) DRAM	78	78
49	ΔT_0 (DT0)	32	32
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	24	24
51	ΔT_{2P} (DT2P)	1E	1E
52	ΔT_{3N} (DT3N)	1B	1B
53	$\Delta T_{3P.fast}$ (DT3P fast)	1E	1E
54	$\Delta T_{3P.slow}$ (DT3P slow)	17	17
55	ΔT_{4R} (DT4R) / $\Delta T_{4R4W\ S}$ Sign (DT4R4W)	28	28
56	ΔT_{5B} (DT5B)	1B	1B
57	ΔT_7 (DT7)	1E	1E
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	ΔT_{PLL} (DTPLL)	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00
62	SPD Revision	11	11
63	Checksum of Bytes 0-62	24	36
64	JEDEC ID Code of Infineon (1)	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00
72	Module Manufacturer Location	xx	xx

Table 30 SPD Codes for HYS[64/72]T128020HU–5–A (cont'd)

Product Type		**HYS64T128020HU–5–A**	**HYS72T128020HU–5–A**
Organization		**1 GByte**	**1 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–3200U–333**	
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	31	31
77	Product Type, Char 5	32	32
78	Product Type, Char 6	38	38
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	48	48
83	Product Type, Char 11	55	55
84	Product Type, Char 12	35	35
85	Product Type, Char 13	41	41
86	Product Type, Char 14	20	20
87	Product Type, Char 15	20	20
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	2x	2x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95	Module Serial Number (1)	xx	xx
96	Module Serial Number (2)	xx	xx
97	Module Serial Number (3)	xx	xx
98	Module Serial Number (4)	xx	xx
99 -127	Not Used	00	00
128-255	BLANK	FF	FF

7 Package Outlines

7.1 Raw Card A

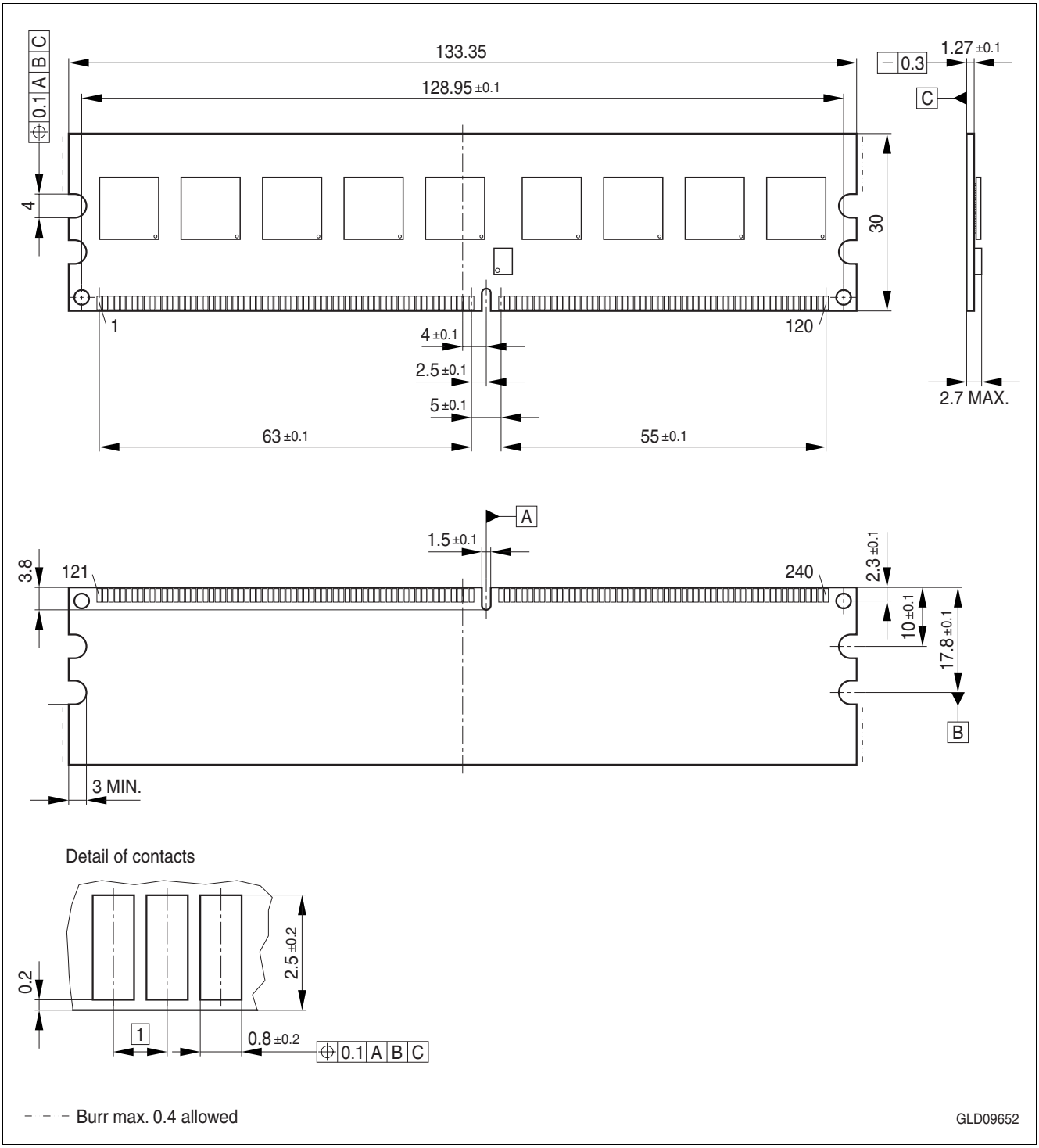

Figure 8 Package Outline L-DIM-240-1

7.2 Raw Card B

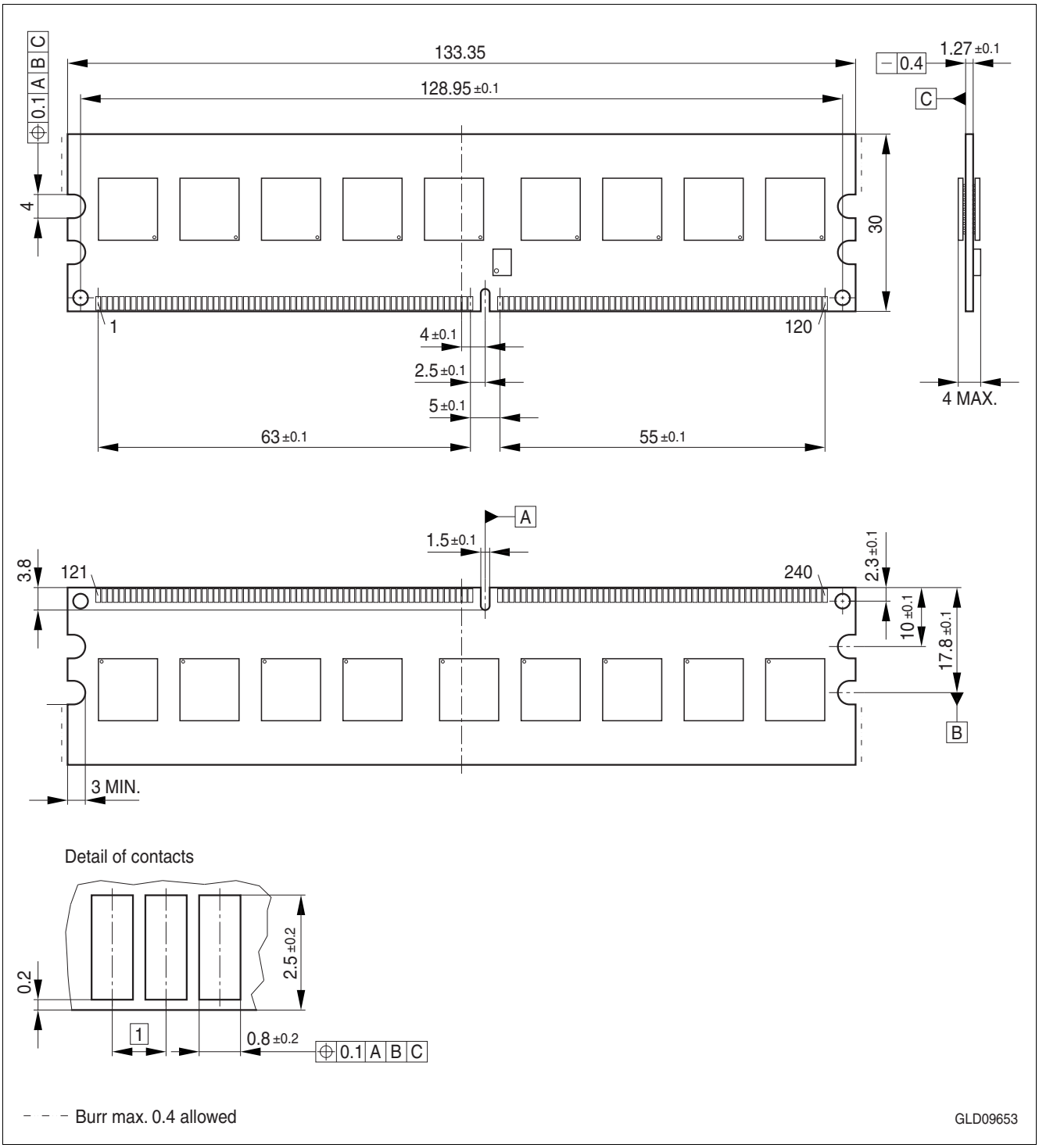

Figure 9 Package Outline L-DIM-240-2

7.3 Raw Card C

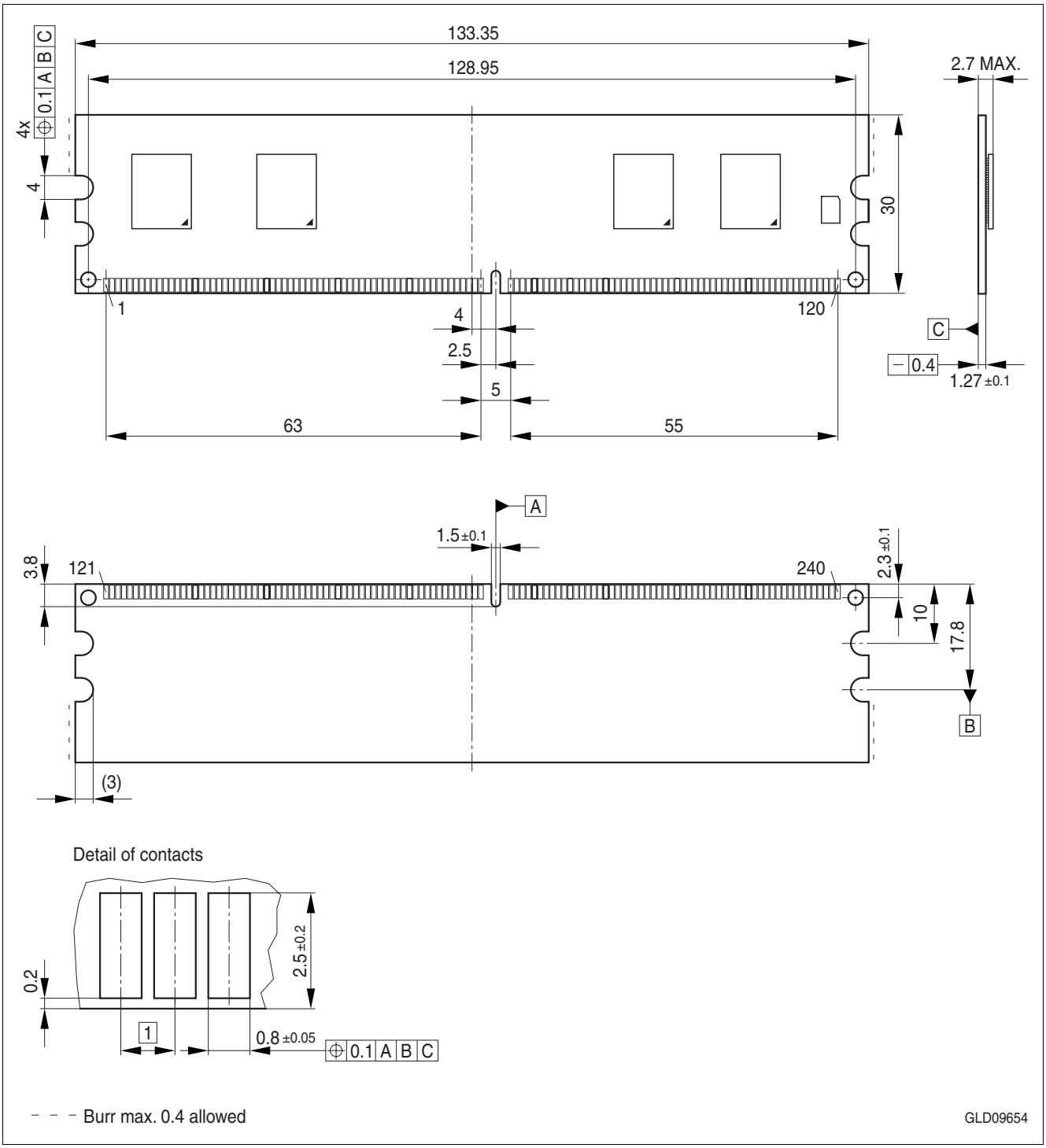

Figure 10 Package Outline L-DIM-240-3

8 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some propriatory coding. Table 31 provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in Table 32 and for components in Table 33.

Table 31 Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	–5	

Table 32 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
5	Raw Card Generation	0 .. 9	look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	look up table
8	Package, Lead-Free Status	A .. Z	look up table
9	Module Type	S	**S**O-DIMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
10	Speed Grade	–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 33 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–3.7	DDR2-533
		–5	DDR2-400
11	N/A for Components		

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