

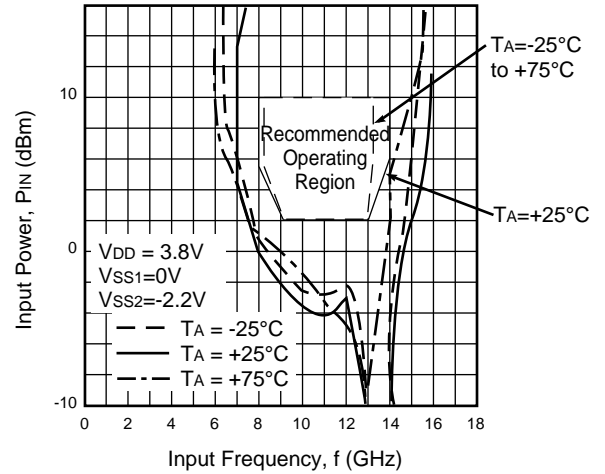
### FEATURES

- **WIDE OPERATING FREQUENCY RANGE:**  
f = 8 to 14 GHz (TA = 25°C)
- **LOW PHASE NOISE**
- **GUARANTEED OPERATING TEMPERATURE RANGE**  
(TA = -25°C to +75°C)

### DESCRIPTION

The UPG506B is a GaAs divide-by-8 prescaler capable of operating up to 14 GHz. It is designed for use in frequency synthesizers of microwave communication systems and measurement equipment. The UPG506B is a dynamic frequency divider and employs BFL (Buffered FET Logic) circuits. The UPG506B is available in a hermetic 8-lead ceramic flat package.

INPUT POWER vs. INPUT FREQUENCY



### ELECTRICAL CHARACTERISTICS (TA = 25°C, VDD = +3.8 V, VSS1 = 0 V, VSS2 = -2.2 V)

PART NUMBER PACKAGE OUTLINE			UPG506B BF08		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I <sub>DD</sub>	Supply Current	mA	70	105	140
I <sub>SS1</sub>	Sink Current <sup>1</sup> I <sub>SS1</sub> = I <sub>DD</sub> - I <sub>SS2</sub>	mA		35	
I <sub>SS2</sub>	Sink Current <sup>1</sup>	mA	44	70	96
f <sub>IN(U)</sub>	Upper Limit of Input Frequency at P <sub>IN</sub> = +6 dBm	GHz	14		
f <sub>IN(L)</sub>	Lower Limit of Input Frequency at P <sub>IN</sub> = +6 dBm	GHz			8
P <sub>IN</sub>	Input Power at f = 9 to 13 GHz	dBm	2.0		10.0
P <sub>OUT</sub>	Output Power at f <sub>IN</sub> = 14 GHz	dBm	0	2.0	
R <sub>TH(CH-C)</sub>	Thermal Resistance (Channel to Case)	°C/W		10.0	

Note:

1. Current is positive into the I<sub>DD</sub> pin and returns through the I<sub>SS1</sub> and I<sub>SS2</sub> pins.

**ELECTRICAL CHARACTERISTICS** ( $T_A = -25^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ ,  $V_{DD} = +3.8\text{ V}$ ,  $V_{SS1} = 0\text{ V}$ ,  $V_{SS2} = -2.2\text{ V}$ )

PART NUMBER PACKAGE OUTLINE			UPG506B BF08		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I <sub>DD</sub>	Supply Current	mA		105	
I <sub>SS1</sub>	Sink Current <sup>1</sup> I <sub>SS1</sub> = I <sub>DD</sub> - I <sub>SS2</sub>	mA		35	
I <sub>SS2</sub>	Sink Current <sup>1</sup>	mA		70	
f <sub>IN(U)</sub>	Upper Limit of Input Frequency at P <sub>IN</sub> = +6 dBm	GHz	13.2		
f <sub>IN(L)</sub>	Lower Limit of Input Frequency at P <sub>IN</sub> = +6 dBm	GHz			8.2
P <sub>IN</sub>	Input Power at f = 9 to 13 GHz	dBm	2.0		10.0
P <sub>OUT</sub>	Output Power at f <sub>IN</sub> = 14 GHz	dBm	-1.0	1.0	

Note:

1. Current is positive into the I<sub>DD</sub> pin and returns through the I<sub>SS1</sub> and I<sub>SS2</sub> pins.

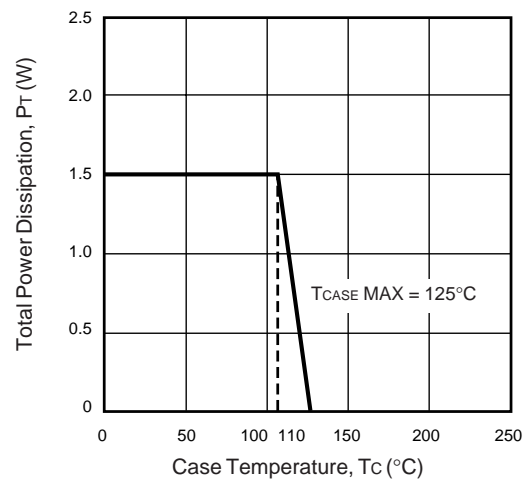
**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>** ( $T_A = 25^{\circ}\text{C}$ )

SYMBOLS	PARAMETERS	UNITS	RATINGS
V <sub>DD</sub> - V <sub>SS1</sub>	Supply Voltage	V	5
V <sub>SS2</sub> - V <sub>SS1</sub>	Supply Current	mA	-5
P <sub>T</sub>	Total Power Dissipation <sup>2</sup>	W	1.5
P <sub>IN</sub>	Input Power Level	dBm	13
T <sub>c</sub>	Case Temperature	°C	-65 to +125
T <sub>STG</sub>	Storage Temperature	°C	-65 to +175

Notes:

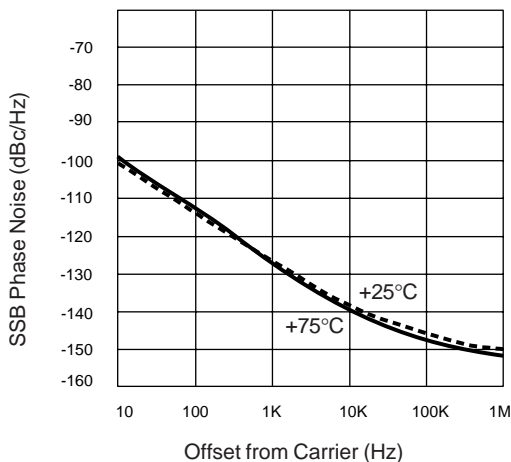
1. Operation in excess of any one of these conditions may result in permanent damage.
2. T<sub>c</sub> ≤ 125°C.

**POWER DERATING CURVES**

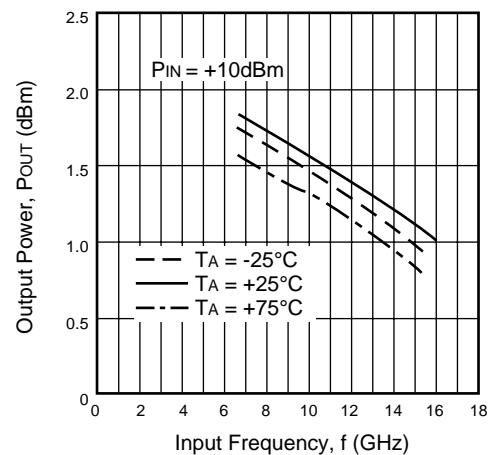


**TYPICAL PERFORMANCE CURVES** ( $T_A = 25^{\circ}\text{C}$ )

**SSB PHASE NOISE vs. OFFSET FROM CARRIER**  
f<sub>IN</sub> = 12.7 GHz

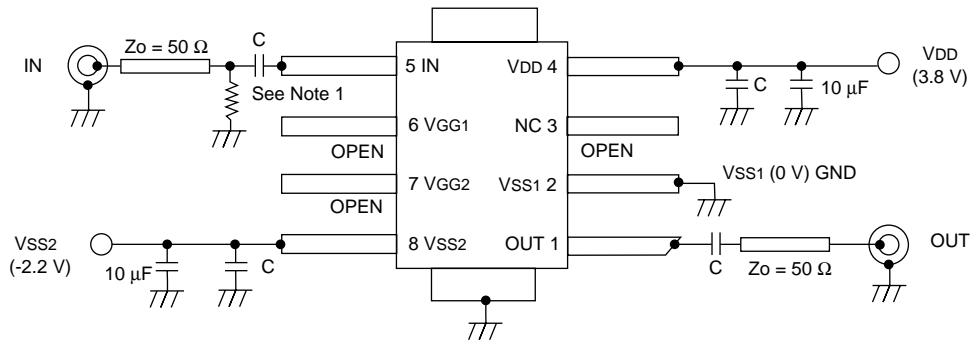


**OUTPUT POWER vs. INPUT FREQUENCY**



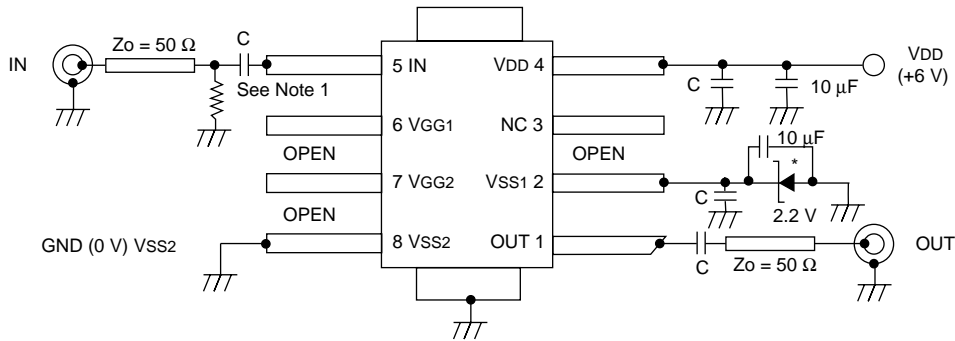
TEST CIRCUITS

CONFIGURATION 1  
2 Bias Supply



VDD = 3.8 V  
VSS1 = 0 V (GND)  
VSS2 = -2.2 V  
C: 1000 - 5000 pF Chip Capacitor

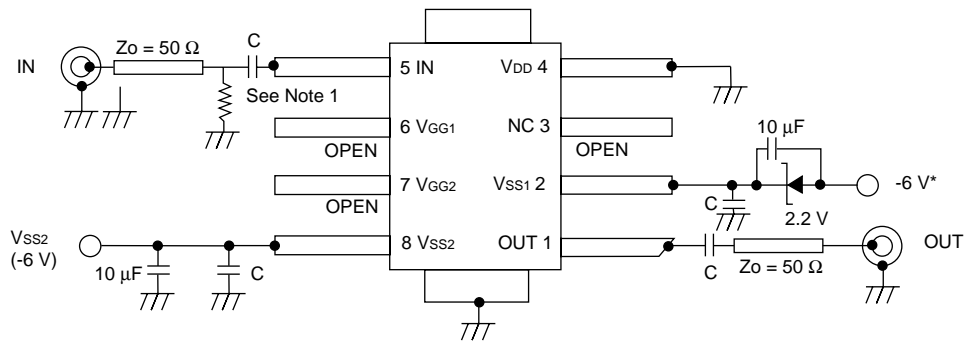
CONFIGURATION 2  
Single Positive Bias Supply



VDD = +6.0 V  
VSS2 = 0 V (GND)  
C: 1000 - 5000 pF Chip Capacitor

\* VSS1 should be connected to GND through a 2.2 V Zener Diode (RD2.2FB or IN3394).

CONFIGURATION 3  
Single Negative Bias Supply



VDD = 0 V (GND)  
VSS2 = -6 V  
C: 1000 - 5000 pF Chip Capacitor

\* For VSS1, the bias voltage of -6.0 should be applied through a 2.2 V Zener Diode (RD2.2FB or IN3394).

Notes:

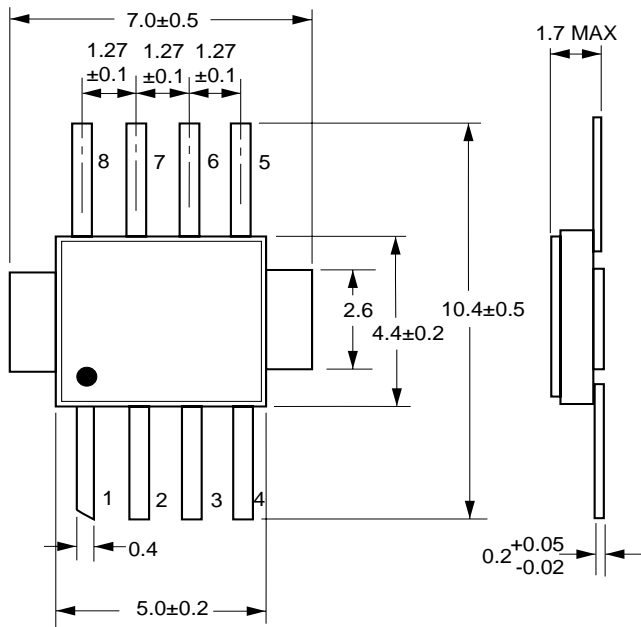
1. Because of the high internal gain and gain compression of the UPG506B, the device is prone to self-oscillation in the absence of an RF input signal. This self-oscillation can be suppressed by either of the following means:

- Add a shunt resistor to the RF input line. Typically a resistor value between 50 and 1000 ohms will suppress the self-oscillation (see the test circuit schematic).
- Apply a negative voltage through a 1000 ohm resistor to the normally open VGG1 connection. Typically voltages between 0 and -9 volts will suppress the self-oscillation.

Both of these approaches will reduce the input sensitivity of the device (by as much as 3 dB for a 50 ohm shunt resistor), but otherwise have no effect on the reliability or electrical characteristics of the device.

**OUTLINE DIMENSIONS** (Units in mm)

**UPG506B  
PACKAGE OUTLINE BFO8**



**LEAD CONNECTIONS**

- |                     |                     |
|---------------------|---------------------|
| 1. OUTPUT           | 5. INPUT            |
| 2. V <sub>SS1</sub> | 6. V <sub>GG1</sub> |
| 3. NC*              | 7. V <sub>GG2</sub> |
| 4. V <sub>DD</sub>  | 8. V <sub>SS2</sub> |

\* No Connection

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