

TMUX110x 5-V, low-leakage-current, 1:1 (SPST) precision switches

1 Features

- Wide supply range: 1.08 V to 5.5 V
- Low leakage current: 5 pA
- Low charge injection: 1.5 pC
- Low on-resistance: 2 Ω
- -40°C to $+125^{\circ}\text{C}$ operating temperature
- [1.8 V Logic compatible](#)
- [Fail-safe logic](#)
- [Rail to rail operation](#)
- [Bidirectional signal path](#)
- Break-before-make switching
- ESD protection HBM: 2000 V

2 Applications

- Ultrasound scanners
- Patient monitoring & diagnostics
- Blood glucose monitors
- Optical networking
- Optical test equipment
- Remote radio units
- Wired networking
- Data acquisition systems
- ATE test equipment
- Factory automation and industrial controls
- Programmable logic controllers (PLC)
- Analog input modules
- SONAR receivers
- Battery monitoring systems

3 Description

The TMUX1101 and TMUX1102 are precision complementary metal-oxide semiconductor (CMOS) single-pole / single-throw (SPST) switches. Wide operating supply of 1.08 V to 5.5 V allows for use in a broad array of applications from medical equipment to industrial systems. The devices supports bidirectional analog and digital signals on the source (S) and drain (D) pins ranging from GND to V_{DD} .

The switch of the TMUX1101 is turned on with a Logic 1 on the select pin, while a Logic 0 is required to turn on switch in the TMUX1102.

The TMUX110x devices are part of the precision switches and multiplexers family. These devices have very low on and off leakage currents and low charge injection, allowing them to be used in high precision measurement applications. A low supply current of 3 nA and small package options enable use in portable applications.

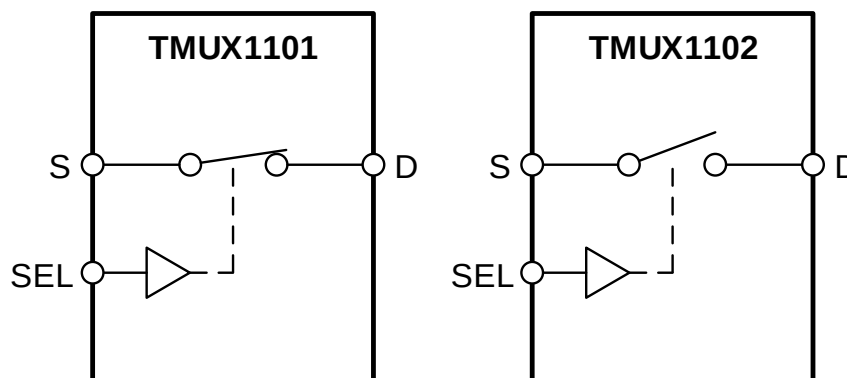
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX1101	SC70 (5) (DCK)	2.00 mm × 1.25 mm
TMUX1102 ⁽²⁾	SOT-23 (5) (DBV)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Product Preview

TMUX110x Block Diagrams



ALL SWITCHES SHOWN FOR A LOGIC 1 INPUT



Table of Contents

1	Features	1	9	Detailed Description	17
2	Applications	1	9.1	Functional Block Diagram	17
3	Description	1	9.2	Feature Description	17
4	Revision History	2	9.3	Device Functional Modes	18
5	Device Comparison Table	3	9.4	Truth Tables	18
6	Pin Configuration and Functions	3	10	Application and Implementation	19
7	Specifications	4	10.1	Application Information	19
7.1	Absolute Maximum Ratings	4	10.2	Typical Application	19
7.2	ESD Ratings	4	10.3	Design Requirements	20
7.3	Recommended Operating Conditions	4	10.4	Detailed Design Procedure	20
7.4	Thermal Information	4	11	Power Supply Recommendations	21
7.5	Electrical Characteristics ($V_{DD} = 5\text{ V} \pm 10\%$)	5	12	Layout	21
7.6	Electrical Characteristics ($V_{DD} = 3.3\text{ V} \pm 10\%$)	7	12.1	Layout Guidelines	21
7.7	Electrical Characteristics ($V_{DD} = 1.8\text{ V} \pm 10\%$)	9	12.2	Layout Example	22
7.8	Electrical Characteristics ($V_{DD} = 1.2\text{ V} \pm 10\%$)	11	13	Device and Documentation Support	23
8	Parameter Measurement Information	13	13.1	Documentation Support	23
8.1	On-resistance	13	13.2	Related Links	23
8.2	Off-leakage current	13	13.3	Receiving Notification of Documentation Updates	23
8.3	On-leakage current	14	13.4	Community Resources	23
8.4	Transition time	14	13.5	Trademarks	23
8.5	Charge injection	15	13.6	Electrostatic Discharge Caution	23
8.6	Off isolation	15	13.7	Glossary	23
8.7	Bandwidth	16	14	Mechanical, Packaging, and Orderable Information	24

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

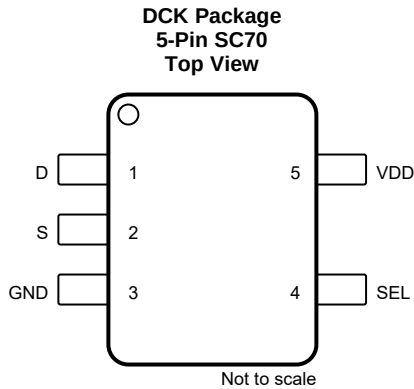
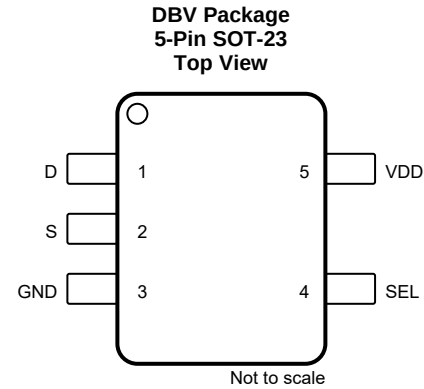
DATE	REVISION	NOTES
March 2019	*	Initial release.

5 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX1101	Low-Leakage-Current, Precision, 1:1 (SPST) Switch (Normally Open)
TMUX1102 ⁽¹⁾	Low-Leakage-Current, Precision, 1:1 (SPST) Switch (Normally Closed)

(1) Product Preview

6 Pin Configuration and Functions



Product Preview

Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
D	1	I/O	Drain pin. Can be an input or output.
S	2	I/O	Source pin. Can be an input or output.
GND	3	P	Ground (0 V) reference
SEL	4	I	Logic control input. Controls the switch state as shown in Truth Tables .
VDD	5	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{DD} and GND.

(1) I = input, O = output, I/O = input and output, P = power

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾ ⁽³⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage	−0.5	6	V
V _{SEL}	Logic control input pin voltage (SEL)	−0.5	6	V
I _{SEL}	Logic control input pin current (SEL)	−30	30	mA
V _S or V _D	Source or drain voltage (S, D)	−0.5	V _{DD} +0.5	V
I _S or I _D (CONT)	Source or drain continuous current (S, D)	−30	30	mA
T _{stg}	Storage temperature	−65	150	°C
T _J	Junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	1.08		5.5	V
V _S or V _D	Signal path input/output voltage (source or drain pin) (S, D)	0		V _{DD}	V
V _{SEL}	Logic control input pin voltage (SEL)	0		5.5	V
T _A	Ambient temperature	−40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX1101 / TMUX1102		UNIT
		DCK (SC70)	DBV (SOT-23)	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	348.5	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	238.3	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	205.7	TBD	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	141.4	TBD	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	204.7	TBD	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	TBD	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics ($V_{DD} = 5\text{ V} \pm 10\%$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	2		4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
ΔR _{ON}	On-resistance matching between channels	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	0.13			Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
R _{ON} FLAT	On-resistance flatness	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	0.85			Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.6	Ω
I _{S(OFF)}	Source off leakage current ⁽¹⁾	V _{DD} = 5 V Switch Off V _D = 4.5 V / 1.5 V V _S = 1.5 V / 4.5 V Refer to Off-leakage current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	V _{DD} = 5 V Switch Off V _D = 4.5 V / 1.5 V V _S = 1.5 V / 4.5 V Refer to Off-leakage current	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
I _{D(ON)} I _{S(ON)}	Channel on leakage current	V _{DD} = 5 V Switch On V _D = V _S = 4.5 V / 1.5 V Refer to On-leakage current	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V _{IH}	Input logic high		–40°C to +125°C	1.49		5.5	V
V _{IL}	Input logic low		–40°C to +125°C	0		0.87	V
I _{IH} I _{IL}	Input leakage current		25°C	±0.005			μA
I _{IH} I _{IL}	Input leakage current		–40°C to +125°C			±0.05	μA
C _{IN}	Logic input capacitance		25°C	1			pF
C _{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I _{DD}	V _{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C	0.003			μA
			–40°C to +125°C			1	μA

(1) When V_S is 4.5 V, V_D is 1.5 V, and vice versa.

Electrical Characteristics ($V_{DD} = 5\text{ V} \pm 10\%$) (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	$V_S = 3\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Transition time	25°C		12		ns
			–40°C to +85°C			17	ns
			–40°C to +125°C			18	ns
Q_C	Charge Injection	$V_S = 1\text{ V}$ $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ Refer to Charge injection	25°C		1.5		pC
O_{ISO}	Off Isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Off isolation	25°C		–62		dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Off isolation	25°C		–40		dB
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	$f = 1\text{ MHz}$	25°C		6		pF
C_{DOFF}	Drain off capacitance	$f = 1\text{ MHz}$	25°C		10		pF
C_{SON} C_{DON}	On capacitance	$f = 1\text{ MHz}$	25°C		18		pF

7.6 Electrical Characteristics ($V_{DD} = 3.3 \text{ V} \pm 10 \%$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	3.7		8.8	Ω
			–40°C to +85°C			9.5	Ω
			–40°C to +125°C			9.8	Ω
ΔR _{ON}	On-resistance matching between channels	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	0.13			Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
R _{ON} FLAT	On-resistance flatness	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	1.9			Ω
			–40°C to +85°C			2	Ω
			–40°C to +125°C			2.2	Ω
I _{S(OFF)}	Source off leakage current ⁽¹⁾	V _{DD} = 3.3 V Switch Off V _D = 3 V / 1 V V _S = 1 V / 3 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	V _{DD} = 3.3 V Switch Off V _D = 3 V / 1 V V _S = 1 V / 3 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
I _{D(ON)} I _{S(ON)}	Channel on leakage current	V _{DD} = 3.3 V Switch On V _D = V _S = 3 V / 1 V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V _{IH}	Input logic high		–40°C to +125°C	1.35		5.5	V
V _{IL}	Input logic low		–40°C to +125°C	0		0.8	V
I _{IH} I _{IL}	Input leakage current		25°C	±0.005			μA
I _{IH} I _{IL}	Input leakage current		–40°C to +125°C			±0.05	μA
C _{IN}	Logic input capacitance		25°C	1			pF
C _{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I _{DD}	V _{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C	0.002			μA
			–40°C to +125°C			0.65	μA

(1) When V_S is 3 V, V_D is 1 V, and vice versa.

Electrical Characteristics ($V_{DD} = 3.3 \text{ V} \pm 10 \%$) (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	$V_S = 2 \text{ V}$ $R_L = 200 \, \Omega$, $C_L = 15 \text{ pF}$ Refer to Transition time	25°C		14		ns
			-40°C to $+85^\circ\text{C}$			20	ns
			-40°C to $+125^\circ\text{C}$			22	ns
Q_C	Charge Injection	$V_S = 1 \text{ V}$ $R_S = 0 \, \Omega$, $C_L = 1 \text{ nF}$ Refer to Charge injection	25°C		–1.5		pC
O_{ISO}	Off Isolation	$R_L = 50 \, \Omega$, $C_L = 5 \text{ pF}$ $f = 1 \text{ MHz}$ Refer to Off isolation	25°C		–62		dB
		$R_L = 50 \, \Omega$, $C_L = 5 \text{ pF}$ $f = 10 \text{ MHz}$ Refer to Off isolation	25°C		–40		dB
BW	Bandwidth	$R_L = 50 \, \Omega$, $C_L = 5 \text{ pF}$ Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	$f = 1 \text{ MHz}$	25°C		6		pF
C_{DOFF}	Drain off capacitance	$f = 1 \text{ MHz}$	25°C		10		pF
C_{SON} C_{DON}	On capacitance	$f = 1 \text{ MHz}$	25°C		18		pF

7.7 Electrical Characteristics ($V_{DD} = 1.8 \text{ V} \pm 10 \%$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	40			Ω
			–40°C to +85°C	80			Ω
			–40°C to +125°C	80			Ω
ΔR _{ON}	On-resistance matching between channels	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	0.4			Ω
			–40°C to +85°C	1.5			Ω
			–40°C to +125°C	1.5			Ω
I _{S(OFF)}	Source off leakage current ⁽¹⁾	V _{DD} = 1.98 V Switch Off V _D = 1.62 V / 1 V V _S = 1 V / 1.62 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	V _{DD} = 1.98 V Switch Off V _D = 1.62 V / 1 V V _S = 1 V / 1.62 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
I _{D(ON)} I _{S(ON)}	Channel on leakage current	V _{DD} = 1.98 V Switch On V _D = V _S = 1.62 V / 1 V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V _{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V _{IL}	Input logic low		–40°C to +125°C	0		0.68	V
I _{IH} I _{IL}	Input leakage current		25°C	±0.005			μA
I _{IH} I _{IL}	Input leakage current		–40°C to +125°C	±0.05			μA
C _{IN}	Logic input capacitance		25°C	1			pF
C _{IN}	Logic input capacitance		–40°C to +125°C	2			pF
POWER SUPPLY							
I _{DD}	V _{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C	0.001			μA
			–40°C to +125°C	0.45			μA

(1) When V_S is 1.62 V, V_D is 1 V, and vice versa.

Electrical Characteristics ($V_{DD} = 1.8 \text{ V} \pm 10 \%$) (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	$V_S = 1 \text{ V}$ $R_L = 200 \, \Omega$, $C_L = 15 \text{ pF}$ Refer to Transition time	25°C		25		ns
			-40°C to $+85^\circ\text{C}$			44	ns
			-40°C to $+125^\circ\text{C}$			44	ns
Q_C	Charge Injection	$V_S = 1 \text{ V}$ $R_S = 0 \, \Omega$, $C_L = 1 \text{ nF}$ Refer to Charge injection	25°C		–0.5		pC
O_{ISO}	Off Isolation	$R_L = 50 \, \Omega$, $C_L = 5 \text{ pF}$ $f = 1 \text{ MHz}$ Refer to Off isolation	25°C		–62		dB
		$R_L = 50 \, \Omega$, $C_L = 5 \text{ pF}$ $f = 10 \text{ MHz}$ Refer to Off isolation	25°C		–40		dB
BW	Bandwidth	$R_L = 50 \, \Omega$, $C_L = 5 \text{ pF}$ Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	$f = 1 \text{ MHz}$	25°C		6		pF
C_{DOFF}	Drain off capacitance	$f = 1 \text{ MHz}$	25°C		10		pF
C_{SON} C_{DON}	On capacitance	$f = 1 \text{ MHz}$	25°C		18		pF

7.8 Electrical Characteristics ($V_{DD} = 1.2 \text{ V} \pm 10 \%$)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R _{ON}	On-resistance	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	70			Ω
			–40°C to +85°C	105			Ω
			–40°C to +125°C	105			Ω
ΔR _{ON}	On-resistance matching between channels	V _S = 0 V to V _{DD} I _{SD} = 10 mA Refer to On-resistance	25°C	0.4			Ω
			–40°C to +85°C	1.5			Ω
			–40°C to +125°C	1.5			Ω
I _{S(OFF)}	Source off leakage current ⁽¹⁾	V _{DD} = 1.32 V Switch Off V _D = 1 V / 0.8 V V _S = 0.8 V / 1 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	V _{DD} = 1.32 V Switch Off V _D = 1 V / 0.8 V V _S = 0.8 V / 1 V Refer to Off-leakage current	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.2		0.2	nA
			–40°C to +125°C	–0.9		0.9	nA
I _{D(ON)} I _{S(ON)}	Channel on leakage current	V _{DD} = 1.32 V Switch On V _D = V _S = 1 V / 0.8 V Refer to On-leakage current	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SEL)							
V _{IH}	Input logic high		–40°C to +125°C	0.96		5.5	V
V _{IL}	Input logic low		–40°C to +125°C	0		0.36	V
I _{IH} I _{IL}	Input leakage current		25°C	±0.005			μA
I _{IH} I _{IL}	Input leakage current		–40°C to +125°C	±0.05			μA
C _{IN}	Logic input capacitance		25°C	1			pF
C _{IN}	Logic input capacitance		–40°C to +125°C	2			pF
POWER SUPPLY							
I _{DD}	V _{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C	0.001			μA
			–40°C to +125°C	0.38			μA

(1) When V_S is 1 V, V_D is 0.8 V, and vice versa.

Electrical Characteristics ($V_{DD} = 1.2\text{ V} \pm 10\%$) (continued)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time from control input	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Transition time	25°C		55		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns
Q_C	Charge Injection	$V_S = 1\text{ V}$ $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ Refer to Charge injection	25°C		–0.5		pC
O_{ISO}	Off Isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Off isolation	25°C		–62		dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Off isolation	25°C		–40		dB
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Bandwidth	25°C		300		MHz
C_{SOFF}	Source off capacitance	$f = 1\text{ MHz}$	25°C		6		pF
C_{DOFF}	Drain off capacitance	$f = 1\text{ MHz}$	25°C		10		pF
C_{SON} C_{DON}	On capacitance	$f = 1\text{ MHz}$	25°C		18		pF

8 Parameter Measurement Information

8.1 On-resistance

The on-resistance of a device is the ohmic resistance between the source (S) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 1. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

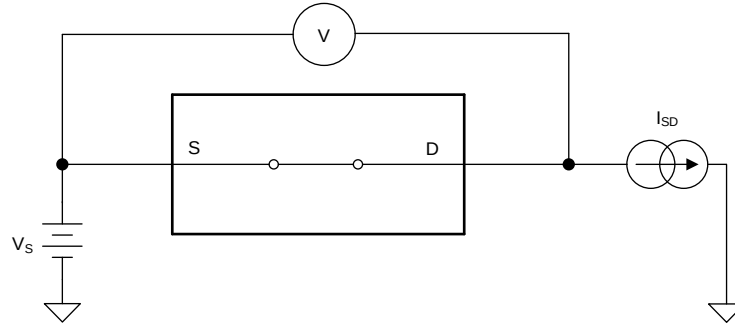


Figure 1. On-Resistance measurement setup

8.2 Off-leakage current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 2.

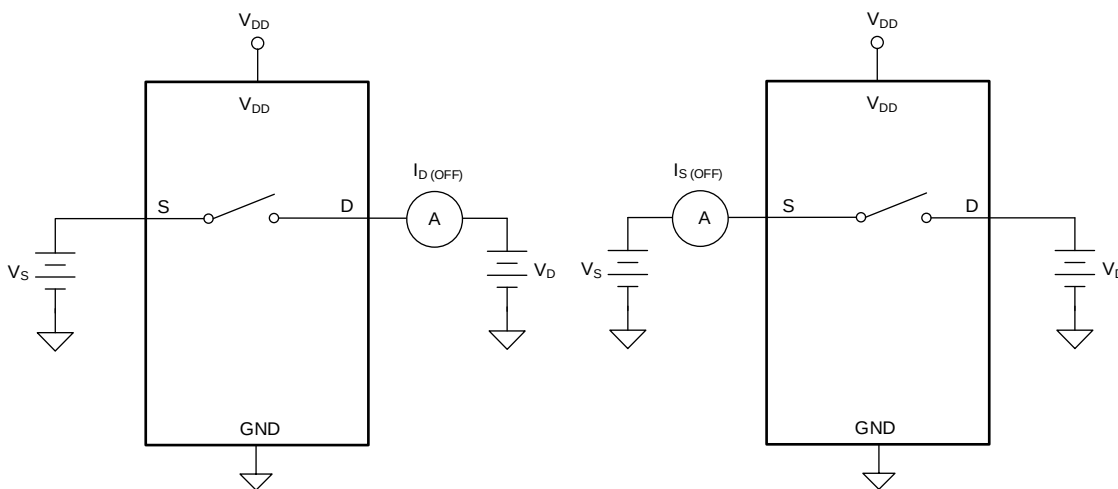


Figure 2. Off-leakage measurement setup

8.3 On-leakage current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

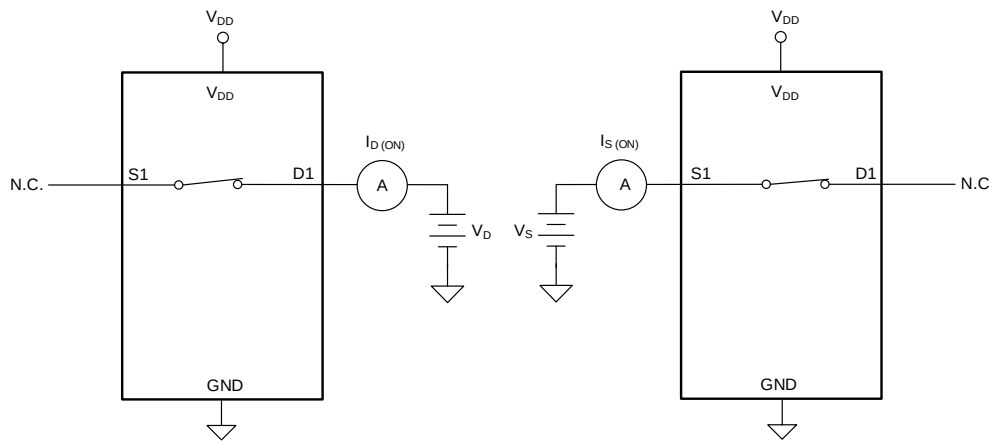


Figure 3. On-leakage measurement setup

8.4 Transition time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 4 shows the setup used to measure transition time, denoted by the symbol $t_{\text{TRANSITION}}$.

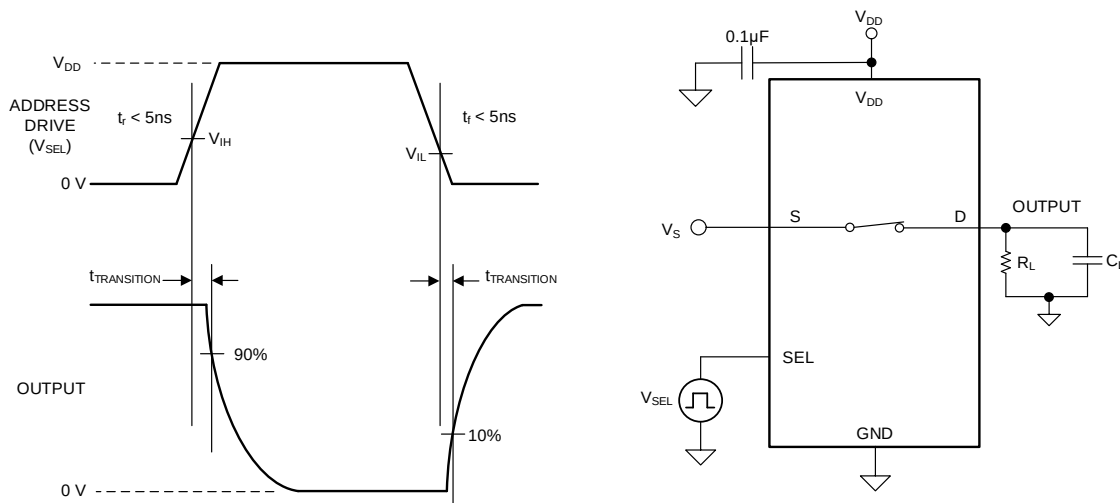


Figure 4. Transition-time measurement setup

8.5 Charge injection

The TMUX110x devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C . Figure 5 shows the setup used to measure charge injection from source (S) to drain (D).

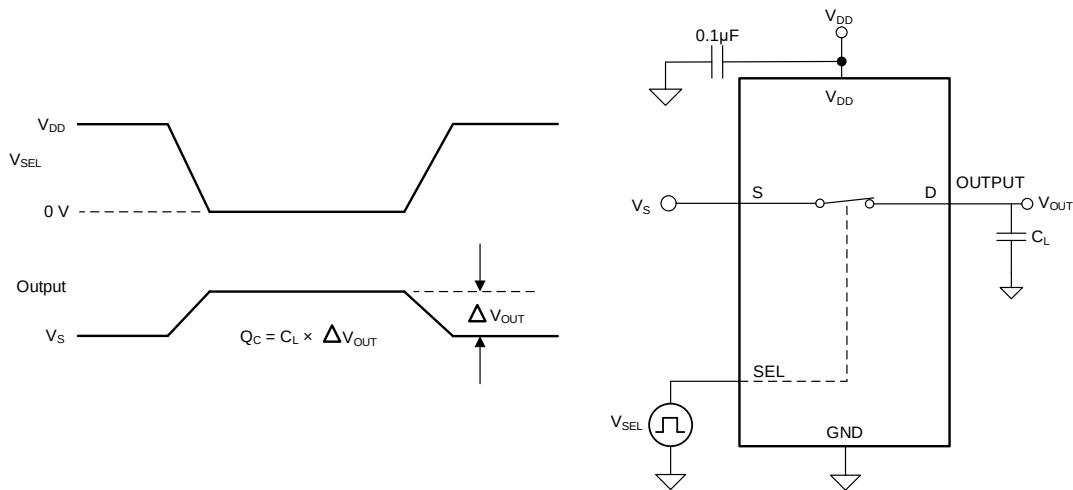


Figure 5. Charge-injection measurement setup

8.6 Off isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (S) of an off-channel. The characteristic impedance, Z_0 , for the measurement is 50 Ω. Figure 6 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

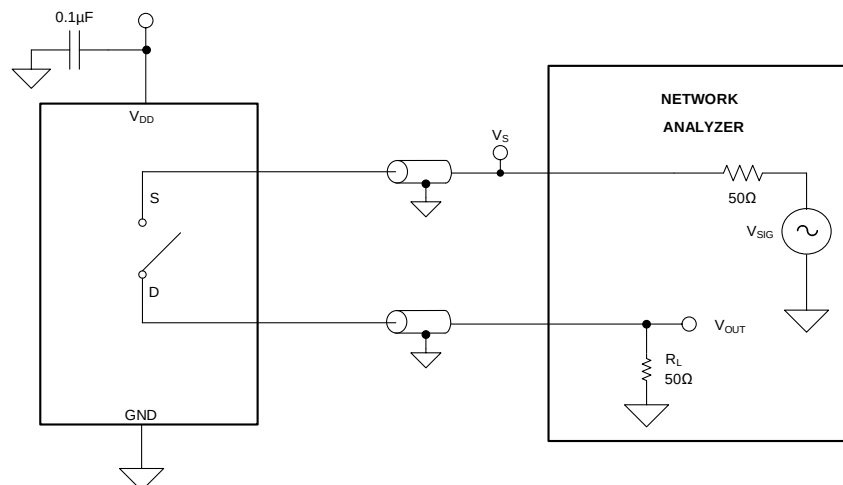


Figure 6. Off isolation measurement setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_S} \right)$$

(1)

8.7 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (S) of an on-channel, and the output is measured at the drain pin (D) of the device. The characteristic impedance, Z_0 , for the measurement is 50 Ω . [Figure 7](#) shows the setup used to measure bandwidth.

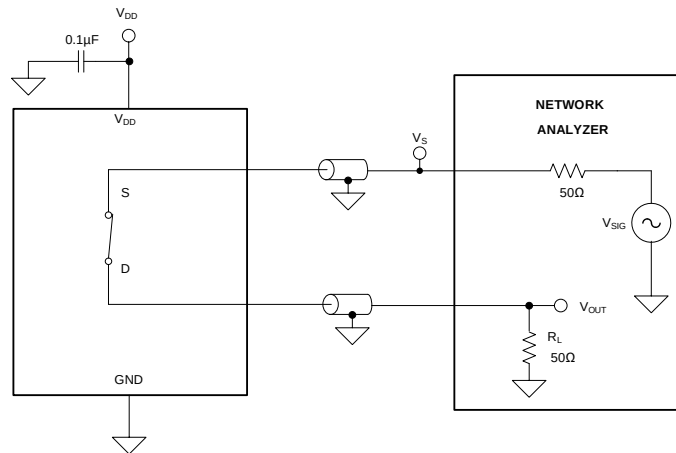


Figure 7. Bandwidth measurement setup

9 Detailed Description

9.1 Functional Block Diagram

The TMUX1101 and TMUX1102 are 1:1 (SPST) switches. The devices have a selectable single-pole/ single-throw switch that is turned on or turned off based on the state of the select pin.

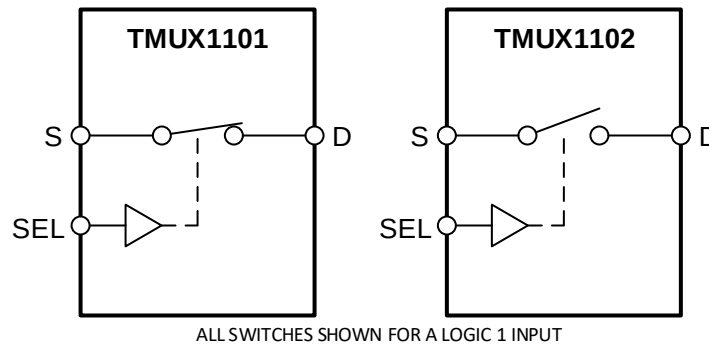


Figure 8. TMUX110x Functional Block Diagram

9.2 Feature Description

9.2.1 Bidirectional operation

The TMUX110x conducts equally well from source (S) to drain (D) or from drain (D) to source (S). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

9.2.2 Rail to rail operation

The valid signal path input/output voltage for TMUX110x ranges from GND to V_{DD} .

9.2.3 1.8 V Logic compatible inputs

The TMUX110x have 1.8-V logic compatible control for the logic control input. The logic input threshold scales with supply but still provides 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allows the TMUX110x to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to [Simplifying Design with 1.8 V logic Muxes and Switches](#)

9.2.4 Fail-safe logic

The TMUX110x supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX110x to be ramped to 5.5 V while $V_{DD} = 0$ V. Additionally, the feature enables operation of the TMUX110x with $V_{DD} = 1.2$ V while allowing the select pins to interface with a logic level of another device up to 5.5 V.

Feature Description (continued)

9.2.5 Ultra-low charge injection

The TMUX110x have a transmission gate topology, as shown in [Figure 9](#). Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

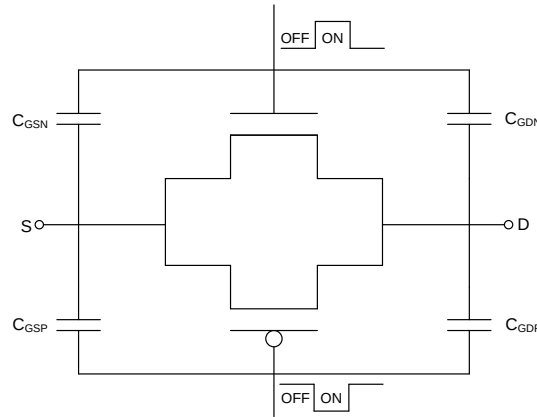


Figure 9. Transmission gate topology

9.3 Device Functional Modes

The TMUX110x devices have a selectable single-pole / single-throw switch that is turned on or turned off based on the state of the corresponding select pin. The control pin can be as high as 5.5 V.

9.4 Truth Tables

[Table 1](#) and [Table 2](#) show the truth tables for the TMUX1101 and TMUX1102 respectively.

Table 1. TMUX1101 Truth table

SEL	SWITCH STATE
0	OFF
1	ON

Table 2. TMUX1102 Truth table

SEL	SWITCH STATE
0	ON
1	OFF

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TMUX11xx family offers ultra-low input/output leakage currents and low charge injection. These devices operate up to 5.5 V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX110x have a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

10.2 Typical Application

Switches and multiplexers are commonly used in the feedback path of amplifier circuits to provide configurable gain control. By using various resistor values on the switch path the TMUX110x allows the system to have multiple gain settings. An external resistor ensures the amplifier isn't operating in an open loop configuration. A transimpedance amplifier (TIA) for photodiode inputs is a common circuit that requires gain control using a switch to convert the output current of the photodiode into a voltage for the MCU or processor. The amount of light present during a photodiode measurement is dependent on the time of day and available light source, an external switch such as the TMUX110x can be utilized to increase the gain when a smaller photodiode current is present. The leakage current, capacitance, and charge injection performance of the TMUX110x are key specifications to evaluate when selecting a device for gain control.

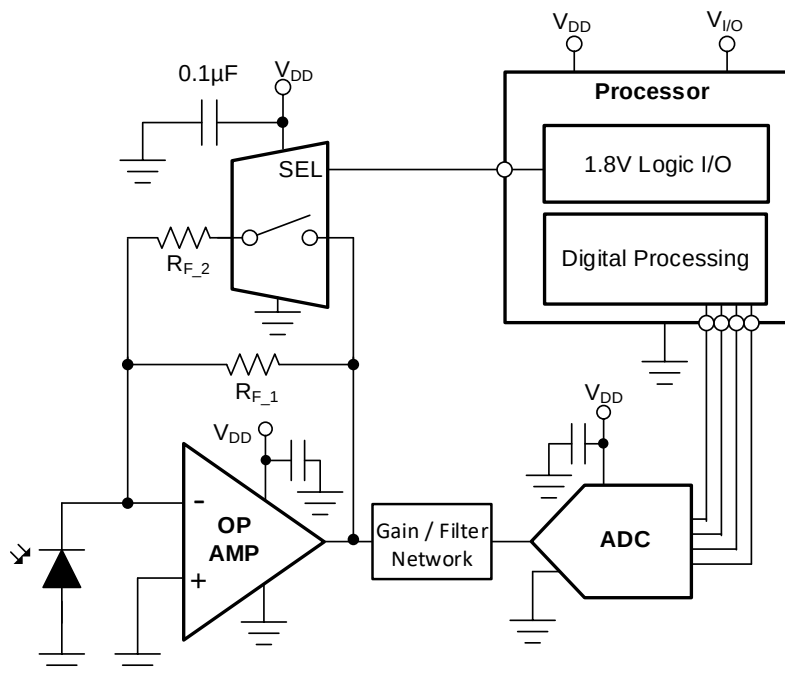


Figure 10. Configurable Gain Setting of a TIA circuit

10.3 Design Requirements

For this design example, use the parameters listed in [Table 3](#).

Table 3. Design parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3 V
Input / Output signal range	0 μ A to 10 μ A
Control logic thresholds	1.8 V compatible

10.4 Detailed Design Procedure

The TMUX110x devices can be operated without any external components except for the supply decoupling capacitors. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX110x including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. The max continuous current can be 30 mA.

Photodiodes commonly have a current output that ranges from a few hundred picoamps to tens of microamps based on the amount of light being absorbed. The TMUX110x have a typical On-leakage current of less than 10 pA which would lead to an accuracy well within 1% of a full scale 10 μ A signal. The low ON and OFF capacitance of the TMUX110x improves system stability by minimizing the total capacitance on the output of the amplifier. Lower capacitance leads to less overshoot and ringing in the system which can cause the amplifier circuit to go unstable if the phase margin is not at least 45°. Refer to [Improve Stability Issues with Low \$C_{ON}\$ Multiplexers](#) for more information on calculating the phase margin vs. percent overshoot.

11 Power Supply Recommendations

The TMUX110x operate across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

12 Layout

12.1 Layout Guidelines

12.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

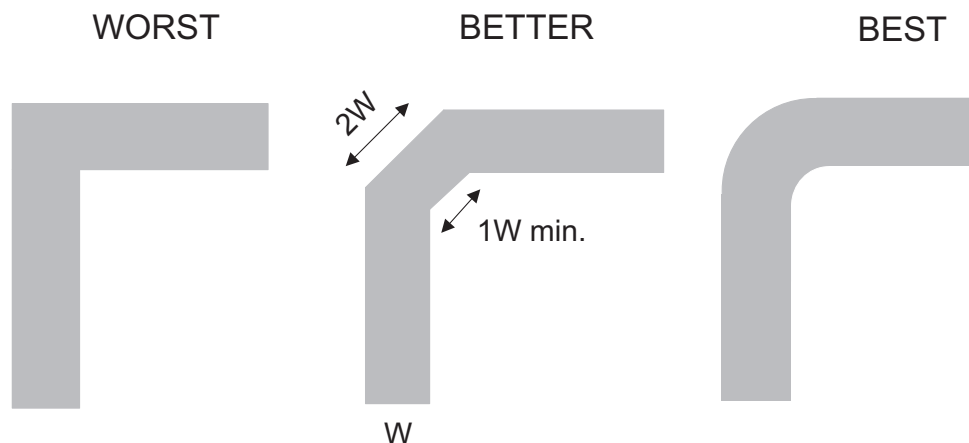


Figure 11. Trace example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Layout Guidelines (continued)

Figure 12 illustrates an example of a PCB layout with the TMUX110x. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1- μ F capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

12.2 Layout Example

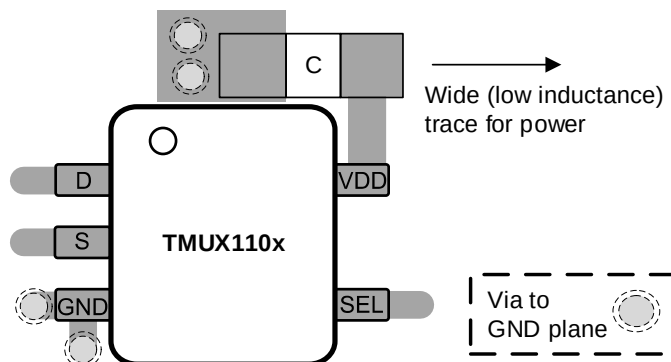


Figure 12. TMUX110x Layout example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

Texas Instruments, [Improve Stability Issues with Low CON Multiplexers](#).

Texas Instruments, [Simplifying Design with 1.8 V logic Muxes and Switches](#).

Texas Instruments, [True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit](#).

Texas Instruments, [Eliminate Power Sequencing with Powered-off Protection Signal Switches](#).

Texas Instruments, [System-Level Protection for High-Voltage Analog Multiplexers](#).

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TMUX1101	Click here	Click here	Click here	Click here	Click here
TMUX1102	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX1101DCKR	ACTIVE	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TMUX1101DBVR	PREVIEW	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TMUX1101DCKR	PREVIEW	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125		
TMUX1102DBVR	PREVIEW	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		
TMUX1102DCKR	PREVIEW	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

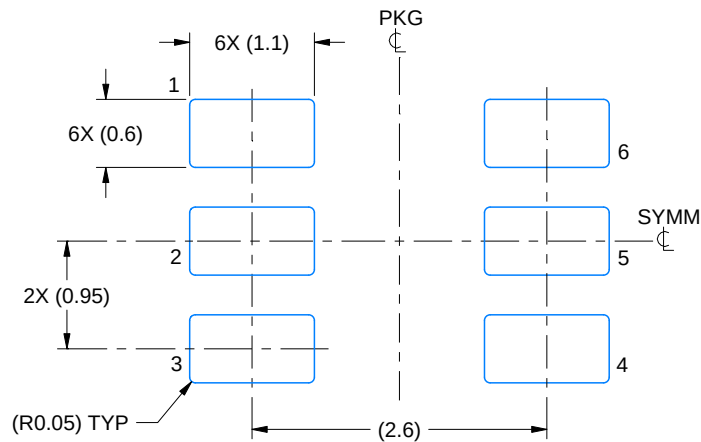
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EXAMPLE BOARD LAYOUT

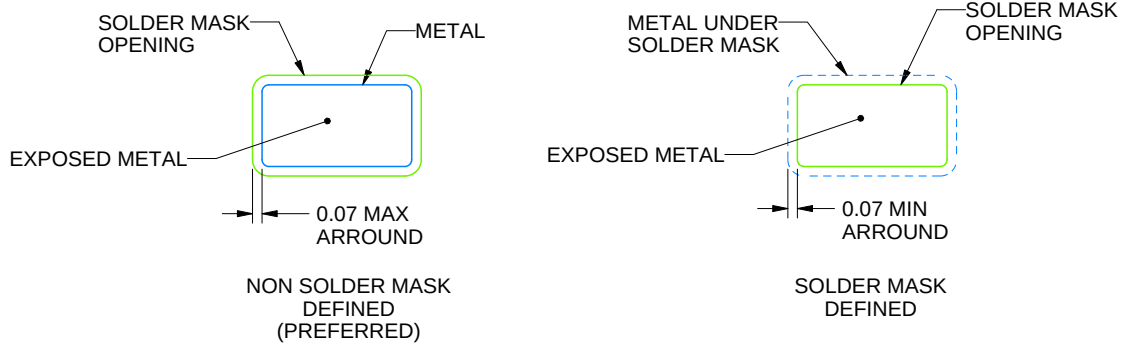
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

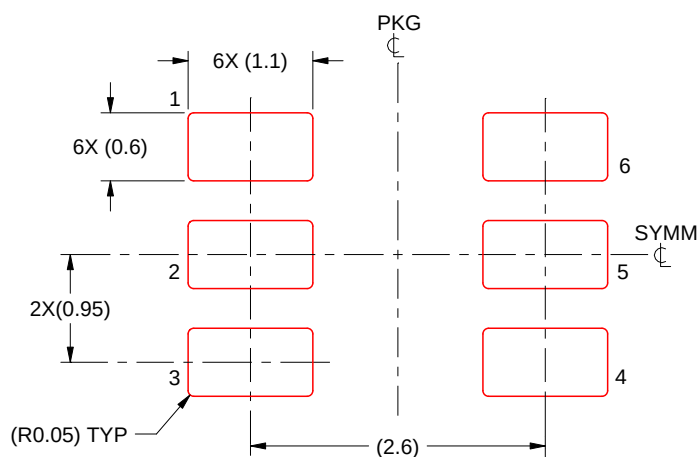
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

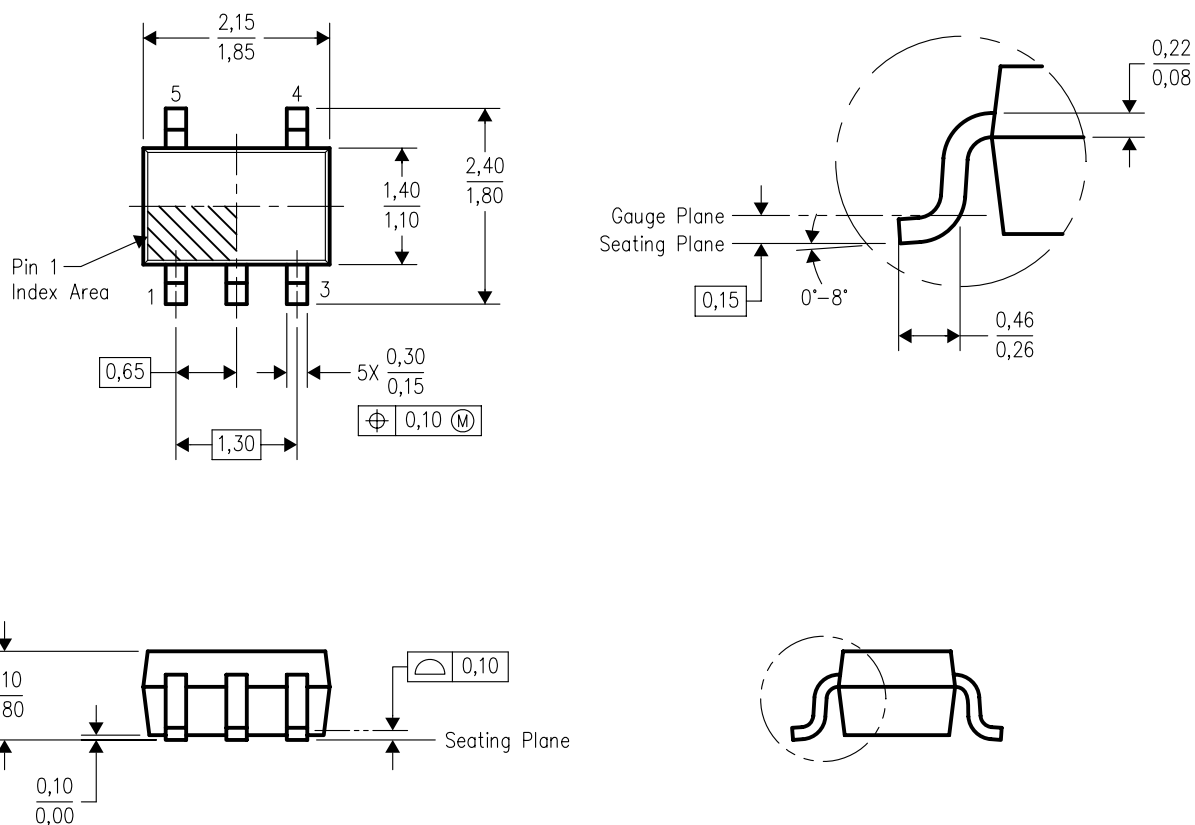
4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated