FAIRCHILD SEMICONDUCTOR™

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USB1T20
Universal Serial Bus Transceiver

General Description

The USB1T20 is a generic USB 2.0 compliant transceiver. Using a single voltage supply, the USB1T20 provides an ideal USB interface solution for any electronic device able to supply 3.0V to 3.6V. It is designed to allow 5.0V or 3.3V programmable and standard logic to interface with the physical layer of the Universal Serial Bus. It is capable of transmitting and receiving serial data at both full speed (12Mbit/s) and low speed (1.5Mbit/s) data rates.

Packaged in industry standard TSSOP and Fairchild's ultra-small 2.5mm x 2.5mm MLP package, the USB1T20 is ideal for ultra-portable electronics and other space constrained applications.

Features

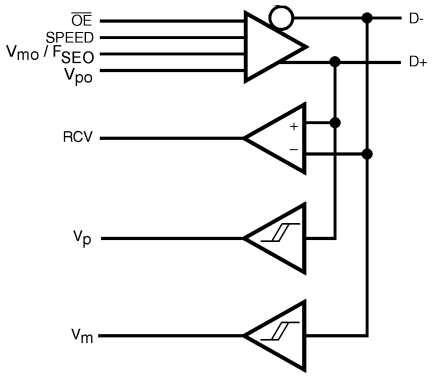
- Complies with Universal Serial Bus specification 2.0 for FS/LS applications
- Utilizes digital inputs and outputs to transmit and receive USB cable data
- Supports 12Mbit/s "Full Speed" and 1.5Mbit/s "Low Speed" serial data transmission
- Supports single-ended and differential data interface as function of MODE
- Single 3.3V supply
- ESD Performance: Human Body Model
  > 9.5 kV on D–, D+ pins only
  > 4 kV on all other pins
- Space saving 14-terminal MLP package

Ordering Code:

Order Number	Package Number	Package Description
USB1T20MPX (Preliminary)	MLP14D	14-Terminal Molded Leadless Package (MLP), 2.5mm Square
USB1T20MTC (Note 1)	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

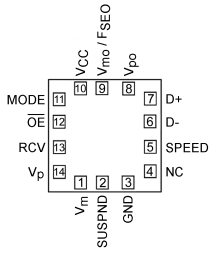
Note 1: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



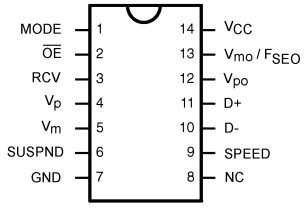
Connection Diagrams

Terminal Assignments for MLP (Preliminary)



(Top View)

Pin Assignments for TSSOP



(Top View)

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Terminal and Pin Descriptions

Terminal or Pin Name	Terminal or Pin Number		I/O	Description
	MLP14D	MTC14		
RCV	13	3	O	Receive data. CMOS level output for USB differential input
$\overline{OE}$	12	2	I	Output Enable. Active LOW, enables the transceiver to transmit data on the bus. When not active the transceiver is in receive mode.
MODE	11	1	I	Mode. When left unconnected, a weak pull-up transistor pulls it to V_{CC} and in this GND, the V_{mo}/F_{SEO} pin takes the function of F_{SEO} (Force SEO).
V_{po}, V_{mo} / F_{SEO}	8, 9	12, 13	I	Inputs to differential driver. (Outputs from SIE).

MODE	V_{po}	V_{mo}/F_{SEO}	RESULT
0	0	0	Logic “0”
	0	1	$\overline{SE0}$
	1	0	Logic “1”
	1	1	$\overline{SE0}$
1	0	0	$\overline{SE0}$
	0	1	Logic “0”
	1	0	Logic “1”
	1	1	Illegal code

V_p, V_m	14, 1	4, 5	O	Gated version of D– and D+. Outputs are logic “0” and logic “1”. Used to detect single ended zero ($\overline{SE0}$), error conditions, and interconnect speed. (Input to SIE).

V_p	V_m	RESULT
0	0	$\overline{SE0}$
0	1	Low Speed
1	0	Full Speed
1	1	Error

D+, D–	7, 6	11, 10	AI/O	Data+, Data–. Differential data bus conforming to the Universal Serial Bus standard.
SUSPND	2	6	I	Suspend. Enables a low power state while the USB bus is inactive. While the SUSPND pin is active it will drive the RCV pin to a logic “0” state. Both D+ and D– are 3-STATE.
SPEED	5	9	I	Edge rate control. Logic “1” operates at edge rates for “full speed”. Logic “0” operates edge rates for “low speed”.
V_{CC}	10	14	—	3.0V to 3.6V power supply
GND	3	7	—	Ground reference
NC	4	8		No Connect

Functional Truth Table

Input					I/O		Outputs			
Mode	V_{po}	V_{mo}/F_{SEO}	$\overline{OE}$	SUSPND	D+	D–	RCV	V_p	V_m	Result
0	0	0	0	0	0	1	0	0	1	Logic 0
0	0	1	0	0	0	0	U	0	0	$\overline{SE0}$
0	1	0	0	0	1	0	1	1	0	Logic 1
0	1	1	0	0	0	0	U	0	0	$\overline{SE0}$
1	0	0	0	0	0	0	U	0	0	$\overline{SE0}$
1	0	1	0	0	0	1	0	0	1	Logic 0
1	1	0	0	0	1	0	1	1	0	Logic 1
1	1	1	0	0	1	1	U	U	U	Illegal Code
X	X	X	1	0	Z	Z	U	U	U	D+/D– Hi-Z
X	X	X	1	1	Z	Z	U	U	U	D+/D– Hi-Z

X = Don't Care Z = 3-STATE U = Undefined State

Absolute Maximum Ratings(Note 2)

DC Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I < 0$	−50 mA
Input Voltage (V_I)	
(Note 3)	−0.5V to +5.5V
Input Voltage ($V_{I/O}$)	−0.5V to V_{CC} + 0.5V
Output Diode Current (I_{OK})	
$V_O > V_{CC}$ or $V_O < 0$	±50 mA
Output Voltage (V_O)	
(Note 3)	−0.5V to V_{CC} + 0.5V
Output Source or Sink Current (I_O)	
V_p.V_m, RCV Pins	
V_O = 0V to V_{CC}	±15 mA
Output Source or Sink Current (I_O)	
D+/D− Pins	
V_O = 0V to V_{CC}	±50 mA
V_{CC} or GND Current (I_{CC}, I_{GND})	±100 mA
Storage Temperature (T_{STO})	−60°C to + 150°C

Recommended Operating Conditions

Supply Voltage V_{CC}	3.0V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Input Range for AI/O ($V_{AI/O}$)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Ambient Temperature	
in Free Air (T_{AMB})	−40°C to +85°C

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristic tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC Electrical Characteristics (Digital Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CC} = 3.0V to 3.6V

Symbol	Parameter	Test Conditions	Limits			Unit
			Temperature = −40°C to +85°C			
			Min	Typ	Max	
Input Levels						
V_{IL}	LOW Level Input Voltage				0.8	V
V_{IH}	HIGH Level Input Voltage		2.0			V
Output Levels						
V_{OL}	LOW Level Output Voltage	I_{OL} = 4 mA			0.4	V
		I_{OL} = 20 µA			0.1	
V_{OH}	HIGH Level Output Voltage	I_{OH} = 4 mA	2.4			V
		I_{OH} = 20 µA	V_{CC} − 0.1			
Leakage Current						
I_L	Input Leakage Current	V_{CC} = 3.0 to 3.6			±5	µA
I_{CCFS}	Supply Current (Full Speed)	V_{CC} = 3.0 to 3.6			5	mA
I_{CCLS}	Supply Current (Low Speed)	V_{CC} = 3.0 to 3.6			5	mA
I_{CCQ}	Quiescent Current	V_{CC} = 3.0 to 3.6 V_{IN} = V_{CC} or GND			5	mA
I_{CCS}	Supply Current in Suspend	V_{CC} = 3.0 to 3.6; Mode = V_{CC}			10	µA

DC Electrical Characteristics (D+/D− Pins)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted). V_{CC} = 3.0V to 3.6V

Symbol	Parameter	Test Conditions	Limits			Units
			Temperature = −40°C to +85°C			
			Min	Typ	Max	
Input Levels						
V_{DI}	Differential Input Sensitivity	|(D+) – (D–)|	0.2			V
V_{CM}	Differential Common Mode Range	Includes V_{DI} Range	0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8		2.0	V
Output Levels						
V_{OL}	Static Output LOW Voltage	R_L of 1.5 kΩ to 3.6V			0.3	V
V_{OH}	Static Output HIGH Voltage	R_L of 15 kΩ to GND	2.8		3.6	V
V_{CR}	Differential Crossover		1.3		2.0	V
Leakage Current						
I_{OZ}	High Z State Data Line Leakage Current	0V < V_{IN} < 3.3V			±5	µA
Capacitance						
C_{IN}	Transceiver Capacitance	Pin-to-GND			10	pF
(Note 5)	Capacitance Match				10	%
Output Resistance						
Z_{DRV}	Driver Output Resistance	Steady State Drive	4		20	Ω
(Note 4)	Resistance Match				10	%

Note 4: Excludes external resistor. In order to comply with USB Specification 1.1, external series resistors of 24Ω ± 1% each on D+ and D– are recommended. This specification is guaranteed by design and statistical process distribution.

Note 5: This specification is guaranteed by design and statistical process distribution.

AC Electrical Characteristics (D+/D− Pins, Full Speed)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} = 3.0V to 3.6V; C_L = 50 pF; R_L = 1.5 kΩ on D+ to V_{CC}

Symbol	Parameter	Test Condition	Limits			Units
			Temperature = −40°C to +85°C			
			Min	Typ	Max	
Driver Characteristics						
		10% and 90%				
t_R	Rise Time	Figure 1	4		20	ns
t_F	Fall Time	Figure 1	4		20	
t_{RFM}	Rise/Fall Time Matching	(t_R/t_F)	90		110	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Driver Timings						
t_{PLH}	Driver Propagation Delay	Figure 2			18	ns
t_{PLH}	(V_{po}, V_{mo}/F_{SEO} to D+/D–)	Figure 2			18	ns
t_{PHZ}	Driver Disable Delay	Figure 4			13	ns
t_{PLZ}	($\overline{OE}$ to D+/D–)	Figure 4			13	ns
t_{PZH}	Driver Enable Delay	Figure 4			17	ns
t_{PZL}	($\overline{OE}$ to D+/D–)	Figure 4			17	ns
Receiver Timings						
t_{PLH}	Receiver Propagation Delay	Figure 3			16	ns
t_{PHL}	(D+, D– to RCV)	Figure 3			19	ns
t_{PLH}	Single-ended Receiver Delay	Figure 3			8	ns
t_{PHL}	(D+, D– to V_p, V_m)	Figure 3			8	ns

AC Electrical Characteristics (D+/D– Pins, Low Speed)

Over recommended range of supply voltage and operating free air temperature (unless otherwise noted).
V_{CC} = 3.0V to 3.6V; C_L = 200 pF to 600 pF; R_L = 1.5kΩ on D– to V_{CC}

Symbol	Parameter	Test Conditions	Limits			Unit
			T_{AMB} = –40°C to +85°C			
			Min	Typ	Max	
Driver Characteristics						
		10% and 90%				
t_{LR}	Rise Time	Figure 1	75		300	ns
t_{LF}	Fall Time	Figure 1	75		300	
t_{RFM}	Rise/Fall Time Matching	(t_R/t_F)	80		120	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Driver Timings						
t_{PLH}	Driver Propagation Delay	Figure 2			300	ns
t_{PHL}	(V_{po}, V_{mo}/F_{SEO} to D+/D–)	Figure 2			300	ns
t_{PHZ}	Driver Disable Delay	Figure 4			13	ns
t_{PLZ}	($\overline{OE}$ to D+/D–)	Figure 4			13	ns
t_{PZH}	Driver Enable Delay	Figure 4			205	ns
t_{PZL}	($\overline{OE}$ to D+/D–)	Figure 4			205	ns
Receiver Timings						
t_{PLH}	Receiver Propagation Delay	Figure 3			18	ns
t_{PHL}	(D+, D– to RCV)	Figure 3			18	ns
t_{PLH}	Single-ended Receiver Delay	Figure 3			28	ns
t_{PHL}	(D+, D– to V_p, V_m)	Figure 3			28	ns

AC Waveforms

V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load. (V_{CC} never goes below 3.0V)

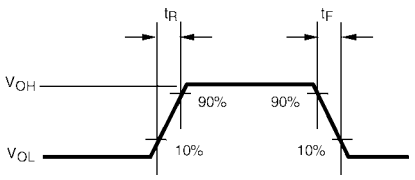


FIGURE 1. Rise and Fall Times

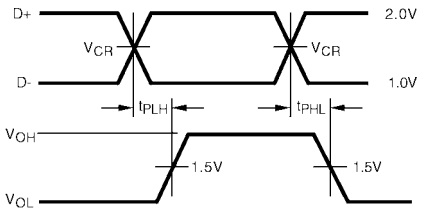


FIGURE 2. V_{pi}, V_{mo}/F_{SEO} to D+/D–

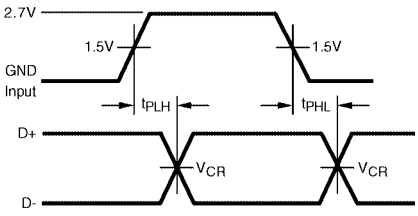


FIGURE 3. D+/D– to RCV, V_p/V_m

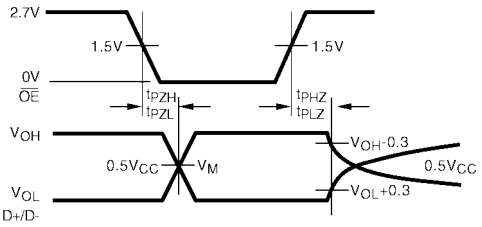
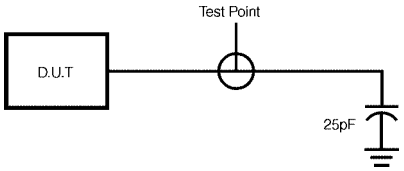
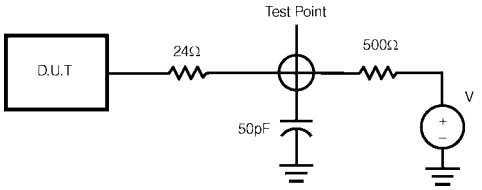


FIGURE 4. $\overline{OE}$ to D+/D–

Test Circuits and Waveforms



Load for V_m/V_p and RCV

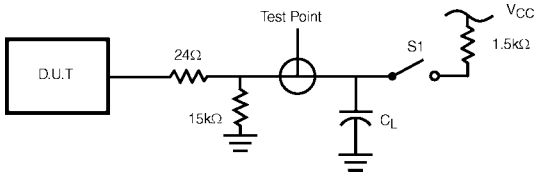


Load for Enable and Disable Times

Note:

V = 0 for t_{PZH}, t_{PHZ}

V = V_{CC} for t_{PZL}, t_{PLZ}



Load for D+/D–

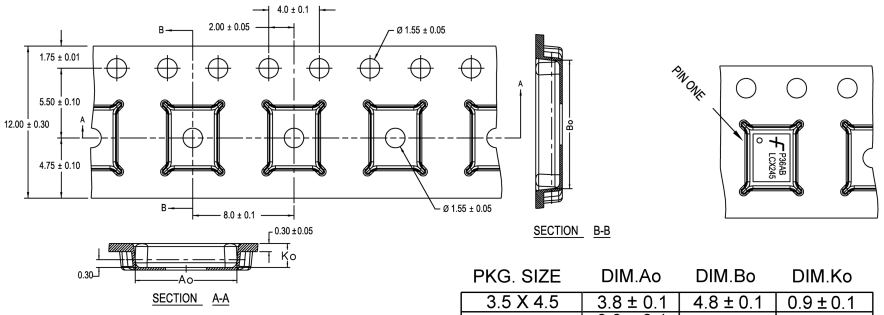
Test	S1
C_L = 50 pF, Full Speed	D–/LS	Close
C_L = 200 pF, Low Speed (Minimum Timing)	D+/LS	Open
C_L = 600 pF, Low Speed (Maximum Timing)	D–/FS	Open
1.5 kΩ on D– (Low Speed) or D+ (Full Speed) only	D+/FS	Close

Tape and Reel Specification

Tape Format for MLP

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
MPX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



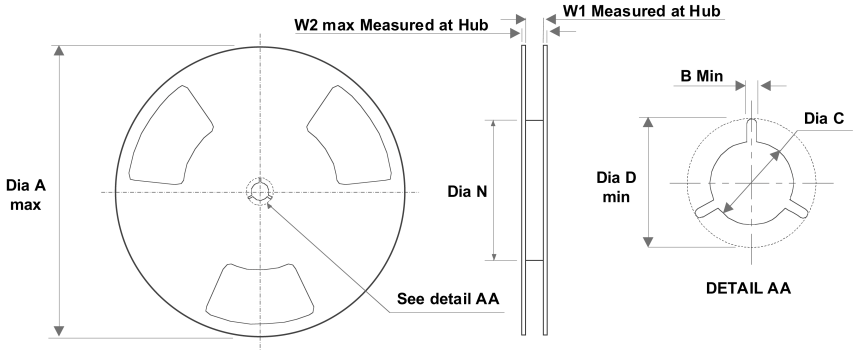
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

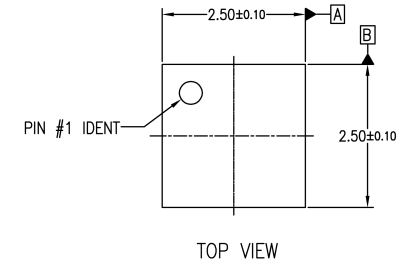
1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.

REEL DIMENSIONS inches (millimeters)

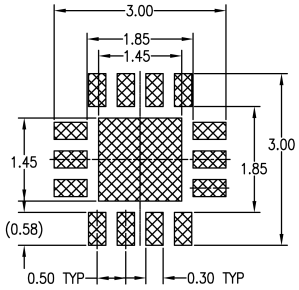


Tape Size	A (mm)	N (Typical) (mm)	W1 (mm)	W2 (Max) (mm)
12 mm	330	178	12.4	18.4

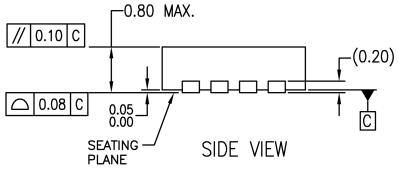
Physical Dimensions inches (millimeters) unless otherwise noted



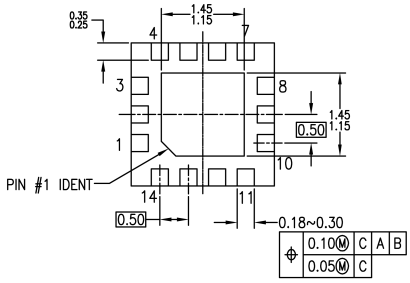
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

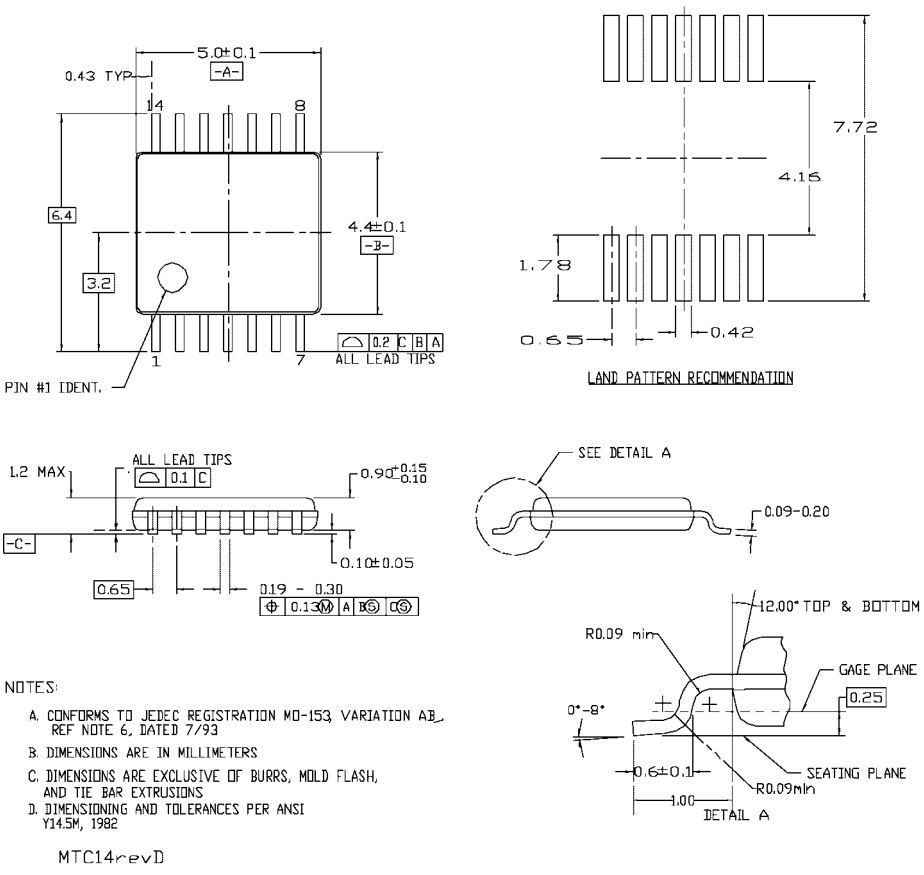
NOTES:

A. NO JEDEC REGISTRATION
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14DrevA

14-Terminal Molded Leadless Package (MLP), 2.5mm Square
Package Number MLP14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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