TC6102

2-PORT 10/100M ETHERNET SWITCH CONTROLLER

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2-PORT 10/100M ETHERNET SWITCH CONTROLLER

1. Features

- Single-chip, low cost, two port Switched Controller.
- Direct interface to two 10/100 Mbps MII (Media Independent Interface).
- Support Half/Full duplex(Full duplex for 10Mbps, Half duplex for 100Mbps).
- Support 'Store and Forward', 'Fragment-free' switching approach.
- Support special backpressure with buffering feature for half-duplex operation.
- Support up to 2K MAC address.
- Automatic address aging at 300 seconds or 20 seconds.
- Forwarding and filtering at full wire speed(148810 packets/sec).
- Glueless interface to 1 Mbyte of EDO DRAM (two 256K*16).
- Low power CMOS design with single +5V supply.
- 100 pin PQFP package.

2. General Description

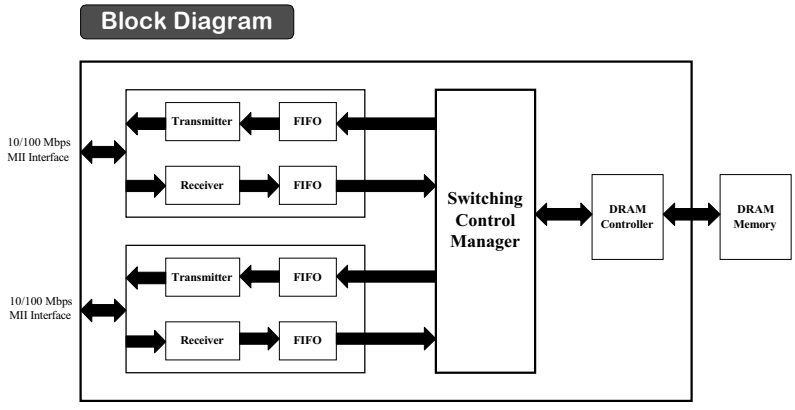
The TC6102 , a two-port Switched Controller, is an ideal solution for dual speed Hub application. It provides functions including filtering, forwarding, learning and aging between two 10/100 Mbps ports. It supports full auto-negotiation for capable PHYs. Therefore, The speed (10 or 100 Mbps) and duplex (half or full) which the PHY resolves to operate is automatically report to the TC6102.

The chip in a system can recognize up to 2K different MAC addresses. An address recognition mechanism enables filtering and forwarding packets at full wire speed. It also implements address aging to update address table, addresses which have not been seen within 300 sec (or 20 sec) will be removed from the address table.

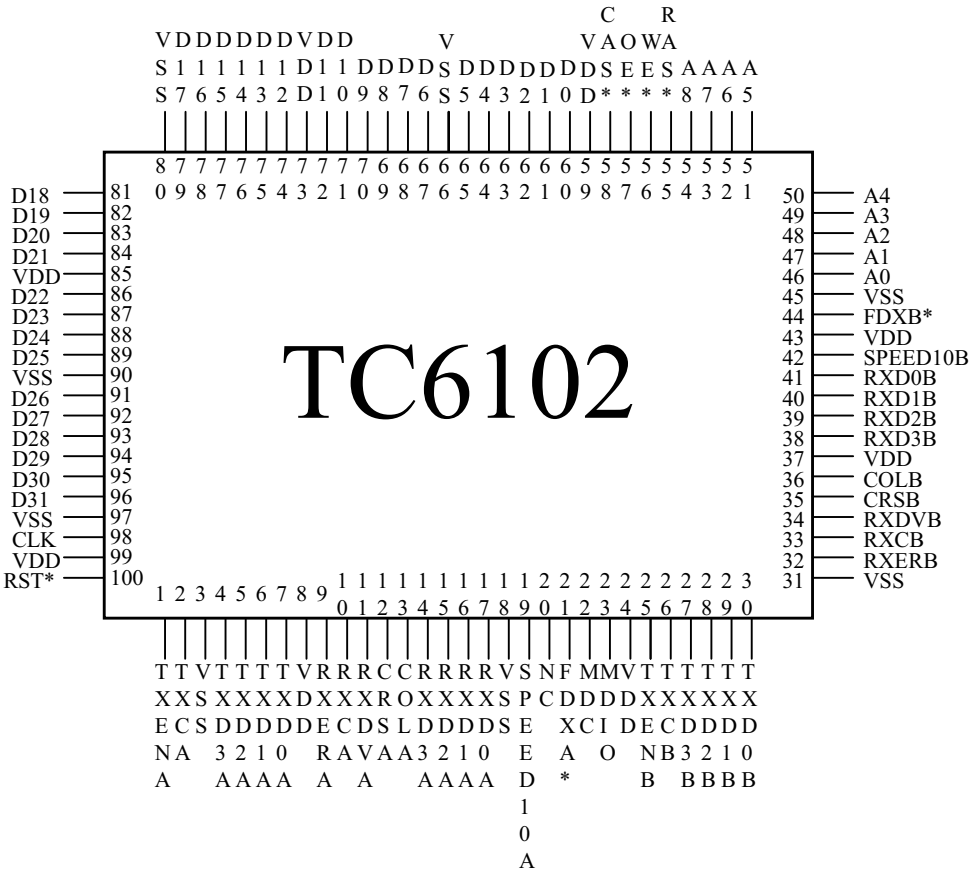
The chip interfaces directly to 1 Mbyte(two 256Kx16) of EDO DRAM. The DRAM is used to store the incoming/outgoing packets. The interface to EDO DRAM is glueless.

The chip supports a special backpressure with buffering feature (in half-duplex mode) for dual-speed Hub application. If the backpressure is enabled; when the stored packet count reached the buffer threshold and the forwarding packet is detected at the same port, the TC6102 will send a JAM pattern on this port to stop receiving this packet. It means collision happened. If the successive collision count is too much, the TC6102 will let the forwarding packet come-in to prevent the Hub from partitioning. This special backpressure with buffering feature improves the communication quality and performance on dual-speed Hub application.

3. Block Diagram



4. Pin Assignment



4.1 MEDIA INDEPENDENT INTERFACE

Symbol	Pin No	I/O	Description
TXENA TXENB	1 25	O	**Transmit Enable :** Active HIGH. This output indicates that the packet is being transmitted. TxEn is synchronous to TxClk.
TXCA TXCB	2 26	I	**Transmit Clock :** Provides the timing reference for the transfer of TxEn, TxD signals. TxClk frequency is one fourth of the data rate (25 MHz for 100Mbps, 2.5 MHz for 10Mbps). Txclk nominal frequency should match the nominal frequency of RxClk for the same port.
TxD[3:0] A	4-7	O	**Transmit Data A :** Outputs the PortA Transmit Data. Synchronous to TxClkA.
TxD[3:0] B	27-30	O	**Transmit Data B :** Outputs the PortB Transmit Data. Synchronous to TxClkB.
COLA COLB	13 36	I	**Collision Detect :** Active HIGH. Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode, and in half-duplex mode when TxEn of the same port is LOW. Col is not synchronous to any clock.

4.1 MEDIA INDEPENDENT INTERFACE

Symbol	Pin No	I/O	Description
RxD[3:0] A	14-17	I	**Receive Data A :** PortA Receive Data. Synchronous to RxClkA.
RxD[3:0] B	38-41	I	**Receive Data B :** PortB Receive Data. Synchronous to RxClkB.
RXERA RXERB	9 32	I	**Receive Error :** Active HIGH. Indicates that an error was detected in the received frame. This input is ignored when RxDV for the same port is inactive.
RXCA RXCB	10 33	I	**Receive Clock :** Provides the timing reference for the transfer of the RxDV, RxD, RxEr signals (per port). Operates at either 25 MHz (100Mbps) or 2.5 MHz (10Mbps). The nominal frequency of RxClk (per port) should match the nominal frequency of that port ' s TxClk.
RXDVA RXDVB	11 34	I	**Receive Data Valid :** Active HIGH. Indicates that valid data is present on the Rxd lines. Synchronous to RxClk.
CRSA CRSB	12 35	I	**Carrier Sense :** Active HIGH. Indicates that either the transmit or receive medium is non-idle. CrS is not synchronous to any clock.
MDC	22	O	**Management Data Clock for NS DP83840A :** 1 MHz clock. Provides the timing reference for the transfer of the MDIO signal. This output may be connected to the PHY devices of both ports.
MDIO	23	O	**Management Data Output for NS DP83840A :** Configure Polarity/Full Duplex LED4(pin37) of NS DP83840A to indicate Full Duplex mode status. The operation will set PHY address 01111 and 11111 PCS configuration register(17H) to 9042H.

4.2 DRAM INTERFACE

Symbol	Pin No	I/O	Description
A0 A1 A2 A3 A4 A5 A6 A7 A8	46 47 48 49 50 51 52 53 54	I/O	**DRAM address bus - Configuration Register Input :** A0-A8 is time multiplexed with row and column address strobes. When RST* is active configuration Register is loaded with the data value on these pins(A0-A8). If the user puts an external pull-down resistor on any of these pins then the corresponding register bit is reset to 0. If the pin is left unconnected then the register bit is 1. A8=Switching approach. 1:Store & forward(default) , 0:fragment-free. A7=Maximum packet size. 1:1522 bytes(default) , 0:1518 bytes. A4=Backpressure 1:Enable(default), 0:disable A2=Hashing aging time. 1:300 sec(default) , 0:20 sec. A1=Filtering packet. 1:forward needed packets(default) , 0:Forward all packets.
CAS*	58	O	**DRAM column address select.**
RAS*	55	O	**DRAM row address select.**
D31 D30 D29 D28	96 95 94 93	I/O	**DRAM data bus :** D31-D0 is bi-directional.

4.2 DRAM INTERFACE

Symbol	Pin No	I/O	Description
D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	92 91 89 88 87 86 84 83 82 81 79 78 77 76 75 74 72 71 70 69 68 67 65 64 63 62 61 60		
OE*	57	O	**DRAM output enable.**
WE*	56	O	**DRAM write enable.**

4.3 MISCELLANEOUS INTERFACE PINS

Symbol	Pin No	I/O	Description
RST*	100	I	**RESET :** Active Low.
CLK	98	I	**Chip clock input for TC6102** The clock frequency is 25MHz .
SPEED10A SPEED10B	19 42	I	**Set Speed 10/100 Mbps :** Set 10Mb/s operation when high. Set 100Mb/s operation when low.
FDXA* FDXB*	21 44	I	**Set Half/Full Duplex :** Set Half Duplex operation when high. Set Full duplex mode operation when low. 100 Mb/s worked at half-duplex only.

4.4 POWER SUPPLY PINS

Symbol	Pin No	I/O	Description
VCC	8 24 37 43 59 73 85 99		**5V Power Pins.**
GND	3 18 31 45 66 80 90 97		**Ground Pins.**

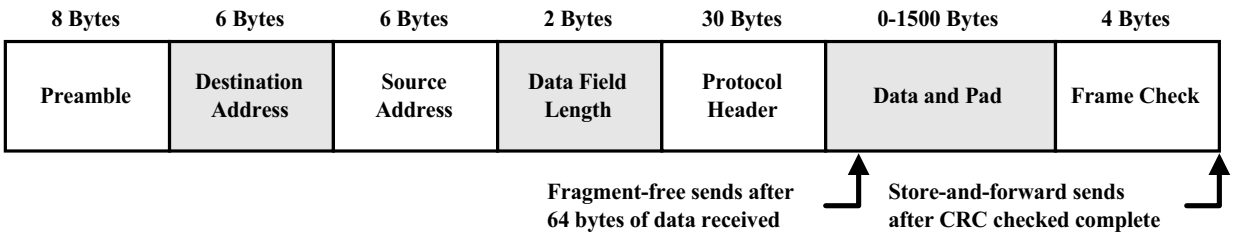
5. Function Description

The TC6102 looks at incoming packet and analyzes the destination address encapsulated in the packet's header. From this information, the switch can check its Address Table and determine whether to forward the packet to another port or filter it out. In this way, the TC6102 can seperate network traffic into two network collision domains.

5.1 FORWARDING APPROACH

(a). Store-and-forward: Completely store the incoming packet in buffers before sending it out on another port, so it can filter the incoming corrupted packet by analyzing the frame check sequence(FCS).

(b). Fragment-free: Forward the incoming packet when the first 64 bytes have been received successfully. If the packet is collided, it can be detected within the first 64 bytes of a frame, so it is a tradeoff between short switch latency and error-checking is achieved.



5.2 ADDRESS LEARNING

The TC6102 keeps a table, called the address table, it contains all of the source address and port number. When a packet is received on a port, the chip checks if the packet's source address is in the table. If it is not, then an entry containing the source address and the port number is added to the table. The TC6102 can learn up to 2K unique MAC addresses.

5.3 ADDRESS AGING

The TC6102 supports address aging. The aging interval can be set at 300 seconds or 20 seconds. If the source addresses have not been seen within the aging internal , it will automatically be removed from the address table. The aging process updates the living node table, if a node is disconnect from its segment, its entry is removed from the table. This also ensures that switch will properly relearn the address of nodes when they are moved from one segment to another.

5.4 ADDRESS RECOGNITION

The TC6102 forwards the incoming packets according the destination address. Recognition procedure are listed below.

(1). If the Destination address is a Multicast or Broadcast address, the packet is forwarded to another port.
(2). If the Destination address is a Unicast address and the address is not found in the address table, the packet is forwarded to another port.
(3). If the Destination address is a Unicast address and the address is found in the address table, then, there are two conditions as follows:

(a). If the Port Number is different from the port packet comes in, the packet is forwarded to another port.
(b). If the Port Number is the same as the port packet comes in, the packet is not forwarded to another port.

5.5 PACKET BUFFER

The TC6102 supports up to 512 full packet size (1522 bytes) receive buffers.

5.6 BACKPRESSURE

Backpressure is support for half-duplex operation. When the stored packet count already reached the buffer threshold and a forwarding packet also detected at the same port & same time , the TC6102 will transmit a JAM on this port, thus forcing a collision.

5.7 VLAN TAG

The TC6102 can accept 1522 bytes VLAN packet.

6. DC Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{IH}	Minimum High Level Input Voltage	TTL Input	2.0		V
V_{IL}	Maximum Low Level Input Voltage	TTL Input		0.8	V
V_{OH}	Minimum High Level Output Voltage	I_{OH} = -4 mA	3.7		V
V_{OL}	Maximum Low Level Output Voltage	I_{OL} = 1 to 4 mA		0.5	V
I_{IN}	Input Current	With Internal Pullup		±150	µA
		Without Internal Pullup		±10	
I_{OZ}	TRI-STATE Output Leakage Current	With Internal Pullup		±150	µA
		Without Internal Pullup		±10	
I_{CC}	Operating Current	Typical V_{CC} = 5V		30	mA

6.1 ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	-0.5V to 7.0V
Input Voltage (DC_{IN})	-0.5V to V_{CC} + 0.5V
Output Voltage (DC_{OUT})	-0.5V to V_{CC} + 0.5V
Storage Temperature	-65°C to 150°C
ESD Protection	2000V

6.2 RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Units
Supply Voltage (V_{DD})	4.75	5.0	5.25	V
Ambient Temperature (T_A)	0		70	°C
Center Frequency (X_{FC})		25		MHz

6.3 THERMAL CHARACTERISTICS

	Max	Units
Theta Junction to Ambient (T_{ja}) degrees Celsius/ Watt-No Airflow	33.4	°C/W

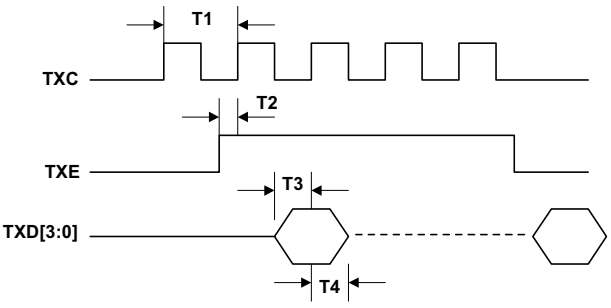
7. AC Specifications

Transmit Timing

Parameter	Description	Min	Typ	Max	Units
T1	TXC Period		40(400)		ns
T2	TXE to TXC septup time	10			ns
T3	TXD[3:0] to TXC setup time	10			ns
T4	TXD[3:0] to TXC hold time	5			ns

Notes:
1. All Delay, Setup, and Hold times are referred to CLK rising edge.
2. All outputs are specified for 50pF load.

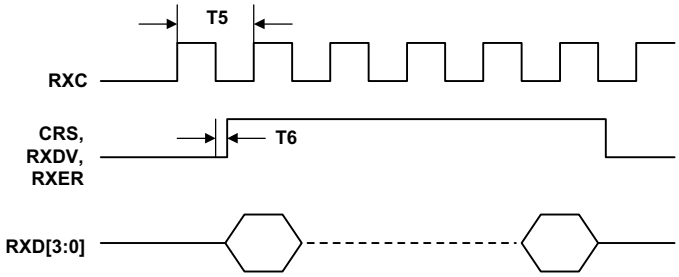
Transmit Timing



Receive Timing

Parameter	Description	Min	Typ	Max	Units
T5	RXC period		40(400)		ns
T6	RXC falling edge to CRS, RXDV, RXD[3:0] and RXER valid		10		ns

Receive Timing



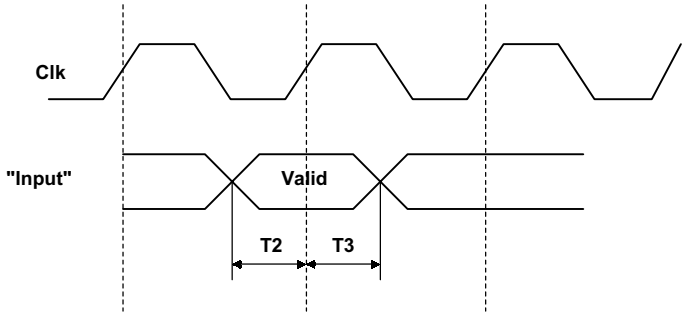
DRAM Timing

Symbol	Signals	Description	Min	Max	Units
	Clk	System Clock	25		MHz
T1	A[8:0], D[31:0], CAS*, RAS*, WE*, OE*	Delay from Clock Rising or Falling Edge	3	15	ns
T2	D[31:0]	Setup	10		ns
T3	D[31:0]	Hold	1		ns
T4	D[31:0]	Float Delay	2	18	ns
T5	D[31:0]	Drive Delay	2	10	ns

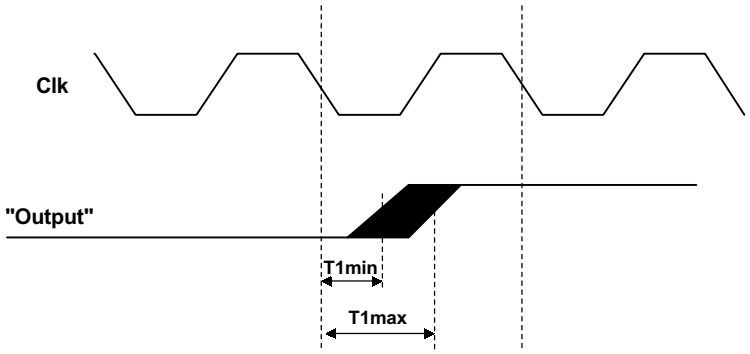
Notes:

1. All Delay, Setup, and Hold times are referred to CLK rising edge, unless stated otherwise.
2. All outputs are specified for 50pF load.

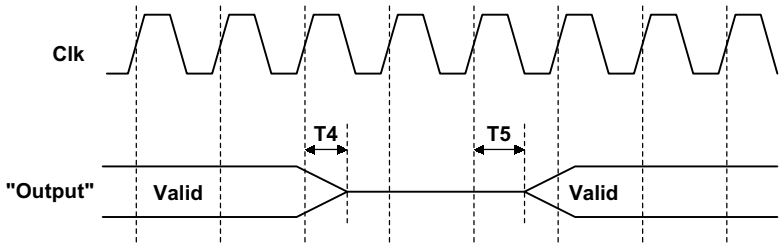
Input Setup and Hold



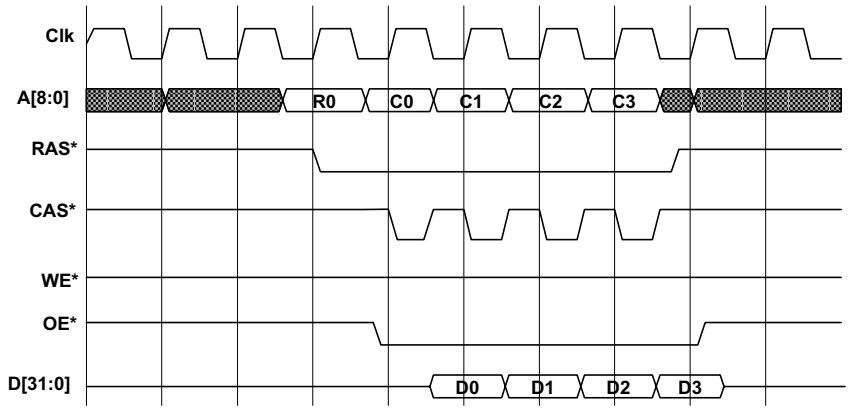
Output Delay from Clock

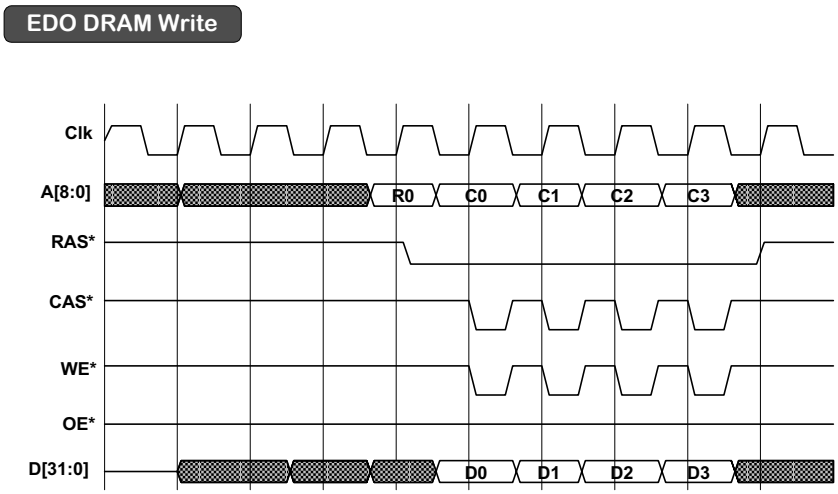


Output Float and Drive Delay

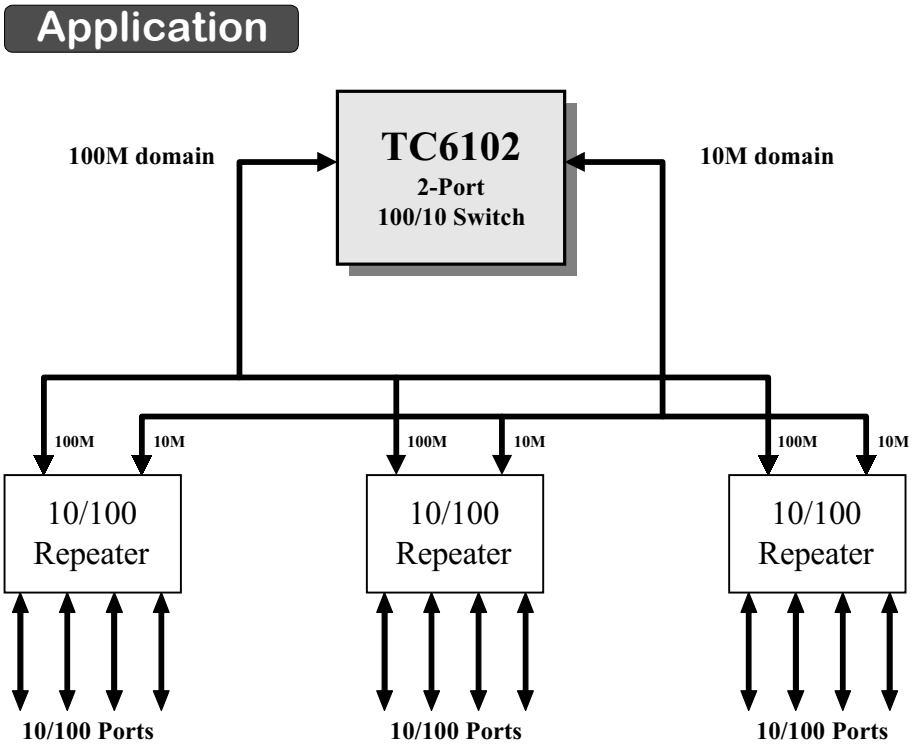


EDO DRAM Read

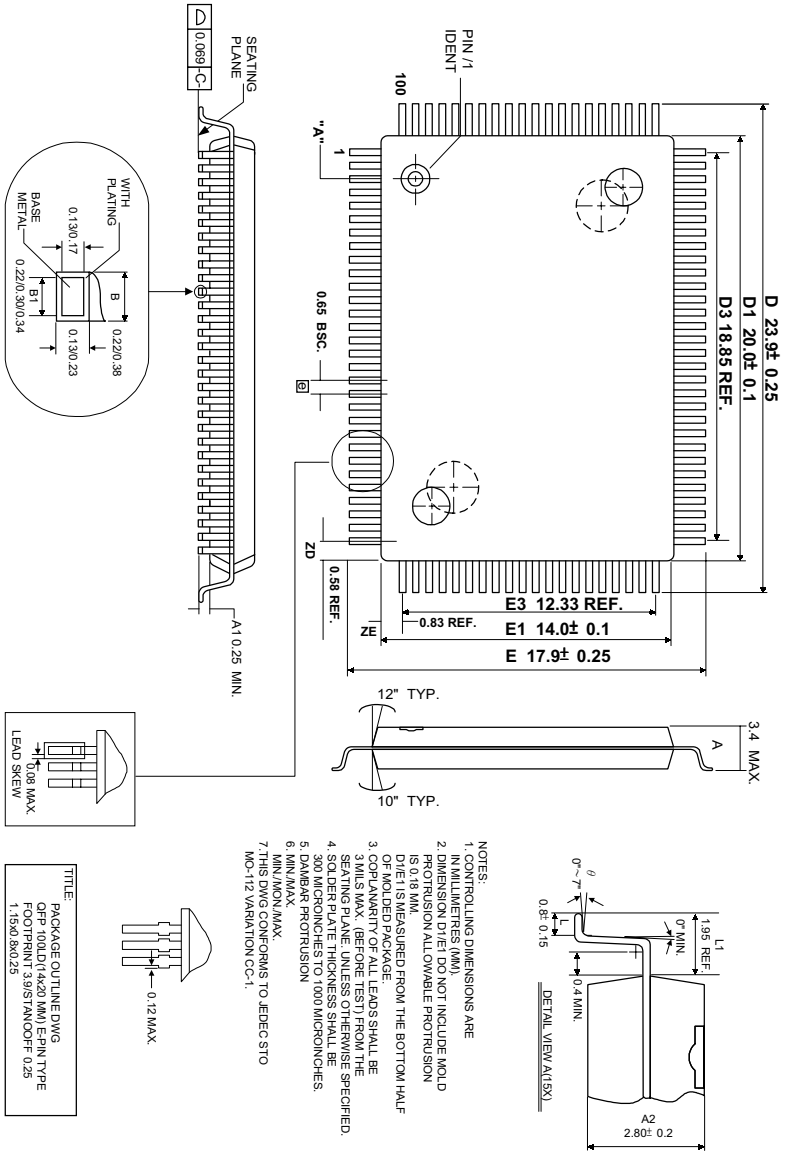




8. Application



9. Physical Dimensions (100pin POFP)



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