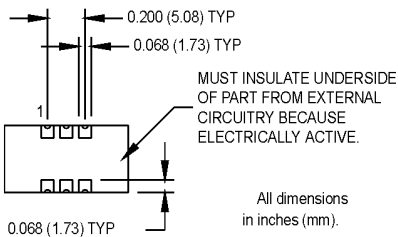
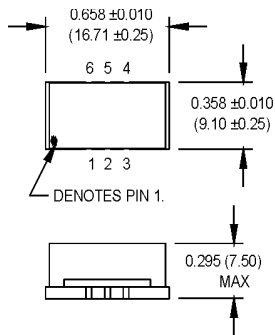


M5003 Series

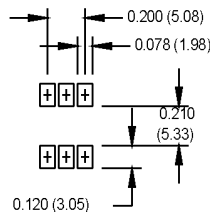
9x16 mm FR-4, 3.3 Volt, CMOS/TTL/PECL/LVDS, HPVCXO



- Ideal for applications requiring long term (20 year) all-inclusive stability



SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Tristate
3	Ground
4	Output 1
5	N/C or Output 2
6	+Vdd

Ordering Information

M5003	2	0	R	1	P	K	-R	00.0000	MHz
Product Series									
Temperature Range									
1: 0°C to +70°C	2: -40°C to +85°C								
6: -20°C to +70°C	7: 0°C to +85°C								
Stability									
0: Nominal per APR selection									
Output Type									
R: Complementary tri-state (PECL/LVDS)									
T: Tri-state (CMOS)									
Absolute Pull Range (APR)									
1: ±25 ppm									
2: ±15 ppm									
Symmetry/Logic Compatibility									
D: 45/55% CMOS/TTL	L: 45/55% LVDS								
P: 45/55% PECL									
Package/Lead Configurations									
K: FR-4, 6-Pad									
RoHS Compliance									
Blank: non-RoHS compliant part									
-R: RoHS compliant part									
Frequency (customer specified)									

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	1		160	MHz	CMOS/TTL
		19.44		800	MHz	PECL/LVDS
Operating Temperature	T _A	(See Ordering Information)				
Storage Temperature	T _S	-55		+105	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				See Note 1
Aging						
1st Year				1.5	ppm	
Thereafter (per year)				0.5	ppm	
Pullability/APR		(See Ordering Information)				Over Control Voltage
Control Voltage	V _C	0.3	1.65	3.0	V	
Tuning Range				25	ppm/V	
Modulation Bandwidth	f _m	10			kHz	
Input Impedance	Z _{in}	50K			Ohms	
Input Voltage	V _{CC/VDD}	3.15	3.3	3.45	V	
Input Current	I _{CC/IDD}	5		50	mA	CMOS/TTL
		50		120	mA	PECL
		5		75	mA	LVDS
Output Type						CMOS/TTL/PECL/LVDS
Load		2 TTL or 15 pF Max. 50 Ohms to V _{CC} -2 Volts 100 Ohm differential load				CMOS/TTL PECL LVDS
Symmetry (Duty Cycle)		(See Ordering Information)				
Output Skew				50	ps	PECL
Differential Voltage		250	375	500	mV	LVDS
Logic "1" Level	V _{OH}	2.5		2.4	V	CMOS/TTL
		2.2			V	PECL
		1.375			V	LVDS
Logic "0" Level	V _{OL}			0.5	V	CMOS/TTL
		1.4		1.7	V	PECL
				1.125	V	LVDS
Rise/Fall Time	T _r /T _f	2.0		10	ns	CMOS/TTL
		0.25		3.0	ns	PECL/LVDS
Tristate Function		Input Logic "1": output active Input Logic "0": output disables				Opposite tristate logic Available upon request
Start up Time		10			ms	
Phase Noise (Typical)		10 Hz	100 Hz	1 kHz	10 kHz	Offset from carrier
@ 19.44 MHz	-60	-90	-120	-135	-148	dBc/Hz
@ 155.52 MHz	-60	-90	-110	-120	-120	dBc/Hz
@ 622.08 MHz	-60	-90	-100	-105	-105	dBc/Hz

1. Stability includes initial tolerance, deviation over temperature, supply and load variation, and aging for 20 years @ 25°C.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.

Please see www.mtronpti.com for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.

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