Low Level Input, 12-Bit Data Acquisition Modules

DAS1150, DAS1151

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PRELIMINARY TECHNICAL DATA

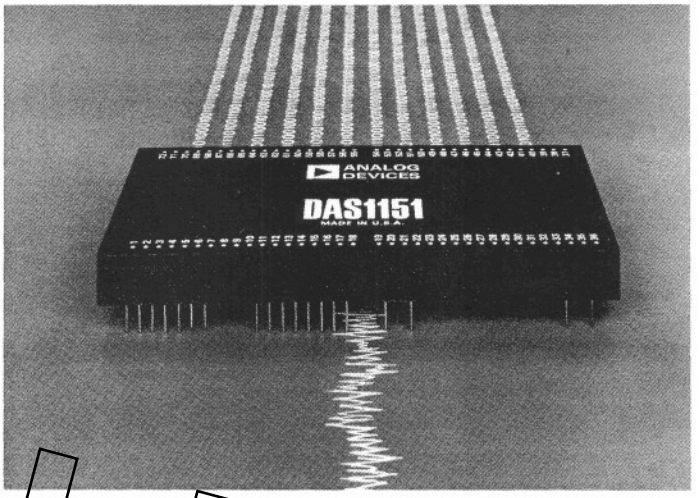
FEATURES

DAS1150

- Resistor-Programmable Gain (1 = 1000V/V)
- High Accuracy with Low Level Input Signals
- Low Cost
- High Throughput Rate and High Gain

DAS1151

- Software-Programmable Gain (1, 2, 4, 8V/V)
- Provides Gain for Signal Conditioning and High Throughput Rate
- Gain Ratio Error: ±0.02% FS max



GENERAL DESCRIPTION

The DAS1150 and DAS1151 are two data acquisition modules designed, built and tested to meet system data acquisition requirements. Each device comprises an instrumentation amplifier, sample-hold amplifier and 12-bit successive approximation A/D converter. These products are used on Analog Devices Real Time Interface boards as data acquisition systems to interface with microcomputer boards.

With the DAS1150 and DAS1151, users can apply gain to the instrumentation amplifier for signal conditioning and still achieve high speed data conversion. The difference between models is how the gain is controlled. With the DAS1150, the designer sets the gain from 1 to 1000 V/V with a resistor, R_G. The DAS1151 has gains of 1-2-4-8 that are software-programmable.

DESIGN FEATURES AND USER BENEFITS

The DAS1150 and DAS1151 offer true high-speed 12-bit performance with maximum overall error at unity gain of ±1 least significant bit (LSB). This performance is guaranteed at a 25kHz throughput rate. There is very little performance lost at high gains. For example, at gain of 1000, the DAS1150 has a throughput of 13kHz and an overall accuracy of ±2LSB. The DAS1151 with its software-programmable gain provides dynamic range expansion as well as the flexibility of using different gain settings to accommodate different input signal levels. The resistor-programmable-gain DAS1150 may be used for input ranges from 10mV full scale to ±10V full scale with very little loss of speed and no degradation of linearity at high gain.

THEORY OF OPERATION

Block diagrams of the DAS1150 and DAS1151 are shown in Figures 1 and 2. Analog input signals are applied to the input of the instrumentation amplifier. The instrumentation amplifier is gain-programmable by the user via a resistor (DAS1150) or TTL/CMOS logic (DAS1151). This feature permits the user to operate the module on any input voltage range from ±10mV to ±10V with the DAS1150 or any of 4 input voltage ranges with the DAS1151. The instrumentation amplifier drives a sample-hold amplifier, whose function is to hold the selected analog input signal at a constant level while the A/D converter is making a conversion.

The A/D converter is a high speed 12-bit successive approximation device that has been designed using Analog Devices AD562 IC D/A converter with a precision reference source, a high speed comparator and successive approximation logic.

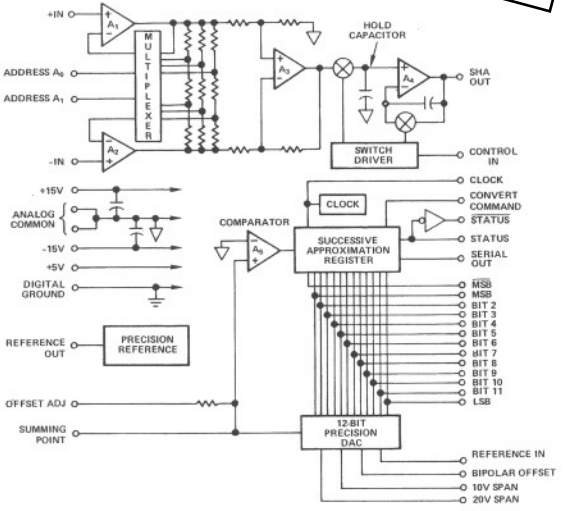


Figure 1. DAS1151 Block Diagram and Pin Designations

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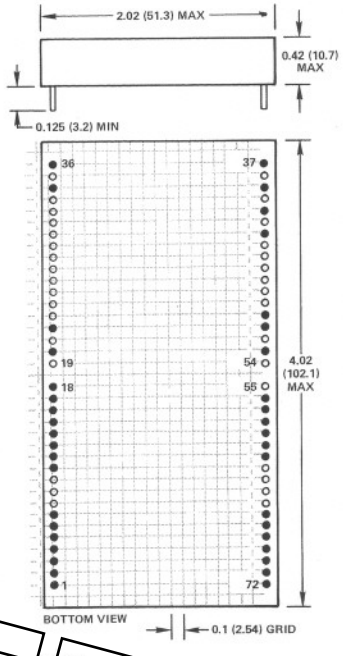
SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise noted)

MODELS	DAS1150	DAS1151
RESOLUTION	12 Bits	*
DYNAMIC CHARACTERISTICS		
ADC Conversion Time	25µs max	*
IA Settling Time, 20V Input Step		
to 0.01% @ G = 1	15µs max	(G = 1-8) 10µs max
to 0.01% @ G = 10	15µs	N.A.
to 0.05% @ G = 1000	50µs	N.A.
Throughput Rate G = 1	25kHz	(G = 1-8) 28.5kHz
G = 10	25kHz	N.A.
G = 1000	13.3kHz	N.A.
Sample-Hold		
Acquisition Time	3µs	*
Aperture Delay Time	90ns	*
Aperture Time	20ns	*
Aperture Uncertainty Time	5ns	*
Droop Rate	2mV/s	*
ACCURACY		
Overall Error[1] @ G = 1	±1LSB max	*
@ G = 1000	±2LSB max	(G = 8) ±2LSB max
Nonlinearity Error	±1/2LSB (±1LSB max)	*
Offset Error	Adjust to Zero	*
Gain Error	Adjust to Zero	*
TEMPERATURE COEFFICIENTS		
Offset (RTI)	$\pm\left(1+\frac{50}{G}\right)$ µV/°C	±30µV/°C
Gain (RTI)	±20ppm of Reading/°C	*
Differential Nonlinearity	2ppm/°C	*
ANALOG INPUTS		
Voltage Input Range $\left(\frac{\text{ADC FS}}{\text{GAIN}}\right)$	10mV to +10V	0.625V to ±10V
ADC Input Ranges	0 to +5V	*
	0 to +10V	*
	±2.5V	*
	±5V	*
	±10V	*
Instrumentation Amplifier		
Gain	Resistor-Programmable	Software-Programmable
Gain Range	1 to 1000	1, 2, 4, 8
Gain Equation	$G = 1 + \left(\frac{20k\Omega}{R_G}\right)$	See Table 4
Gain Ratio Error[2]	N.A.	±0.02% FS max
Input Impedance	$10^8\Omega$	*
Bias Current	20nA	2nA
Offset Current	2nA	500pA
Offset Voltage (RTI)	±50µV	±200µV
DIGITAL INPUTS		
ADC Convert Command	Positive Pulse, TTL Compatible, 100ns min Width	* *
SHA Mode Control	Positive Pulse TTL Compatible Logic "1" = Hold, Logic "0" = Sample	* *
PGA Gain Control	N.A.	TTL Compatible, Positive True
DIGITAL OUTPUT		
Parallel Data Output	6TTL Loads/Bit	*
Unipolar	Positive True Binary	*
Bipolar	Positive True Offset Binary or Two's Complement	* *
Serial Data Output	6 TTL Loads	*
Unipolar	Positive True Binary NRZ Format, MSB First	* *
Bipolar	Positive True Offset Binary, NRZ Format, MSB First	* *
Status Output	Logic "1" During Conversion, TTL Compatible, 4TTL Loads, Complement also Available	* * *
Clock Output	480kHz, TTL Compatible, 6TTL Loads	*
POWER REQUIREMENTS	+5V dc ±5% @ 130mA (170mA max)	*
	±15V dc ±3% @ 30mA (40mA max)	*
	±15V dc ±3% @ 30mA (40mA max)	*
TEMPERATURE RANGE		
Operating	0 to +70°C	*
Storage	-55°C to +85°C	*
PRICE		
(1-24)	$199	$249

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OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.
SEE TABLE BELOW FOR PIN DELETIONS.
MODULE WEIGHT: 3.5 OUNCES (99.3 GRAMS)
ALL PINS ARE GOLD PLATED HALF-HARD BRASS (MIL-G-45204), 0.019" ±0.001" (0.48 ±0.03mm) DIA.

MODEL	DELETED PINS
DAS1150	PINS 50, 51
DAS1151	PINS 41, 43

MATING SOCKET: AC1577
(4 per, $3 each)

NOTES

[1] Overall error is specified with gains and offset trimmed and is defined as the deviation from a straight line passing through the end points of the range.

[2] Once the full scale has been calibrated on any gain setting, switching to any other gain setting will cause no more than a 0.02% shift in full scale.

*Specifications same as DAS1150.

Specifications subject to change without notice.

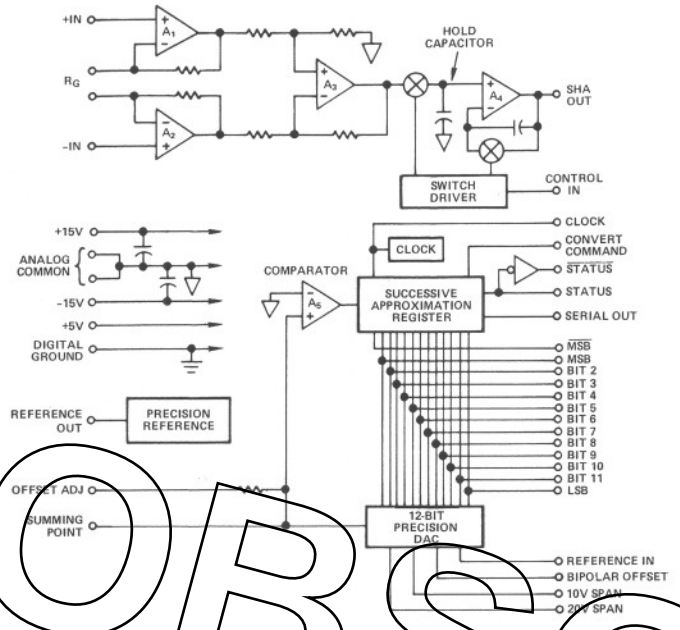


Figure 2. DAS1150 Block Diagram and Pin Designations

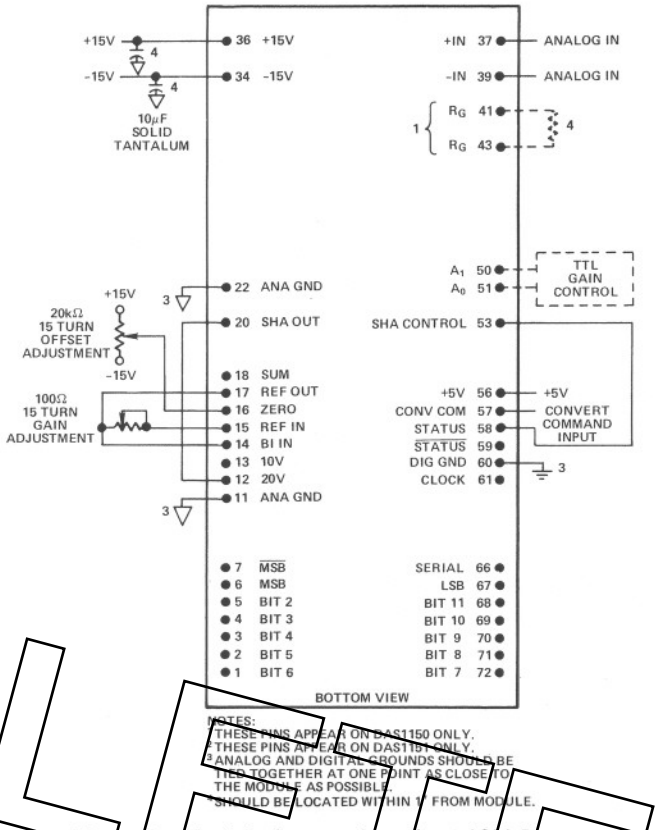


Figure 3. Module Connections for ±10V Range

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GROUNDING PRACTICE

Attention should be given to the methods of connection for electrical returns and voltage reference points. Analog ground and digital ground are provided. These data acquisition systems do not have an internal connection between analog ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops between the high current carrying logic supply ground and the sensitive analog circuit sections.

1. If the ±15V power supply is floating (for optimum analog accuracy), connect its common to analog ground. If the ±15V power supply is not floating, connect its common to digital ground.
2. Connect the +5V supply common to digital ground. If this supply also powers additional equipment, run separate, parallel returns to the equipment ground and to digital ground.
3. Single-ended input signals should only be returned to analog ground. If this is not possible, then connect the input signals in the differential configuration.
4. Connect computer ground to digital ground. Use heavy wire or ground planes.
5. The computer chassis should be connected to the computer and power supply grounds at only one point.
6. Connect the third wire ground from main ac power input to the computer power supply return.
7. Bias return path should always be provided.

Figure 3 shows the connections required to operate the DAS1150 or DAS1151 with a ±10V input range. Table 1 shows connections for ADC input ranges.

Input Range	Jumper
0 to +5V	Pin 17 to 15, Pin 20 to 18
±2.5V	Pin 17 to 14, Pin 20 to 18
0 to +10V	Pin 17 to 15, Pin 20 to 13
±5V	Pin 17 to 14, Pin 20 to 13
±10V	Pin 17 to 14, Pin 20 to 12

Table 1. ADC Input Range Connections

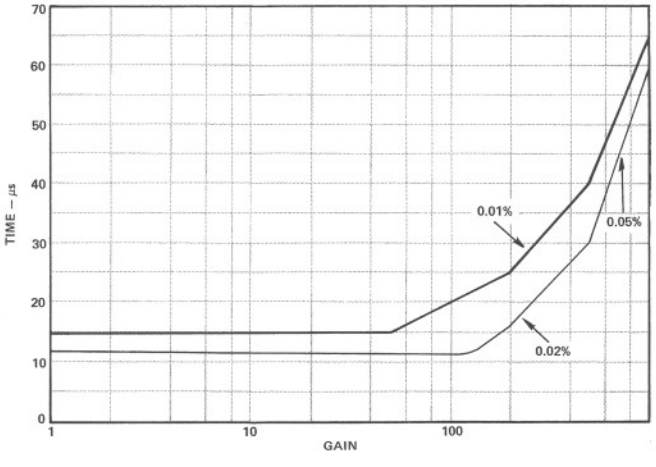


Figure 4. Typical Settling Time Curves for DAS1150

GAIN AND OFFSET ADJUSTMENT PROCEDURE

ADC ANALOG INPUT		DIGITAL OUTPUT
+5V RANGE	+10V RANGE	BINARY CODE
+4.9988V	+9.9976V	111111111111
+2.5000V	+5.0000V	100000000000
+0.6250V	+1.2500V	001000000000
+0.0012V	+0.0024V	000000000001
+0.0000V	+0.0000V	000000000000

Table 2. Nominal Unipolar Input-Output Relationships

ADC ANALOG INPUT			DIGITAL OUTPUT	
±2.5V RANGE	±5V RANGE	±10V RANGE	OFFSET BINARY CODE	TWO'S COMPLEMENT CODE
+2.4988V	+4.9976V	+9.9951V	111111111111	0111111111111
+1.2500V	+2.5000V	+5.0000V	110000000000	0100000000000
+0.0012V	+0.0024V	+0.0049V	100000000001	0000000000001
+0.0000V	+0.0000V	+0.0000V	100000000000	0000000000000
−2.5000V	−5.0000V	−10.0000V	000000000000	1000000000000

Table 3. Nominal Bipolar Input-Output Relationships

OFFSET CALIBRATION

For unipolar mode set the input voltage precisely to the value of 1LSB (see Table 2) and adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For bipolar mode set the input voltage precisely to zero volts. Adjust the offset potentiometer until the offset binary coded units are just on the verge of switching from 011111111111 to 100000000000 and two's complement coded units are just on the verge of switching 111111111111 to 000000000000.

GAIN CALIBRATION

The analog input values given in Tables 2 and 3 are values that should be present at the input to the internal ADC. The value of the analog input will be affected by the gain of the module, i.e., $\text{ANALOG IN} = \left(\frac{\text{ADC FULL SCALE}}{\text{GAIN}}\right)$

Set the ADC input voltage precisely to plus full scale minus 1 1/2 LSB's: +4.9982V for 5V units, +9.9963V for ±10V units, +2.4982V for ±2.5V units, +4.9963V for ±5V units, or +9.9926V for ±10V units. Adjust the 100Ω variable gain resistor until binary and offset binary coded units are just on the verge of switching from 111111111110 to 111111111111 and two's complement coded units are just on the verge of switching from 011111111110 to 011111111111.

INCREASING THROUGHPUT RATE

Throughput rates for the DAS1150 and DAS1151 can be increased by the use of the OVERLAP MODE, i.e. updating the input while the ADC is making a conversion. Typical throughput rates can be increased to 35kHz @ G = 1, 20kHz @ G = 1000 for the DAS1150 and 35kHz for G = 1 thru 8 for the DAS1151. When the IA settling time is less than or equal to the sum of SHA acquisition time and ADC conversion time, 28μs, the DAS throughput rate equals 1/28μs or 35kHz. When IA settling time is greater than 28μs (see Figure 4), the DAS throughput rate equals the reciprocal of IA settling time.

TIMING

The "0" to "1" transition of the CONVERT COMMAND input resets the $\overline{\text{MSB}}$ output to Logic "0" and the CLOCK STATUS, MSB, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the CONVERT COMMAND returns to Logic "0", at which time the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's (D/A) output is compared with the analog input (SHA OUT). If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 12 (LSB) comparison is completed. At this time the STATUS output returns to Logic "0" and the conversion cycle ends.

The SERIAL DATA output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, 40ns after each of the twelve "0" to "1" clock transitions.

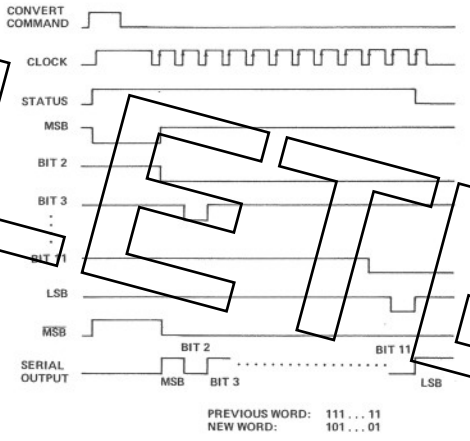


Figure 5. ADC Timing Diagram

AMPLIFIER GAIN

The DAS1150 instrumentation amplifier gain may be set to any any value between 1 and 1000 by connecting an external gain resistor between pins 41 and 43. The resistance is determined by the formula $G = 1 + \left(\frac{20k\Omega}{R_G}\right)$. R_G should be located as close as possible to the module pins. It must be noted that the TC of R_G directly affects the gain temperature coefficient of the DAS1150. A high quality metal film resistor 0.1% is recommended.

The gain of the DAS1151 is programmed by loading the proper code into the gain address, as shown in Table 4.

ADDRESS INPUTS		DAS1151
A_1	A_0	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

Table 4. DAS1151 Gain State Truth Table

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