



Frequency Timing Generator for Pentium II Systems

General Description

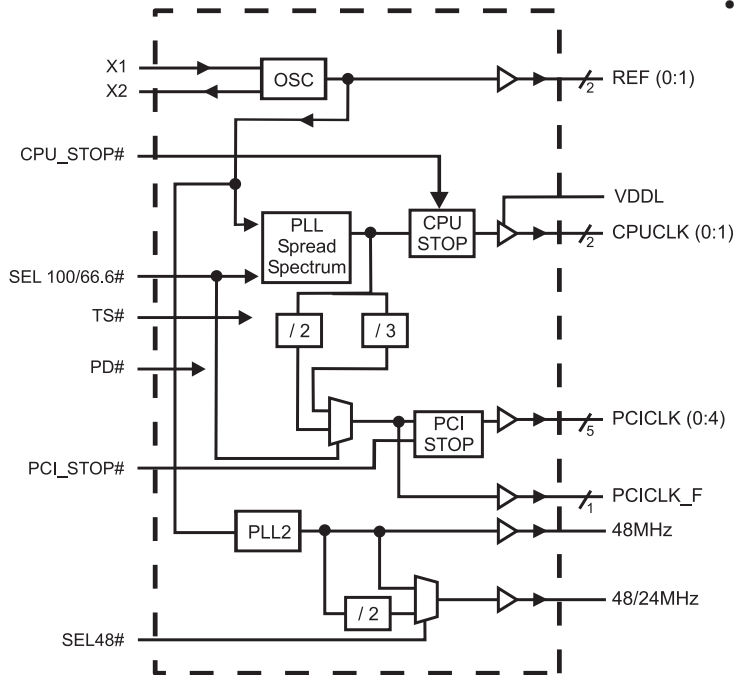
The ICS9248-50

ICS9248-50

Features

- Generates the following system clocks:
 - 2 CPU (2.5V) up to 100MHz.
 - 6 PCI (3.3V) @ 33.3MHz (Includes one free running).
 - 2 REF clks (3.3V) at 14.318MHz.
- Skew characteristics:
 - CPU – CPU ≤ 175 ps
 - PCI – PCI ≤ 500 ps
 - CPU(early) – PCI = 1.5ns – 4ns.
- Supports Spread Spectrum modulation for CPU and PCI clocks, 0.5% down spread
- Efficient Power management scheme through stop clocks and power down modes.
- Uses external 14.318MHz crystal, no external load cap required for CL=18pF crystal.
- 28-pin (209 mil) SSOP package

Block Diagram



Pin Configuration

GNDREF	1	28	VDDREF
X1	2	27	REF0/SEL48#
X2	3	26	REF1/SPREAD#
PCICLK_F	4	25	VDDL
PCICLK0	5	24	CPUCLK1
PCICLK1	6	23	CPUCLK0
GNDPCI	7	22	GNDL
VDDPCI	8	21	GND
PCICLK2	9	20	PCI_STOP#
PCICLK3	10	19	VDD
PCICLK4	11	18	CPU_STOP#
VDD48	12	17	PD#
48MHz	13	16	SEL 100/66#
TS#/48/24MHz	14	15	GND48

28-Pin SSOP

Power Groups



Pin Descriptions

Pin number	Pin name	Type	Description
1	GNDREF	Power	Ground for 14.318 MHz reference clock outputs
2	X1	Input	14.318 MHz crystal input
3	X2	Output	14.318 MHz crystal output
4	PCICLK_F	Output	3.3 V free running PCI clock output, will not be stopped by the PCI_STOP#
5,6,9,10,11	PCICLK (1:5)	Output	3.3 V PCI clock outputs, generating timing requirements for Pentium IIä
7	GNDPCI	Power	Ground for PCI clock outputs
8	VDDPCI	Power	3.3 V power for the PCI clock outputs
12	VDD48	Power	3.3 V power for 48/24 MHz clocks
13	48 MHz	Output	3.3 V 48 MHz clock output, fixed frequency clock typically used with USB devices
14	TS#/48/24MHz	Output	3.3 V 48 or 24 MHz output and Tri-state option, active low = tri state mode for testing, active high = normal operation
15	GND48	Power	Ground for 48/24 MHz clocks
16	SEL 100/66#	Input	control for the frequency of clocks at the CPU & PCICLK output pins. If logic "0" is used the 66.6 MHz frequency is selected. If Logic "1" is used, the 100 MHz frequency is selected. The PCI clock is multiplexed to run at 33.3 MHz for both selected cases.
17	PD#	Input	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
18	CPU_STOP#	Input	Asynchronous active low input pin used to stop the CPUCLK in active low state, all other clocks will continue to run. The CPUCLK will have a "Turnon " latency of at least 3 CPU clocks.
19	VDD	Power	Isolated 3.3 V power for core
20	PCI-Stop#	Input	Synchronous active low input used to stop the PCICLK in active low state. It will not effect PCICLK_F or any other outputs.
21	GND	Power	Isolated ground for core
22	GNDL	Power	Ground for CPU clock outputs
23,24	CPUCLK(1:0)	Output	2.5 V CPU clock outputs
25	VDDL	Power	2.5 V power for CPU clock outputs
26	REF1/SPREAD#	Output	3.3 V 14.318 MHz reference clock output and power-on spread spectrum enable option. Active low = spread spectrum clocking enable. Active high = spread spectrum clocking disable.
27	REF0/SEL48#	Output	3.3 V 14.318 MHz reference clock output and power-on 48/24 MHz select option. Active low = 48 MHz output at pin 14. Active high = 24 MHz output at pin 14.
28	VDDREF	Power	3.3 V power for 14.318 MHz reference clock outputs.



Select Functions

Functionality	CPUCLK	PCI, PCI_F	REF0
Tristate	HI - Z	HI - Z	HI - Z
Testmode	TCLK/2 ¹	TCLK/6 ¹	TCLK ¹

SEL 100/66#	TS#	Function
0	0	Tri-State
0	-	(Reserved)
0	-	(Reserved)
0	1	Active 66.6MHz CPU, 33.3 PCI
1	0	Test Mode
1	-	(Reserved)
1	-	(Reserved)
1	1	Active 100MHz CPU, 33.3 PCI

Power Management

Clock Enable Configuration

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	PCICLK_F	REF	Crystal	VCOs
X	X	0	Low	Low	Low	Stopped	Off	Off
0	0	1	Low	Low	33.3MHz	Running	Running	Running
0	1	1	Low	33.3 MHz	33.3MHz	Running	Running	Running
1	0	1	100/66.6MHz	Low	33.3MHz	Running	Running	Running
1	1	1	100/66.6MHz	33.3 MHz	33.3MHz	Running	Running	Running

ICS9248-50 Power Management Requirements

SIGNAL	SIGNAL STATE	Latency No. of rising edges of free running PCICLK
CPU_STOP#	0 (Disabled) ²	1
	1 (Enabled) ¹	1
PCI_STOP#	0 (Disabled) ²	1
	1 (Enabled) ¹	1
PD#	1 (Normal Operation) ³	3ms
	0 (Power Down) ⁴	2max

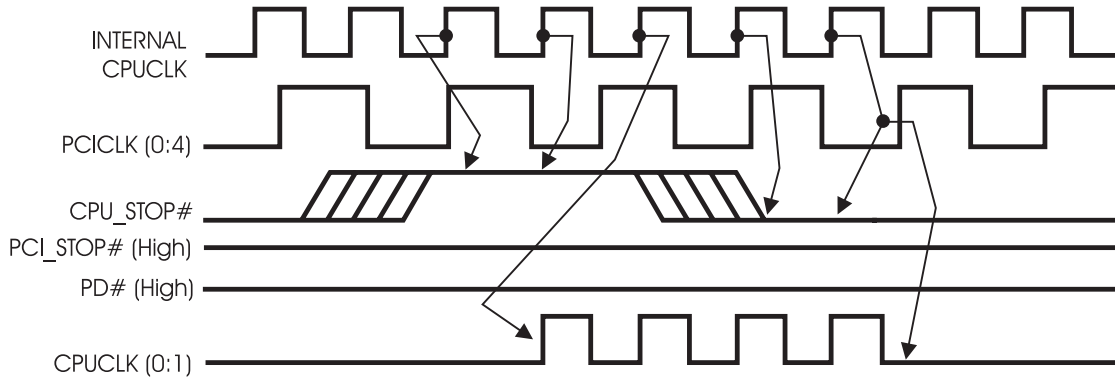
Notes.

1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, PCICLK only.
The REF will be stopped independent of these.



CPU_STOP# Timing Diagram

ICS9248-50

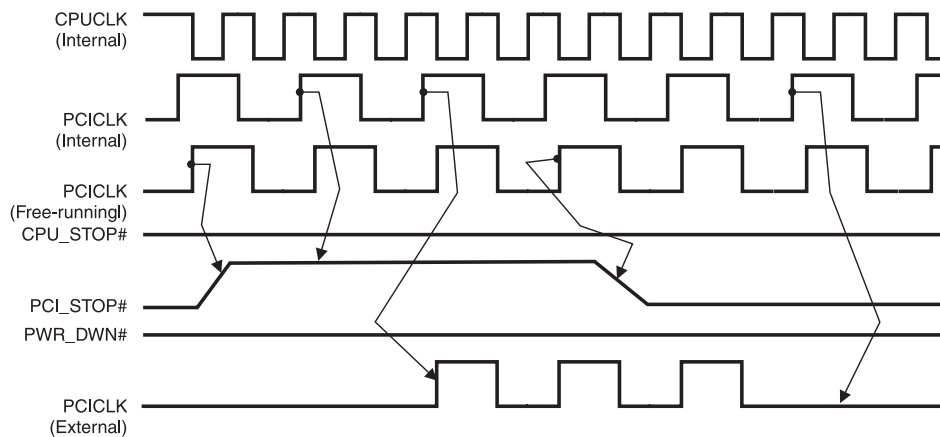


Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the ICS9248-50.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

ICS9248-50
ICS9248-50



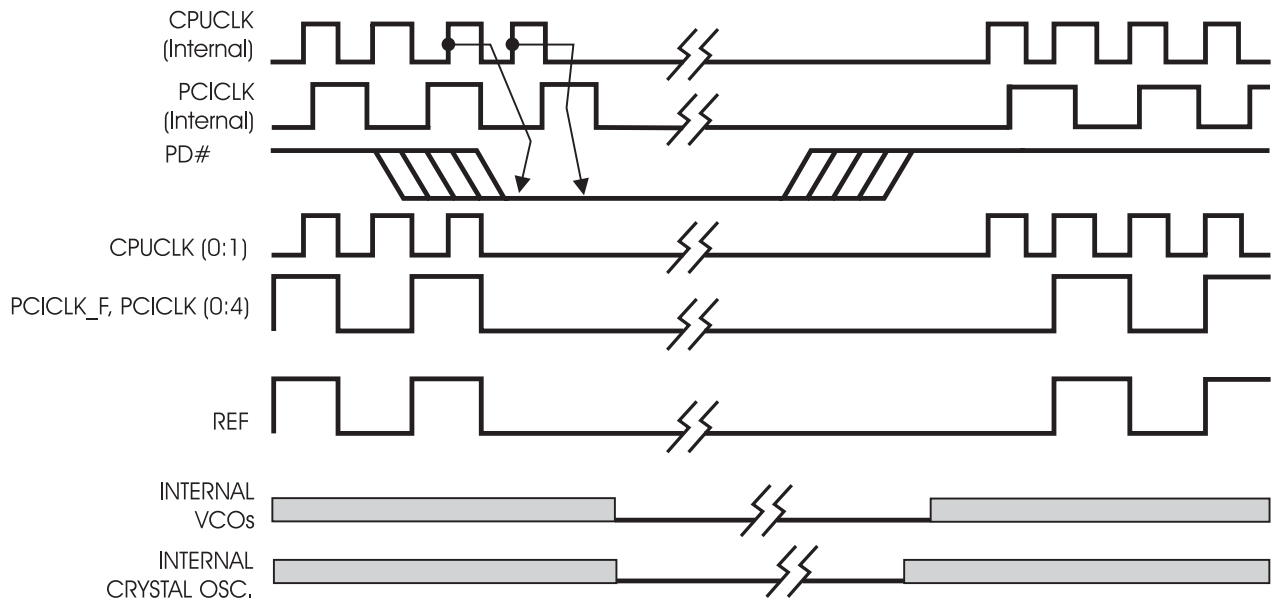
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.



PD# Timing Diagram

ICS9248-50



Notes:

- 1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
- 2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9248.
- 3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.



Absolute Maximum Ratings

$V_{DD} + 0.5\text{ V}$

Ambient Operating Temperature 0°C to +70°C
 Case Temperature 0°C to +115°C
 Storage Temperature -65°C to +150°C

Absolute Maximum Ratings

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}		$V_{SS} - 0.3$		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	5	mA
Input Low Current	I_{IL1}	$V_{IN} = 0\text{ V}$; Inputs with no pull-up resistors	-5	2.0		mA
Input Low Current	I_{IL2}	$V_{IN} = 0\text{ V}$; Inputs with pull-up resistors	-200	-100		mA
Operating Supply Current	$I_{DD3.3OP66}$	$C_L = 0\text{ pF}$; Select @ 66MHz		60	180	mA
	$I_{DD3.3OP100}$	$C_L = 0\text{ pF}$; Select @ 100MHz		66	180	mA
	$I_{DD2.5OP66}$	$C_L = 0\text{ pF}$; Select @ 66.8 MHz		16	72	mA
	$I_{DD2.5OP100}$	$C_L = 0\text{ pF}$; Select @ 100 MHz		23	100	mA
Power Down Supply Current	$I_{DD3.3PD}$	$C_L = 0\text{ pF}$; With input address to Vdd or GND		70	600	mA
Input frequency	F_i	$V_{DD} = 3.3\text{ V}$;	11	14.318	16	MHz
Input Capacitance ¹	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time ¹	T_{trans}	To 1st crossing of target Freq.			3	ms
Clk Stabilization ¹	T_{STAB}	From $V_{DD} = 3.3\text{ V}$ to 1% target Freq.			3	ms
Skew ¹	$T_{CPU-PCI}$	$V_T = 1.5\text{ V}$; $V_{TL} = 1.25\text{ V}$	1.5	3	4	ns



Electrical Characteristics - CPUCLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V _{OH2B}	I _{OH} = -12.0 mA	1.8	2.3		V
Output Low Voltage	V _{OL2B}	I _{OL} = 12 mA		0.31	0.4	V
Output High Current	I _{OH2B}	V _{OH} = 1.7 V			-27	mA
Output Low Current	I _{OL2B}	V _{OL} = 0.7 V	27			mA
Rise Time	t _{r2B} ¹	V _{OL} = 0.4 V, V _{OH} = 2.0 V	0.4	1.15	1.6	ns
Fall Time	t _{f2B} ¹	V _{OH} = 2.0 V, V _{OL} = 0.4 V	0.4	1.4	1.6	ns
Duty Cycle	d _{t2B} ¹	V _T = 1.25 V	44	48	55	%
Skew	t _{sk2B} ¹	V _T = 1.25 V		134	175	ps
Jitter	period(norm)	V _T = 1.25 V; 100MHz	10	10	10.5	ns
Jitter	t _{jcy-cyc2B} ¹	V _T = 1.25 V		186	200	ps
Jitter, Absolute	t _{jabs2B} ¹	V _T = 1.25 V	-250	150	+250	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF/48MHz/24MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V _{OH5}	I _{OH} = -12 mA	2.6	3.1		V
Output Low Voltage	V _{OL5}	I _{OL} = 9 mA		0.17	0.4	V
Output High Current	I _{OH5}	V _{OH} = 2.0 V		-44	-22	mA
Output Low Current	I _{OL5}	V _{OL} = 0.8 V	16	42		mA
Rise Time ¹	t _{r5}	V _{OL} = 0.4 V, V _{OH} = 2.4 V		1.4	4	ns
Fall Time ¹	t _{f5}	V _{OH} = 2.4 V, V _{OL} = 0.4 V		1.1	4	ns
Duty Cycle ¹	d _{t5}	V _T = 1.5 V	45	53	55	%
Jitter ¹	t _{j1s5}	V _T = 1.5 V, REF		185	250	ps
	t _{jabs5}	V _T = 1.5 V, REF		385	800	ps
Jitter ¹	t _{j1s5}	V _T = 1.5 V, 48 MHz		169	250	ps
	t _{jabs5}	V _T = 1.5 V, 48 MHz		469	800	ps



Electrical Characteristics - PCICLK

TA = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF

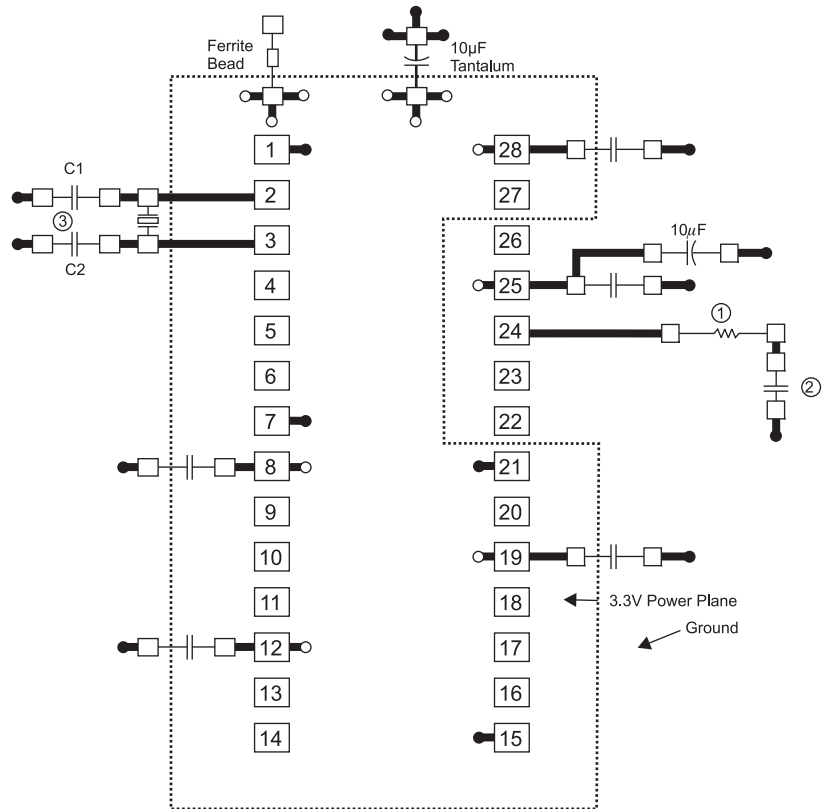
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V _{OH1}	I _{OH} = -18 mA	2.1	3.3		V
Output Low Voltage	V _{OL1}	I _{OL} = 9.4 mA		0.1	0.4	V
Output High Current	I _{OH1}	V _{OH} = 2.0 V			-22	mA
Output Low Current	I _{OL1}	V _{OL} = 0.8 V	16		57	mA
Rise Time ¹	t _{r1}	V _{OL} = 0.4 V, V _{OH} = 2.4 V		1.6	2	ns
Fall Time ¹	t _{f1}	V _{OH} = 2.4 V, V _{OL} = 0.4 V		1.8	2	ns
Duty Cycle ¹	d _{t1}	V _T = 1.5 V	45	50	55	%
Skew ¹	t _{sk1}	V _T = 1.5 V		222	500	ps
Jitter ¹	t _{j_{cyc-cyc}}	V _T = 1.5 V		186	500	ps
	t _{j1s}	V _T = 1.5 V		52	150	ps
	t _{jabs}	V _T = 1.5 V		200	500	ps

¹Guaranteed by design, not 100% tested in production.



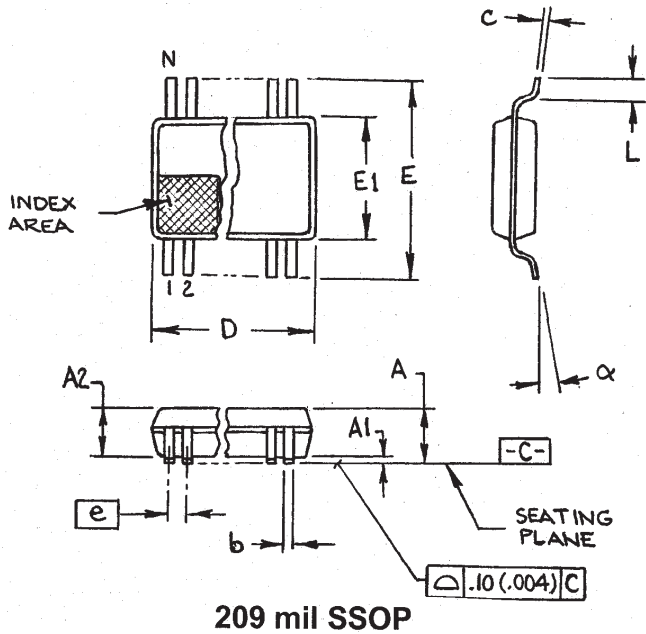
General Layout Precautions:

Notes:



- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads

Capacitor Values:



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	2.00	-	.079
A1	0.05	-	.002	-
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	2.70	3.30	.106	.130
14	5.90	6.50	.232	.256
16	5.90	6.50	.232	.256
18	6.90	7.50	.271	.295
20	6.90	7.50	.271	.295
22	7.90	8.50	.311	.335
24	7.90	8.50	.311	.335
28	9.90	10.50	.390	.413
30	9.90	10.50	.390	.413
38	12.30	12.90	.484	.508

MO-150 JEDEC
Doc.# 10-0033
6/7/00 Rev B

Ordering Information

9248yF-50-T

XXXX y F - PPP - T

