National Semiconductor

October 1992

DM54161/DM74161/DM74163 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 161 and 163 are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear function for the 161 is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the 163 is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 163 are also permissible, regardless of the logic levels on the clock, enable, or load inputs.

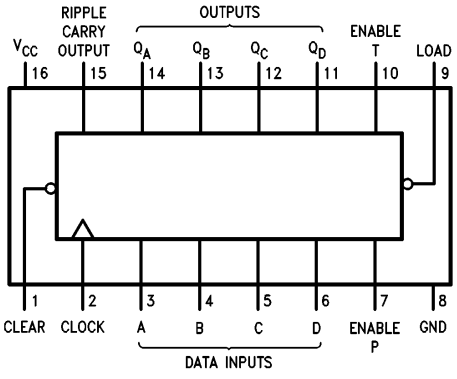
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the 161 through 163 may occur, regardless of the logic level on the clock.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

Connection Diagram

Dual-In-Line Package



TL/F/6551–1

Order Number DM54161J, DM54161W, DM74161N or DM74163N
See NS Package Number J16A, N16E or W16A

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54161			DM74161 and 163			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 6)	Data	20			20			ns
		Enable P	34			34			
		Load	25			25			
		Clear (Note 5)	20			20			
t_H	Hold Time (Note 6)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Enable T			80	μA
			Clock			80	
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable T			−3.2	mA
			Clock			−3.2	
			Others			−1.6	

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−20		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54			85	mA
			DM74		59	94	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)	DM54			91	mA
			DM74		63	101	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with the LOAD high, then again with the LOAD low, with all inputs high and all outputs open.

Note 4: I_{CCL} is measured with the CLOCK high, then again with the CLOCK input low, with all inputs low and all outputs open.

Note 5: Applies to 163 which has synchronous clear inputs.

Note 6: T_A = 25°C and V_{CC} = 5V.

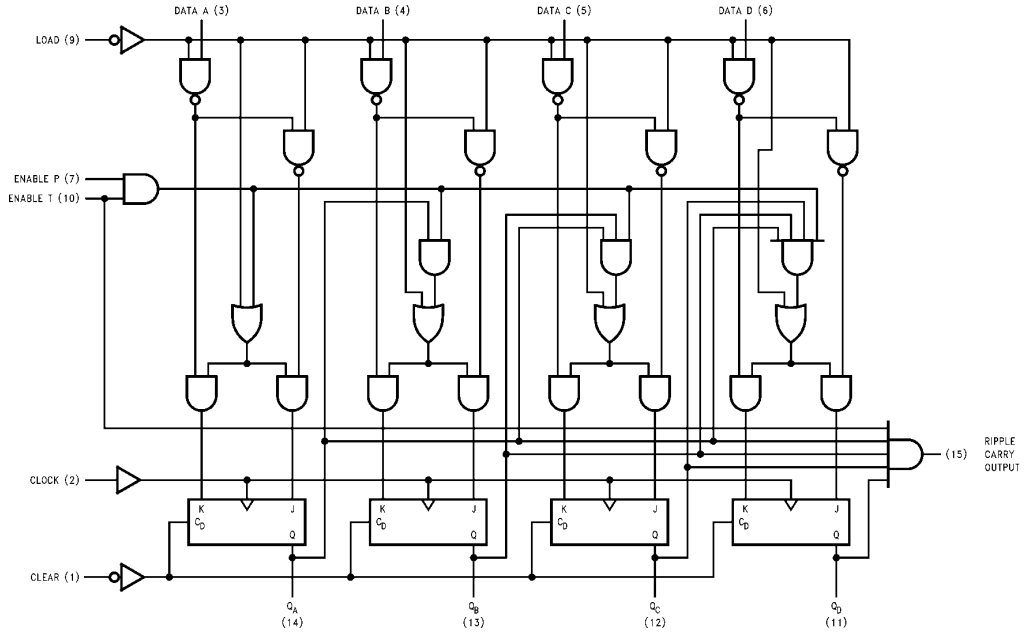
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock (Load High) to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock (Load High) to Q		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock (Load Low) to Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock (Load Low) to Q		29	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear (Note 7) to Q		38	ns

Note 7: Propagation delay for clearing is measured from the clear input for the 161 or from the clock input transition for the 163.

Logic Diagrams

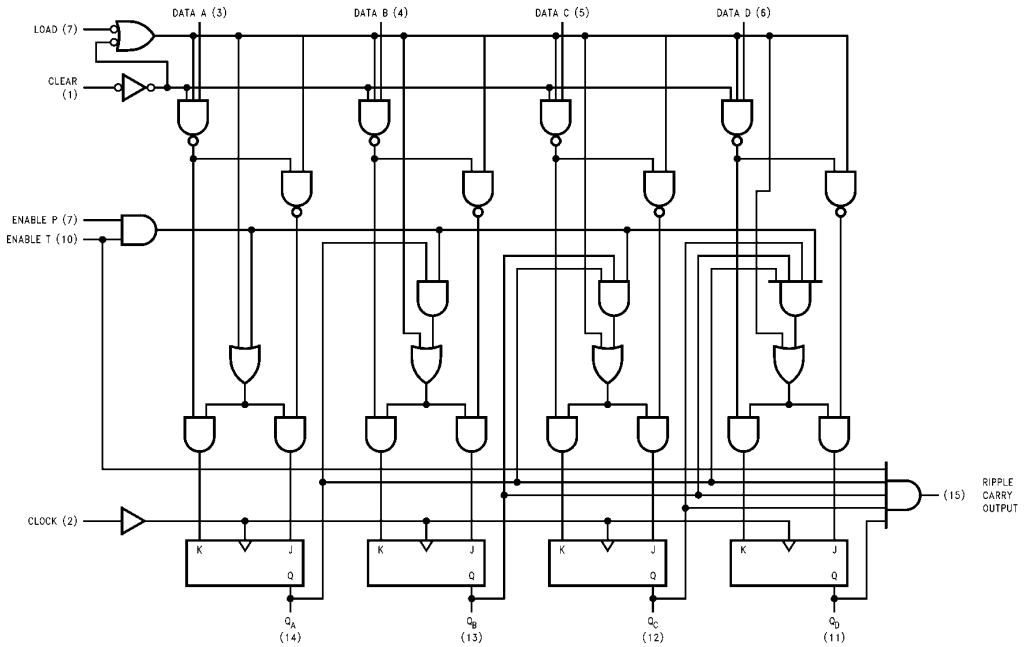
161



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Logic Diagrams (Continued)

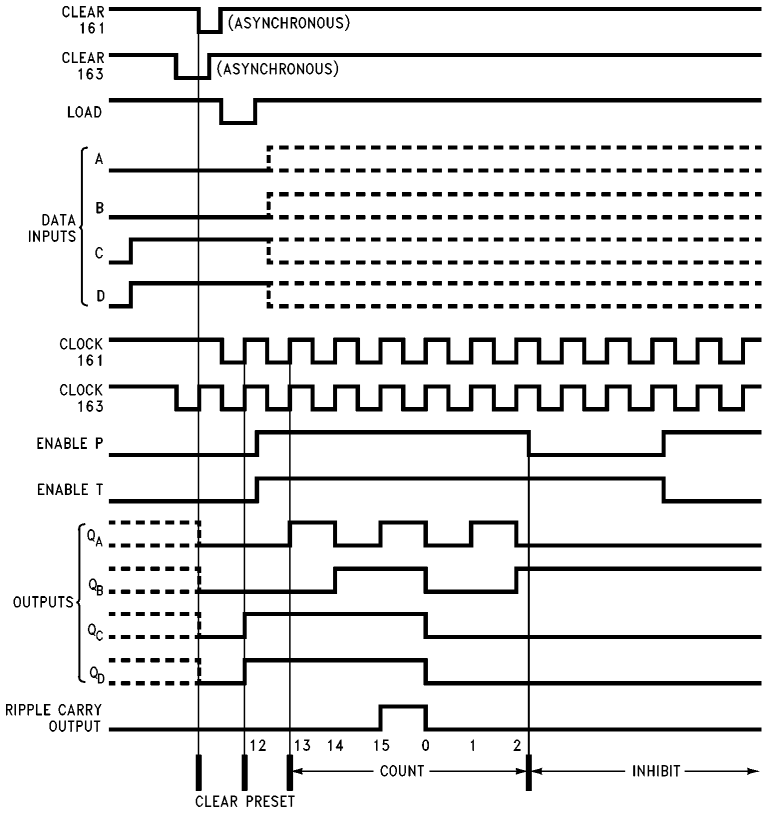
163



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Logic Diagrams (Continued)

161, 163 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences

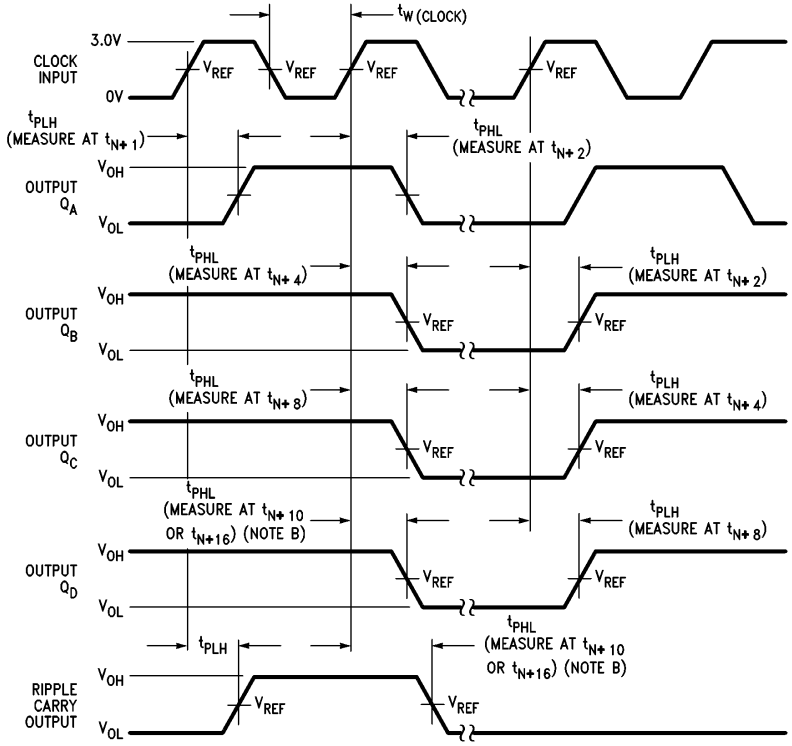


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(1) Clear outputs to zero
(2) Reset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

Parameter Measurement Information

Switching Time Waveforms



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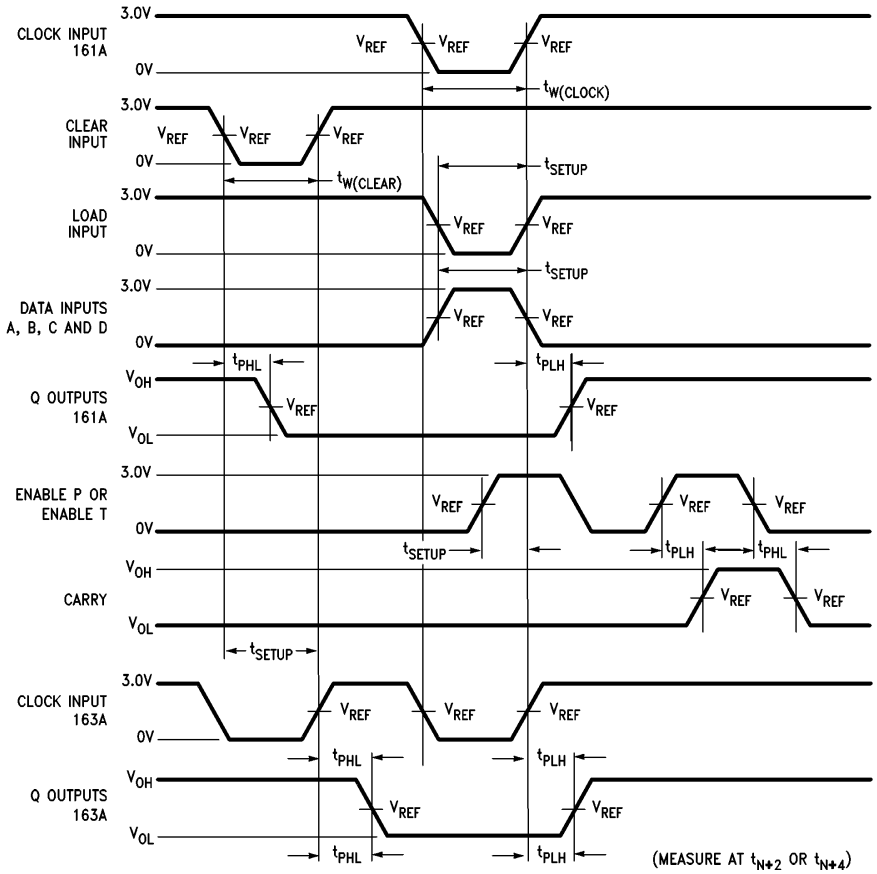
Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$. For 161 and 163, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+16} for 161, 163 where t_n is the bit time when all outputs are low.

Note C: For 161 and 163, $V_{REF} = 1.5V$.

Parameter Measurement Information (Continued)

Switching Time Waveforms



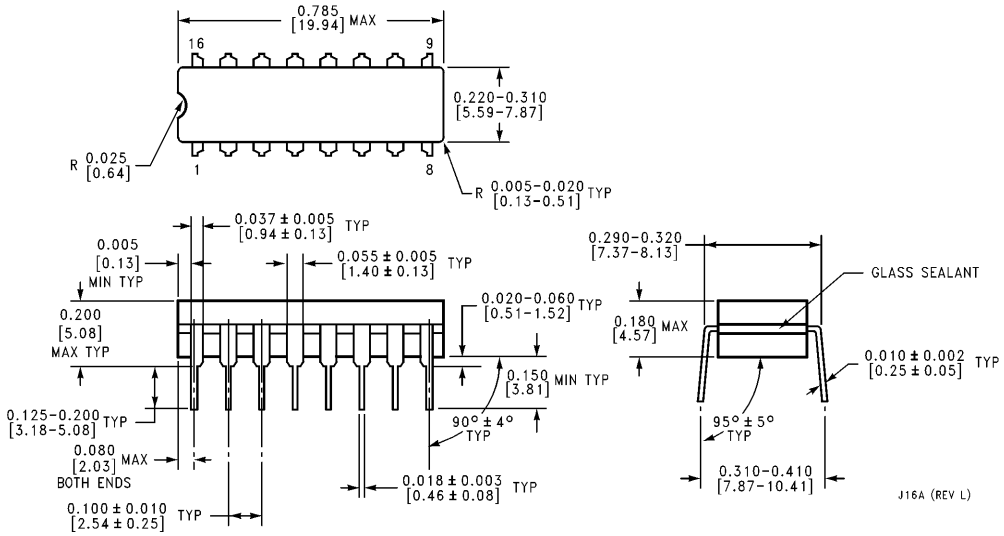
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Note A: The input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$. For 161 and 163, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

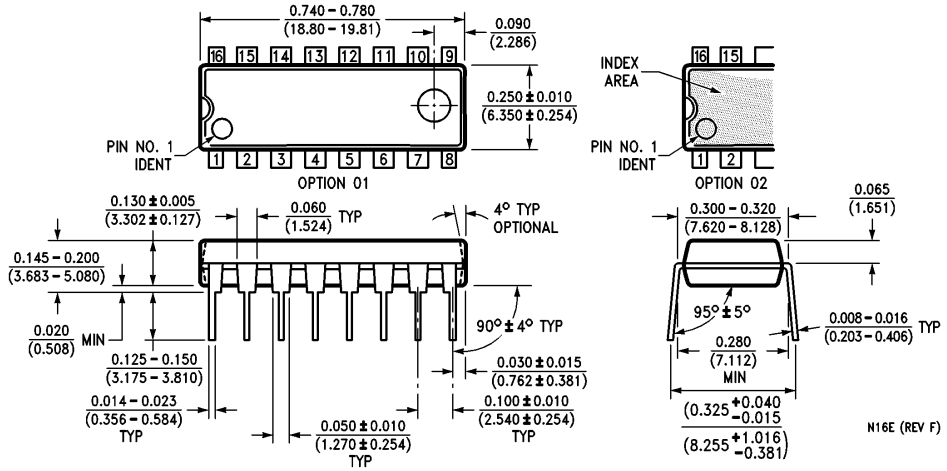
Note B: Enable P and enable T setup times are measured at t_{n+0}.

Note C: For 161 and 163, $V_{REF} = 1.5V$.

Physical Dimensions inches (millimeters)

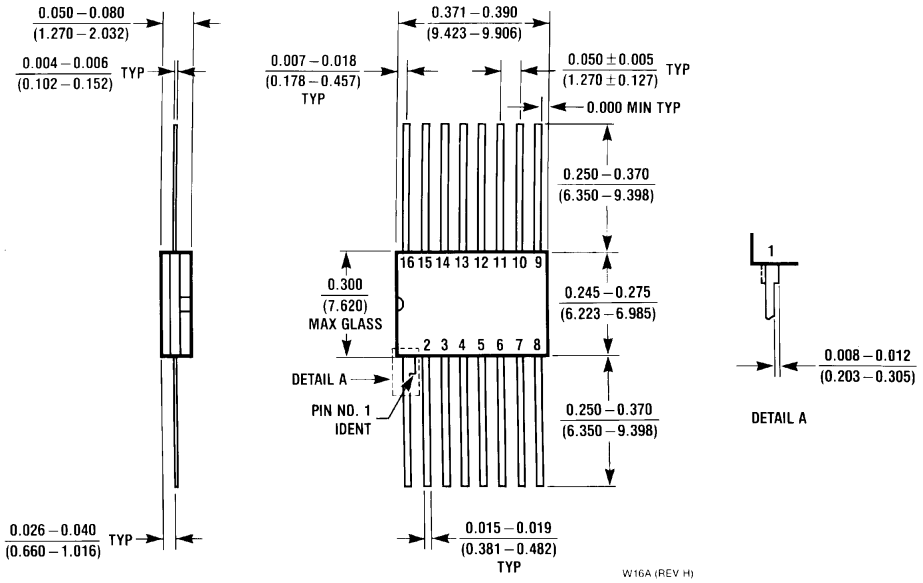


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54161J or DM54163AJ
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74161N or DM74163N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number DM54161W or DM54163AW
NS Package Number W16A

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