

## FEATURES

- Latch-up proof
- 2.9 pF off source capacitance
- 34 pF off drain capacitance
- 0.2 pC charge injection
- Low on resistance: 160  $\Omega$  typical
- $\pm 9$  V to  $\pm 22$  V dual-supply operation
- 9 V to 40 V single-supply operation
- 48 V supply maximum ratings
- Fully specified at  $\pm 15$  V,  $\pm 20$  V, +12 V, and +36 V
- $V_{SS}$  to  $V_{DD}$  analog signal range
- Human body model (HBM) ESD rating
  - 8 kV I/O port to supplies
  - 2 kV I/O port to I/O port
  - 8 kV all other pins
- Supports defense and aerospace applications (AQEC standard)
- Military temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Controlled manufacturing baseline
- One assembly and test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

## APPLICATIONS

- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Audio and video switching
- Communication systems

## GENERAL DESCRIPTION

The [ADG5208-EP/ADG5209-EP](#) are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The [ADG5208-EP](#) switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The [ADG5209-EP](#) switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1.

An EN input on both devices enables or disables the device. When EN is disabled, all channels switch off. The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make these devices suitable for video signal switching.

## FUNCTIONAL BLOCK DIAGRAM

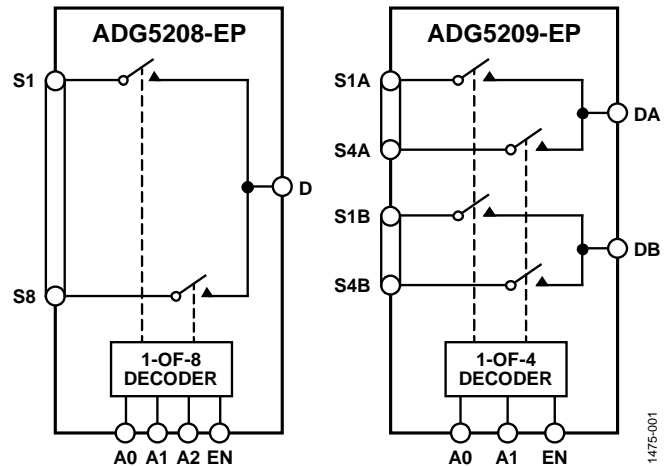


Figure 1.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked.

The [ADG5208-EP/ADG5209-EP](#) do not have  $V_L$  pins; instead, the logic power supply is generated internally by an on-chip voltage generator.

Additional application and technical information can be found in the [ADG5208/ADG5209](#) data sheet.

## PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up.  
A dielectric trench separates the P and N channel transistors to prevent latch-up even under severe overvoltage conditions.
2. 0.2 pC Charge Injection.
3. Dual-Supply Operation.  
For applications where the analog signal is bipolar, the [ADG5208-EP/ADG5209-EP](#) can be operated from dual supplies of up to  $\pm 22$  V.
4. Single-Supply Operation.  
For applications where the analog signal is unipolar, the [ADG5208-EP/ADG5209-EP](#) can be operated from a single rail power supply of up to 40 V.
5. 3 V Logic-Compatible Digital Inputs.  
 $V_{INH} = 2.0$  V,  $V_{INL} = 0.8$  V.
6. No  $V_L$  Logic Power Supply Required.

Rev. C

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## REVISION HISTORY

### 11/2017—Rev. B to Rev. C

Changes to Ordering Guide .....	19
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### 8/2014—Rev. A to Rev. B

Changes to Table 1.....	3
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### 10/2013—Rev. 0 to Rev. A

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### 7/2013—Revision 0: Initial Version

## SPECIFICATIONS

### ±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	160 200	250	280	$\Omega$ typ $\Omega$ max	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 26 $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	3.5			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	8	9	10	$\Omega$ max	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$
	40			$\Omega$ typ	
	50	65	70	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.005$ $\pm 0.1$	$\pm 0.2$	$\pm 0.4$	nA typ nA max	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ ; see Figure 28
Drain Off Leakage, $I_D$ (Off)	$\pm 0.005$ $\pm 0.1$	$\pm 0.4$	$\pm 1.4$	nA typ nA max	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ ; see Figure 28
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.01$ $\pm 0.2$	$\pm 0.5$	$\pm 1.4$	nA typ nA max	$V_S = V_D = \pm 10\text{ V}$ ; see Figure 25
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	$V_{IN} = V_{GND}$ or $V_{DD}$
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	3			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	150			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$ ; see Figure 31
	180	210	245	ns max	
$t_{ON}$ (EN)	125			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$ ; see Figure 33
	150	185	215	ns max	
$t_{OFF}$ (EN)	160			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$ ; see Figure 33
	185	210	230	ns max	
Break-Before-Make Time Delay, $t_D$	55			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
Charge Injection, $Q_{INJ}$	0.2		20	ns min pC typ	$V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 32 $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 34
Off Isolation	-86			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 29
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27
-3 dB Bandwidth					$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 30
	ADG5208-EP	110		MHz typ	
ADG5209-EP	240			MHz typ	
Insertion Loss	-6.4			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 30
$C_S$ (Off)	2.9			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)					$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
	ADG5208-EP	34		pF typ	
ADG5209-EP	17			pF typ	

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
$C_D$ (On), $C_S$ (On)					
ADG5208-EP	37			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
ADG5209-EP	21			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
POWER REQUIREMENTS					$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
$I_{DD}$	45		80	$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
	55			$\mu\text{A}$ max	
$I_{SS}$	0.001		1	$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
				$\mu\text{A}$ max	
$V_{DD}/V_{SS}$			$\pm 9/\pm 22$	V min/V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

### ±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	140			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 26
	160	200	230	$\Omega$ max	$V_{DD} = +18\text{ V}$ , $V_{SS} = -18\text{ V}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	3.5			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -1\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	8	9	10	$\Omega$ max	
	34			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -1\text{ mA}$
	45	55	60	$\Omega$ max	
LEAKAGE CURRENTS					$V_{DD} = +22\text{ V}$ , $V_{SS} = -22\text{ V}$
Source Off Leakage, $I_S$ (Off)	$\pm 0.005$			nA typ	$V_S = \pm 15\text{ V}$ , $V_D = \mp 15\text{ V}$ ; see Figure 28
	$\pm 0.1$	$\pm 0.2$	$\pm 0.4$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.005$			nA typ	$V_S = \pm 15\text{ V}$ , $V_D = \mp 15\text{ V}$ ; see Figure 28
	$\pm 0.1$	$\pm 0.4$	$\pm 1.4$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.01$			nA typ	$V_S = V_D = \pm 15\text{ V}$ ; see Figure 25
	$\pm 0.2$	$\pm 0.5$	$\pm 1.4$	nA max	
DIGITAL INPUTS					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	3			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
Transition Time, $t_{TRANSITION}$	140			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	170	195	220	ns max	$V_S = 10\text{ V}$ ; see Figure 31
$t_{ON}$ (EN)	120			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	140	170	195	ns max	$V_S = 10\text{ V}$ ; see Figure 33
$t_{OFF}$ (EN)	160			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	185	205	220	ns max	$V_S = 10\text{ V}$ ; see Figure 33
Break-Before-Make Time Delay, $t_D$	45			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
			20	ns min	$V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 32
Charge Injection, $Q_{INJ}$	0.4			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 34
Off Isolation	-86			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 29
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
-3 dB Bandwidth					$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; see Figure 30
ADG5208-EP	121			MHz typ	
ADG5209-EP	225			MHz typ	
Insertion Loss	-5.6			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 30
$C_S$ (Off)	2.8			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (Off)					
ADG5208-EP	33			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
ADG5209-EP	17			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)					
ADG5208-EP	36			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
ADG5209-EP	21			pF typ	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	50			$\mu\text{A}$ typ	$V_{DD} = +22 \text{ V}$ , $V_{SS} = -22 \text{ V}$ Digital inputs = 0 V or $V_{DD}$
	70		120	$\mu\text{A}$ max	
$I_{SS}$	0.001			$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
			1	$\mu\text{A}$ max	
$V_{DD}/V_{SS}$			$\pm 9/\pm 22$	V min/V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

## 12 V SINGLE SUPPLY

$V_{DD} = 12 \text{ V} \pm 10\%$ ,  $V_{SS} = 0 \text{ V}$ , GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance, $R_{ON}$	350			$\Omega$ typ	$V_S = 0 \text{ V}$ to 10 V, $I_S = -1 \text{ mA}$ ; see Figure 26
	500	610	700	$\Omega$ max	$V_{DD} = 10.8 \text{ V}$ , $V_{SS} = 0 \text{ V}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	5			$\Omega$ typ	$V_S = 0 \text{ V}$ to 10 V, $I_S = -1 \text{ mA}$
	20	22	24	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	160			$\Omega$ typ	$V_S = 0 \text{ V}$ to 10 V, $I_S = -1 \text{ mA}$
	280	335	370	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.005$			nA typ	$V_{DD} = 13.2 \text{ V}$ , $V_{SS} = 0 \text{ V}$ $V_S = 1 \text{ V}/10 \text{ V}$ , $V_D = 10 \text{ V}/1 \text{ V}$ ; see Figure 28
	$\pm 0.1$	$\pm 0.2$	$\pm 0.4$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.005$			nA typ	$V_S = 1 \text{ V}/10 \text{ V}$ , $V_D = 10 \text{ V}/1 \text{ V}$ ; see Figure 28
	$\pm 0.1$	$\pm 0.4$	$\pm 1.4$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.01$			nA typ	$V_S = V_D = 1 \text{ V}/10 \text{ V}$ ; see Figure 25
	$\pm 0.2$	$\pm 0.5$	$\pm 1.4$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	3			pF typ	

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{\text{TRANSITION}}$	200 250			ns typ ns max	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ $V_S = 8 \text{ V}$ ; see Figure 31
$t_{\text{ON}}$ (EN)	180 225	295	335	ns typ ns max	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ $V_S = 8 \text{ V}$ ; see Figure 33
$t_{\text{OFF}}$ (EN)	165 200	280	320	ns typ ns max	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ $V_S = 8 \text{ V}$ ; see Figure 33
Break-Before-Make Time Delay, $t_D$	95			ns typ ns min	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$ $V_{S1} = V_{S2} = 8 \text{ V}$ ; see Figure 32
Charge Injection, $Q_{\text{INJ}}$	0.2		45	pC typ	$V_S = 6 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; see Figure 34
Off Isolation	-86			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 29
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 27
-3 dB Bandwidth					$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; see Figure 30
ADG5208-EP	95			MHz typ	
ADG5209-EP	180			MHz typ	
Insertion Loss	-8.9			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 30
$C_S$ (Off)	3.3			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (Off)					
ADG5208-EP	38			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
ADG5209-EP	19			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)					
ADG5208-EP	41			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
ADG5209-EP	24			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{\text{DD}}$	40 50			$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{\text{DD}} = 13.2 \text{ V}$ Digital inputs = 0 V or $V_{\text{DD}}$
$V_{\text{DD}}$			9/40	V min/V max	$\text{GND} = 0 \text{ V}$ , $V_{\text{SS}} = 0 \text{ V}$

<sup>1</sup> Guaranteed by design; not subject to production test.

### 36 V SINGLE SUPPLY

$V_{\text{DD}} = 36 \text{ V} \pm 10\%$ ,  $V_{\text{SS}} = 0 \text{ V}$ ,  $\text{GND} = 0 \text{ V}$ , unless otherwise noted.

Table 4.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{\text{DD}}$	V	
On Resistance, $R_{\text{ON}}$	150			$\Omega$ typ	$V_S = 0 \text{ V}$ to 30 V, $I_S = -1 \text{ mA}$ ; see Figure 26
On-Resistance Match Between Channels, $\Delta R_{\text{ON}}$	170 3.5	215	245	$\Omega$ max $\Omega$ typ	$V_{\text{DD}} = 32.4 \text{ V}$ , $V_{\text{SS}} = 0 \text{ V}$ $V_S = 0 \text{ V}$ to 30 V, $I_S = -1 \text{ mA}$
On-Resistance Flatness, $R_{\text{FLAT(ON)}}$	8 35 55	9 65	10 70	$\Omega$ max $\Omega$ typ $\Omega$ max	$V_S = 0 \text{ V}$ to 30 V, $I_S = -1 \text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.005$ $\pm 0.1$			nA typ nA max	$V_{\text{DD}} = 39.6 \text{ V}$ , $V_{\text{SS}} = 0 \text{ V}$ $V_S = 1 \text{ V}/30 \text{ V}$ , $V_D = 30 \text{ V}/1 \text{ V}$ ; see Figure 28

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
Drain Off Leakage, $I_D$ (Off)	±0.005			nA typ	$V_S = 1\text{ V}/30\text{ V}$ , $V_D = 30\text{ V}/1\text{ V}$ ; see Figure 28
Channel On Leakage, $I_D$ (On), $I_S$ (On)	±0.1 ±0.01 ±0.2	±0.4 ±0.5	±1.4 ±1.4	nA max nA typ nA max	$V_S = V_D = 1\text{ V}/30\text{ V}$ ; see Figure 25
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	$V_{IN} = V_{GND}$ or $V_{DD}$
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.002		±0.1	µA typ µA max	
Digital Input Capacitance, $C_{IN}$	3			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
Transition Time, $t_{TRANSITION}$	170 205			ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$ ; see Figure 31
$t_{ON}$ (EN)	150 180	225 195	235 215	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$ ; see Figure 33
$t_{OFF}$ (EN)	180 225	195 225	215 230	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$ ; see Figure 33
Break-Before-Make Time Delay, $t_D$	55			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
Charge Injection, $Q_{INJ}$	0.3		20	ns min pC typ	$V_{S1} = V_{S2} = 18\text{ V}$ ; see Figure 32
Off Isolation	-86			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 29
Channel-to-Channel Crosstalk	-80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27
-3 dB Bandwidth					$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 30
ADG5208-EP	105			MHz typ	
ADG5209-EP	195			MHz typ	
Insertion Loss	-6.2			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 30
$C_S$ (Off)	2.7			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)					
ADG5208-EP	32			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$
ADG5209-EP	16			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (On), $C_S$ (On)					
ADG5208-EP	35			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$
ADG5209-EP	20			pF typ	$V_S = 18\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	80 100			µA typ µA max	$V_{DD} = 39.6\text{ V}$ Digital inputs = 0 V or $V_{DD}$
$V_{DD}$			155 9/40	V min/V max	$GND = 0\text{ V}$ , $V_{SS} = 0\text{ V}$

<sup>1</sup> Guaranteed by design; not subject to production test.

**CONTINUOUS CURRENT PER CHANNEL, Sx, D, OR Dx**

**Table 5. ADG5208-EP**

<b>Parameter</b>	<b>25°C</b>	<b>85°C</b>	<b>125°C</b>	<b>Unit</b>
<b>CONTINUOUS CURRENT, Sx OR D</b>				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^\circ\text{C/W}$ )	40	24	14.5	mA maximum
LFCSP ( $\theta_{JA} = 30.4^\circ\text{C/W}$ )	69	37	18	mA maximum
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^\circ\text{C/W}$ )	42	26.5	14.5	mA maximum
LFCSP ( $\theta_{JA} = 30.4^\circ\text{C/W}$ )	75	40	18	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^\circ\text{C/W}$ )	28	19	12	mA maximum
LFCSP ( $\theta_{JA} = 30.4^\circ\text{C/W}$ )	40	25	14.5	mA maximum
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^\circ\text{C/W}$ )	40	26	14.5	mA maximum
LFCSP ( $\theta_{JA} = 30.4^\circ\text{C/W}$ )	72	39	18	mA maximum

**Table 6. ADG5209-EP**

<b>Parameter</b>	<b>25°C</b>	<b>85°C</b>	<b>125°C</b>	<b>Unit</b>
<b>CONTINUOUS CURRENT, Sx OR Dx</b>				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^\circ\text{C/W}$ )	29	19	12	mA maximum
LFCSP ( $\theta_{JA} = 30.4^\circ\text{C/W}$ )	51	30	16	mA maximum
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^\circ\text{C/W}$ )	30	20	12.5	mA maximum
LFCSP ( $\theta_{JA} = 30.4^\circ\text{C/W}$ )	55	32	17	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^\circ\text{C/W}$ )	20	14	10	mA maximum
LFCSP ( $\theta_{JA} = 30.4^\circ\text{C/W}$ )	29	20	12.5	mA maximum
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$				
TSSOP ( $\theta_{JA} = 112.6^\circ\text{C/W}$ )	30	20	12.5	mA maximum
LFCSP ( $\theta_{JA} = 30.4^\circ\text{C/W}$ )	54	31	17	mA maximum



## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 7.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	48 V
$V_{DD}$ to GND	-0.3 V to +48 V
$V_{SS}$ to GND	+0.3 V to -48 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, $S_x$ , D, or $D_x$ Pins ADG5208-EP	126 mA (pulsed at 1 ms, 10% duty cycle maximum)
ADG5209-EP	92 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, $S_x$ , D, or $D_x$ Pins <sup>2</sup>	Data + 15%
Temperature Range	
Operating	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Storage	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Junction Temperature	$150^\circ\text{C}$
Thermal Impedance, $\theta_{JA}$	
16-Lead TSSOP (4-Layer Board)	$112.6^\circ\text{C}/\text{W}$
16-Lead LFCSP (4-Layer Board)	$30.4^\circ\text{C}/\text{W}$
Reflow Soldering Peak Temperature, Pb Free	$260(+0/-5)^\circ\text{C}$
HBM ESD	
I/O Port to Supplies	8 kV
I/O Port to I/O Port	2 kV
All Other Pins	8 kV

<sup>1</sup> Overvoltages at the  $A_x$ , EN,  $S_x$ , D, and  $D_x$  pins are clamped by internal diodes. Limit current to the maximum ratings given.

<sup>2</sup> See Table 5 and Table 6.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

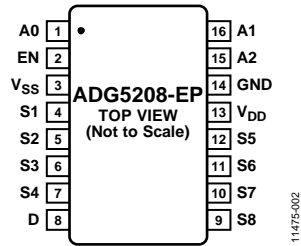


Figure 2. ADG5208-EP Pin Configuration (TSSOP)

Table 8. ADG5208-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, the Ax logic inputs determine the on switches.
3	V <sub>SS</sub>	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1	Source Terminal 1. This pin can be an input or an output.
5	S2	Source Terminal 2. This pin can be an input or an output.
6	S3	Source Terminal 3. This pin can be an input or an output.
7	S4	Source Terminal 4. This pin can be an input or an output.
8	D	Drain Terminal. This pin can be an input or an output.
9	S8	Source Terminal 8. This pin can be an input or an output.
10	S7	Source Terminal 7. This pin can be an input or an output.
11	S6	Source Terminal 6. This pin can be an input or an output.
12	S5	Source Terminal 5. This pin can be an input or an output.
13	V <sub>DD</sub>	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input.
16	A1	Logic Control Input.

Table 9. ADG5208-EP Truth Table

A2	A1	A0	EN	On Switch
X <sup>1</sup>	X <sup>1</sup>	X <sup>1</sup>	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

<sup>1</sup> X is don't care.

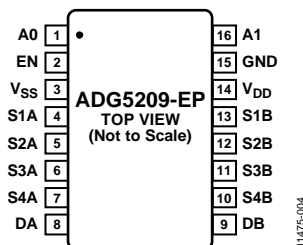


Figure 3. ADG5209-EP Pin Configuration (TSSOP)

Table 10. ADG5209-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine the on switches.
3	V <sub>SS</sub>	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1A	Source Terminal 1A. This pin can be an input or an output.
5	S2A	Source Terminal 2A. This pin can be an input or an output.
6	S3A	Source Terminal 3A. This pin can be an input or an output.
7	S4A	Source Terminal 4A. This pin can be an input or an output.
8	DA	Drain Terminal A. This pin can be an input or an output.
9	DB	Drain Terminal B. This pin can be an input or an output.
10	S4B	Source Terminal 4B. This pin can be an input or an output.
11	S3B	Source Terminal 3B. This pin can be an input or an output.
12	S2B	Source Terminal 2B. This pin can be an input or an output.
13	S1B	Source Terminal 1B. This pin can be an input or an output.
14	V <sub>DD</sub>	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input.

Table 11. ADG5209-EP Truth Table

A1	A0	EN	On Switch Pair
X <sup>1</sup>	X <sup>1</sup>	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

<sup>1</sup> X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

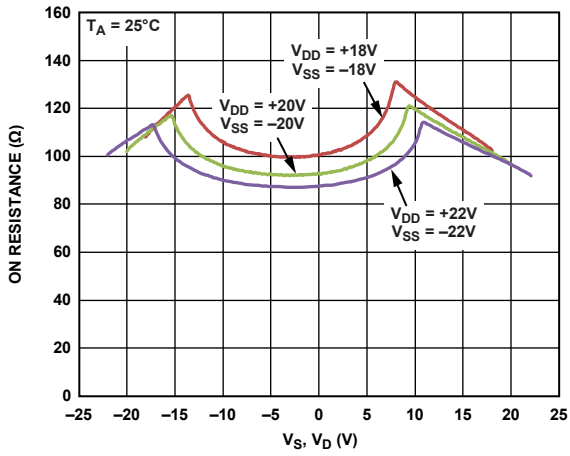


Figure 4.  $R_{ON}$  as a Function of  $V_S, V_D$  ( $\pm 20$  V Dual Supply)

11475-006

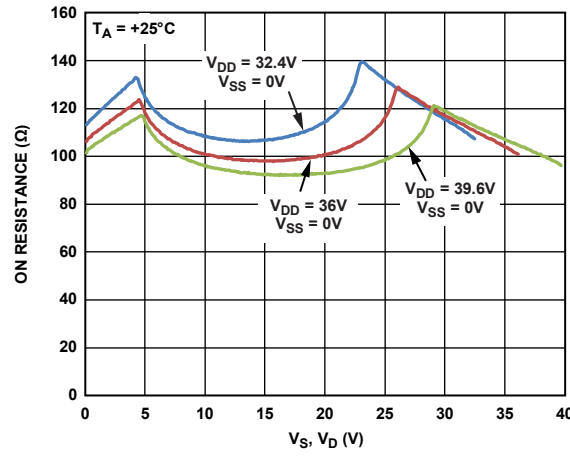


Figure 7.  $R_{ON}$  as a Function of  $V_S, V_D$  (36 V Single Supply)

11475-009

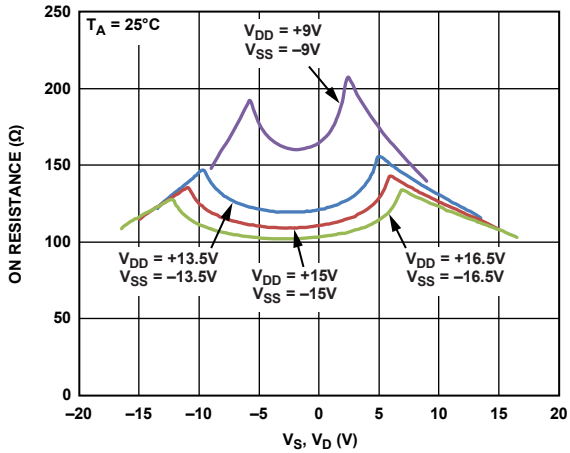


Figure 5.  $R_{ON}$  as a Function of  $V_S, V_D$  ( $\pm 15$  V Dual Supply)

11475-007

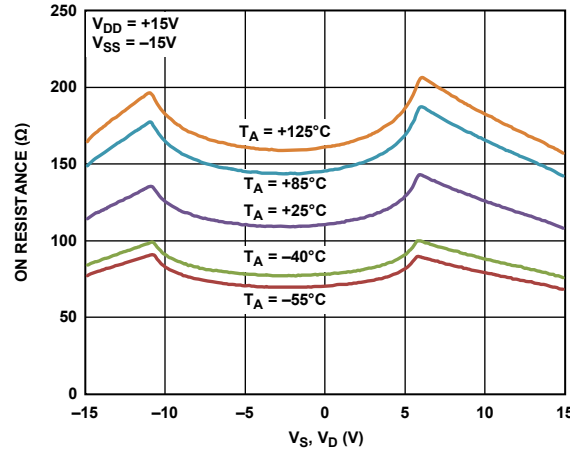


Figure 8.  $R_{ON}$  as a Function of  $V_S, V_D$  for Different Temperatures,  $\pm 15$  V Dual Supply

11475-008

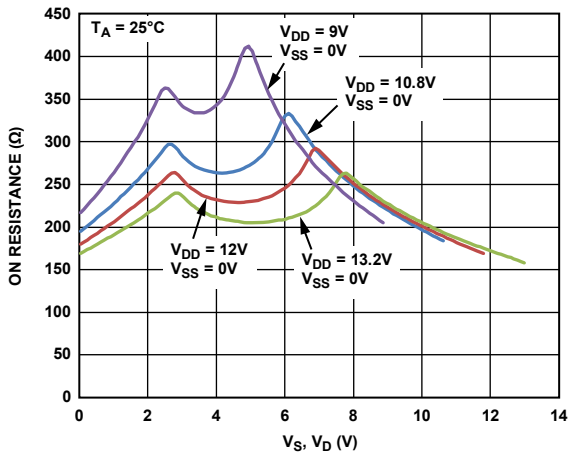


Figure 6.  $R_{ON}$  as a Function of  $V_S, V_D$  (12 V Single Supply)

11475-005

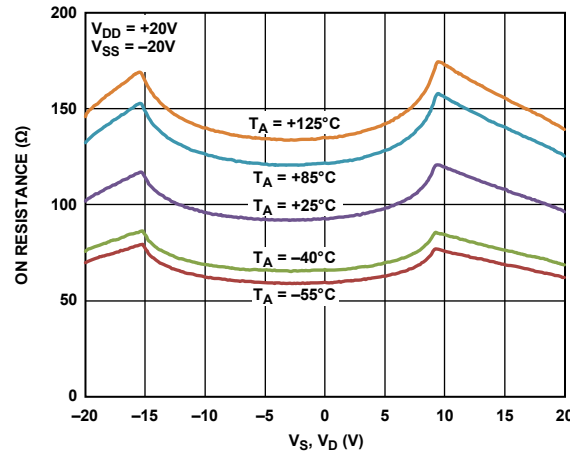


Figure 9.  $R_{ON}$  as a Function of  $V_S, V_D$  for Different Temperatures,  $\pm 20$  V Dual Supply

11475-100

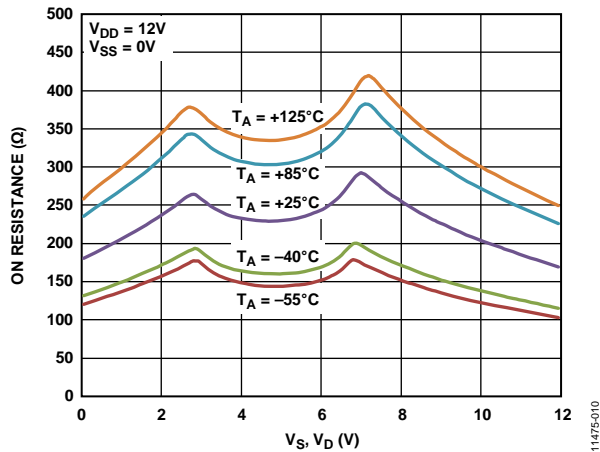


Figure 10.  $R_{ON}$  as a Function of  $V_S$ ,  $V_D$  for Different Temperatures, 12 V Single Supply

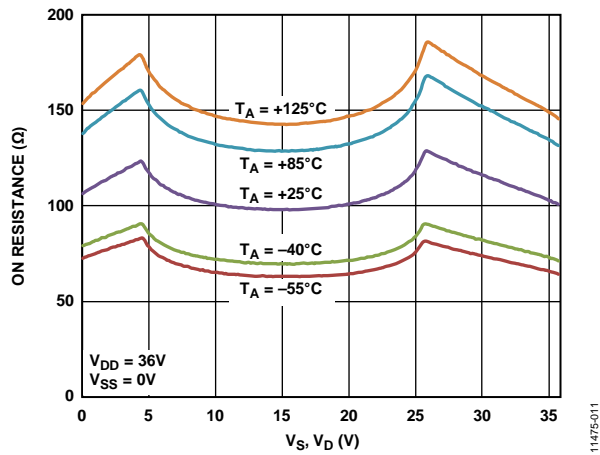


Figure 11.  $R_{ON}$  as a Function of  $V_S$ ,  $V_D$  for Different Temperatures, 36 V Single Supply

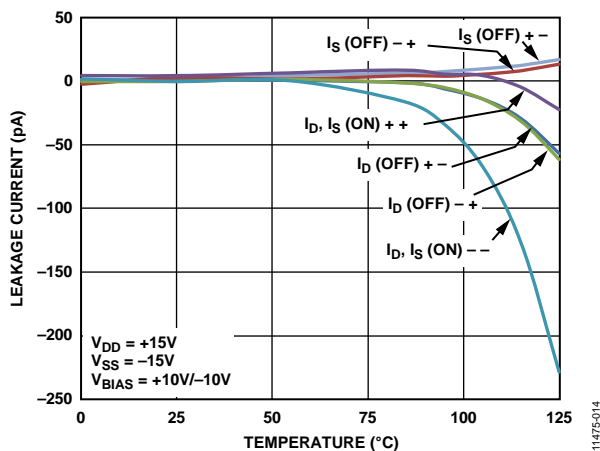


Figure 12. Leakage Currents vs. Temperature,  $\pm 15$  V Dual Supply

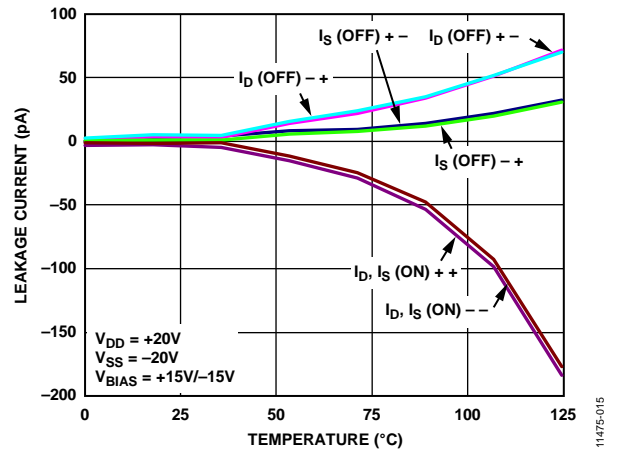


Figure 13. Leakage Currents vs. Temperature,  $\pm 20$  V Dual Supply

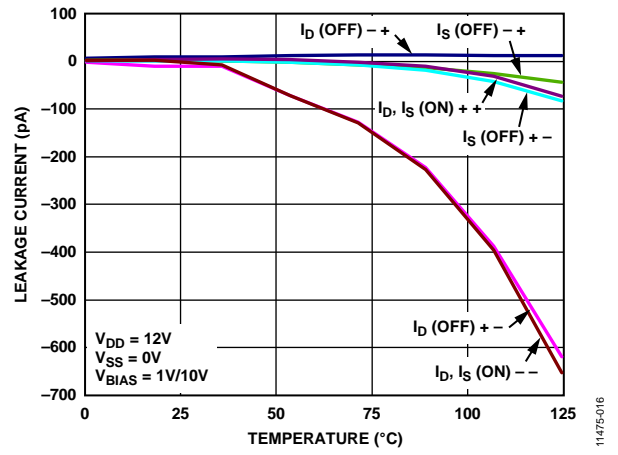


Figure 14. Leakage Currents vs. Temperature, 12 V Single Supply

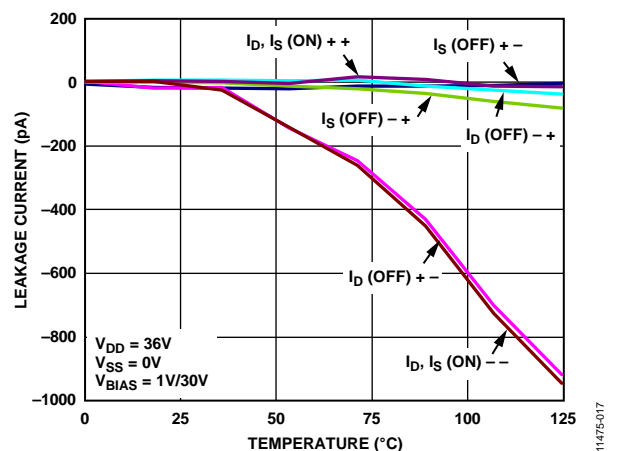


Figure 15. Leakage Currents vs. Temperature, 36 V Single Supply

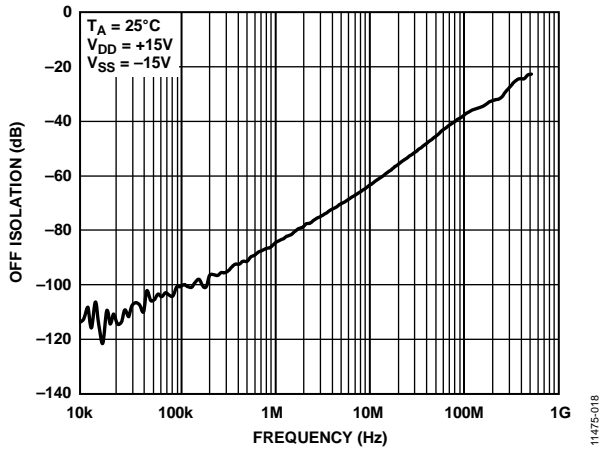


Figure 16. Off Isolation vs. Frequency, ±15 V Dual Supply

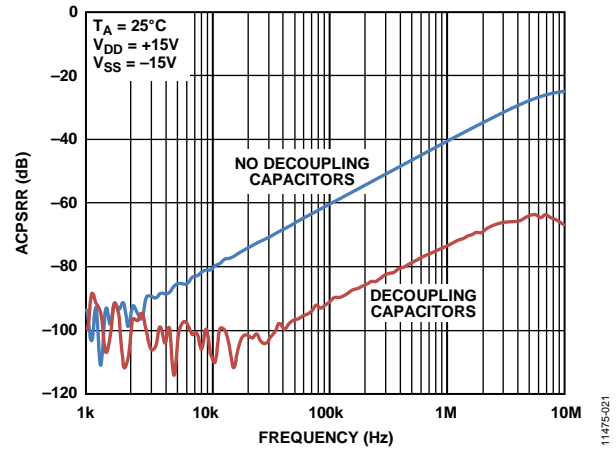


Figure 19. ACPSRR vs. Frequency, ±15 V Dual Supply

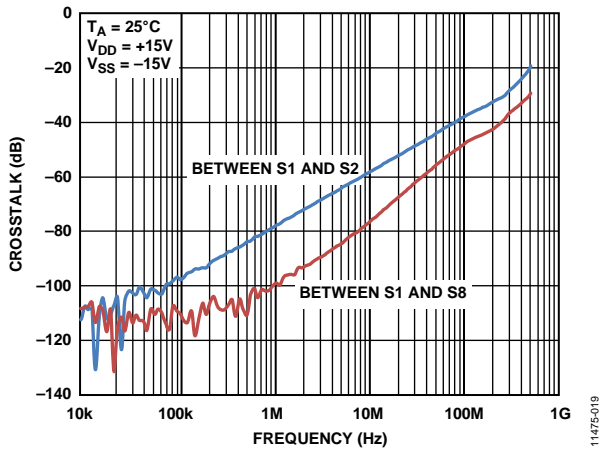


Figure 17. Crosstalk vs. Frequency, ±15 V Dual Supply

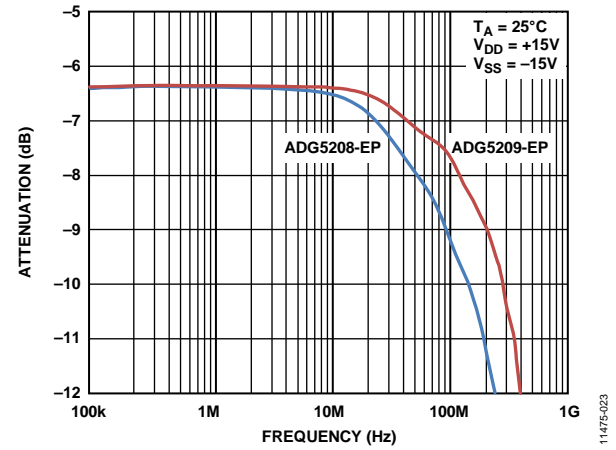


Figure 20. Bandwidth

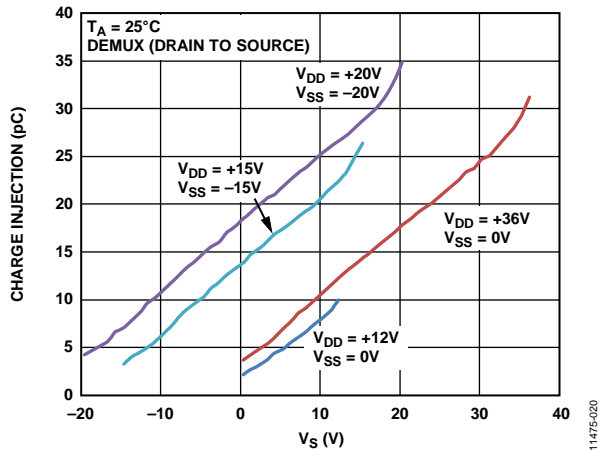


Figure 18. Charge Injection vs. Source Voltage, Drain to Source

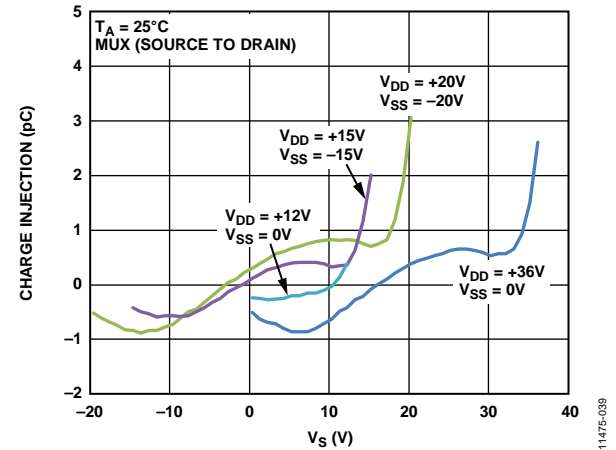


Figure 21. Charge Injection vs. Source Voltage, Source to Drain

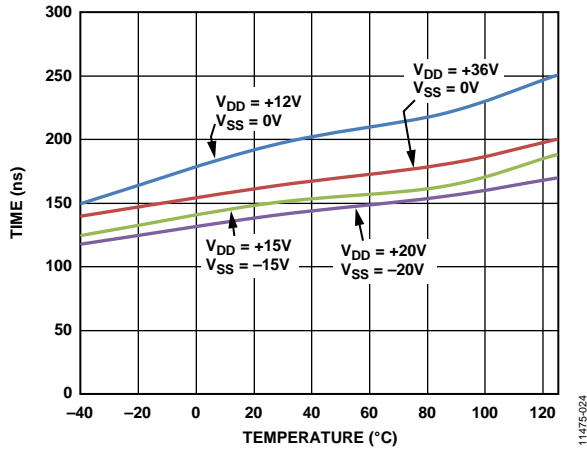


Figure 22.  $t_{\text{TRANSITION}}$  Times vs. Temperature

11475-024

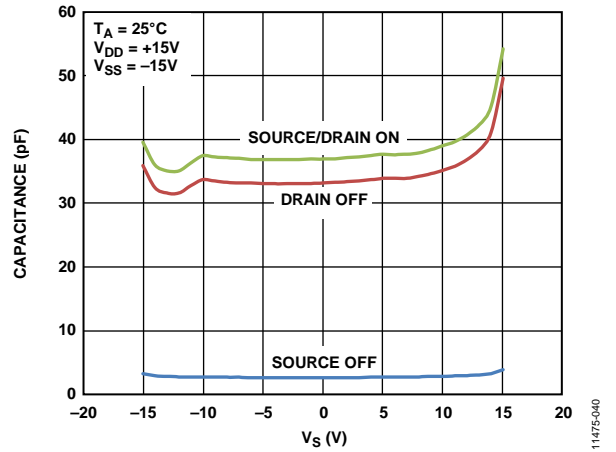


Figure 24. ADG5208-EP Capacitance vs. Source Voltage,  $\pm 15$  V Dual Supply

11475-040

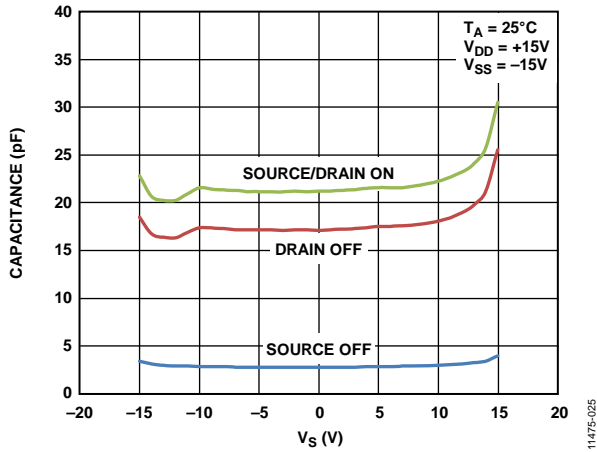


Figure 23. ADG5209-EP Capacitance vs. Source Voltage,  $\pm 15$  V Dual Supply

11475-025

TEST CIRCUITS

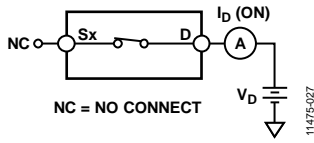


Figure 25. On Leakage

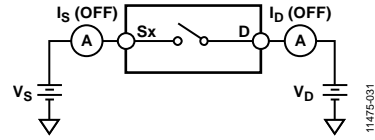


Figure 28. Off Leakage

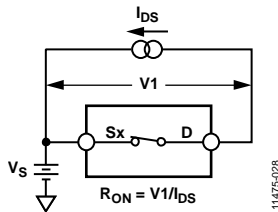


Figure 26. On Resistance

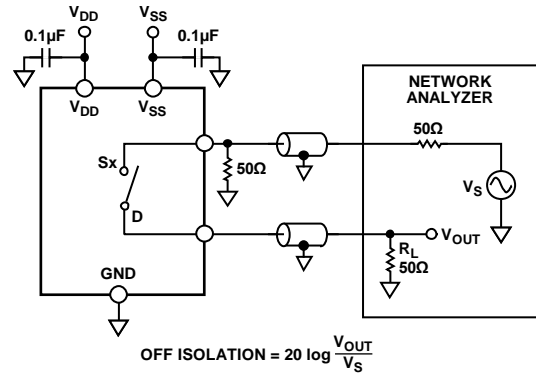


Figure 29. Off Isolation

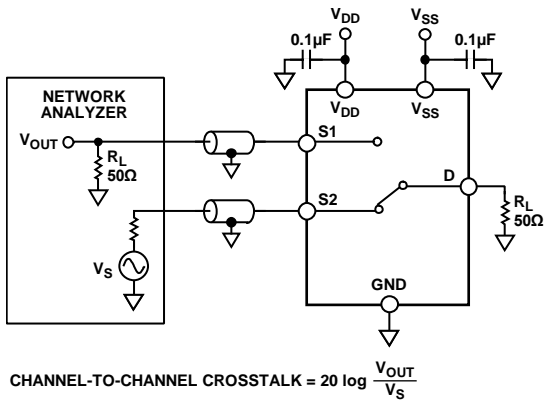


Figure 27. Channel-to-Channel Crosstalk

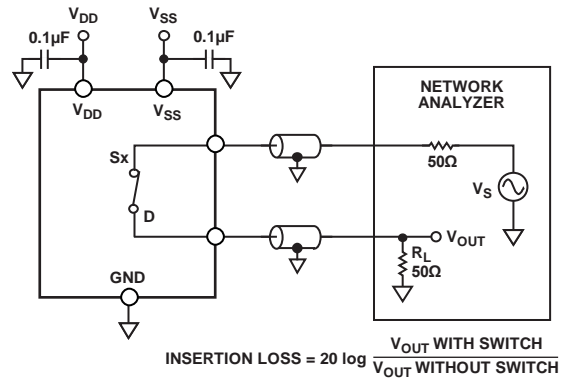


Figure 30. Bandwidth



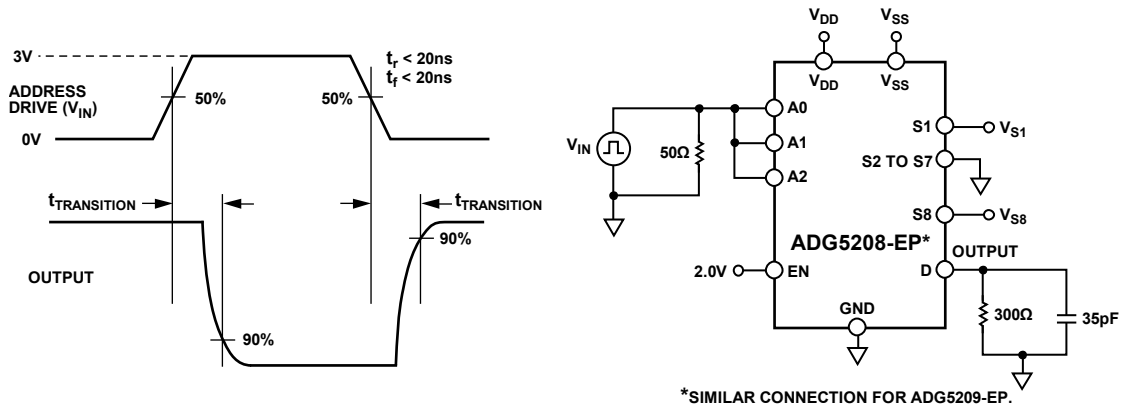


Figure 31. Address to Output Switching Times,  $t_{\text{TRANSITION}}$

11475-034

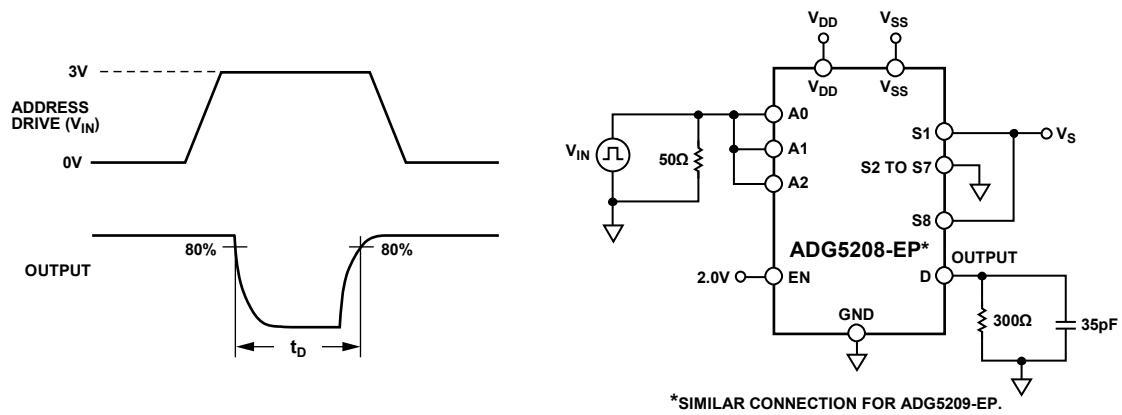


Figure 32. Break-Before-Make Time Delay,  $t_D$

11475-035

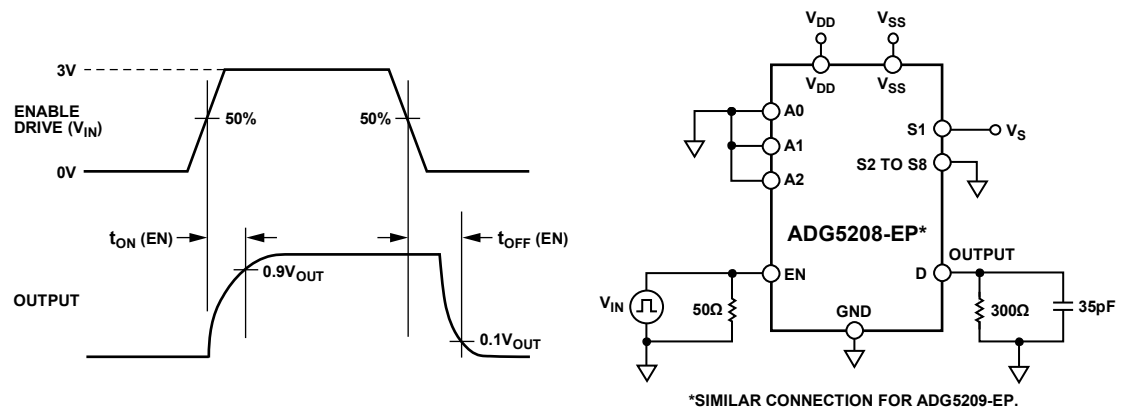


Figure 33. Enable Delay,  $t_{\text{ON}}(\text{EN})$ ,  $t_{\text{OFF}}(\text{EN})$

11475-036

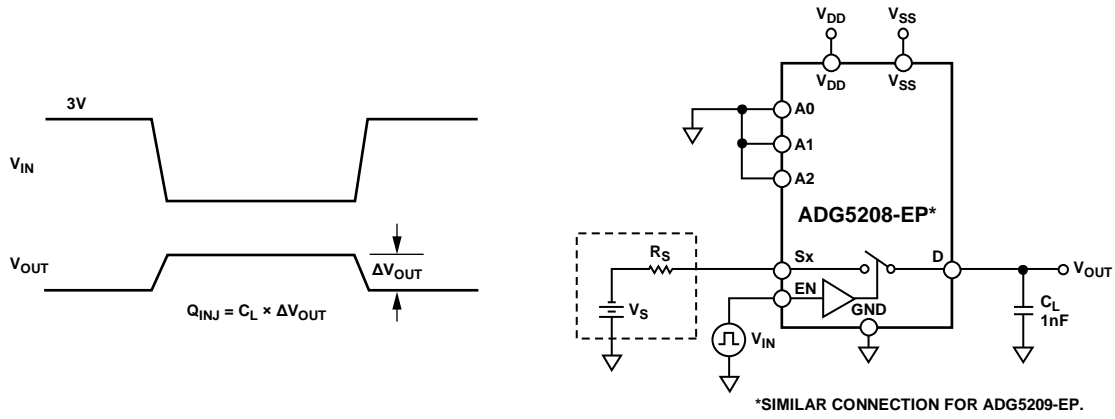
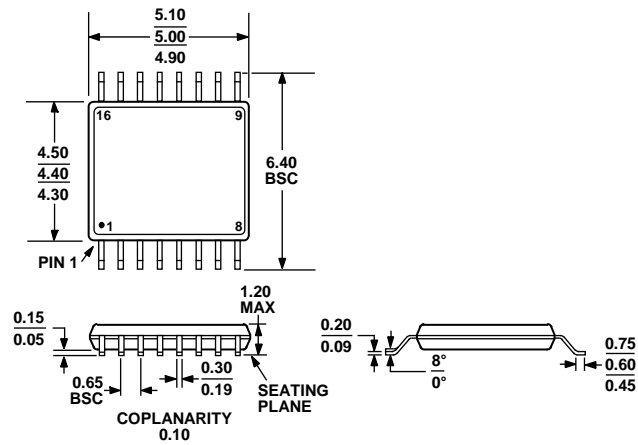


Figure 34. Charge Injection

11475-037

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)  
Dimensions shown in millimeters

## ORDERING GUIDE<sup>1</sup>

Model	Temperature Range	Package Description	Package Option
ADG5208SRU-EP-RL7	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5209SRU-EP-RL7	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5208SRUZ-EP-RL7	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5209SRUZ-EP-RL7	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**