

I²C BUS Control 5-Input 2-Output AV Switch Monolithic IC MM1495X

Outline

This IC is a 5-input, 2-output AV switch with I²C BUS control, developed for use in TV. This IC supports S2 and Cenelec standards.

Features

1. Serial control by I²C BUS.
2. 5 - inputs, 2 - outputs (2 of the 5 input lines can be used for either composite or Y)
3. Built-in sync separation circuit
4. Built-in Y/C mix circuit
5. Video and audio switches can be controlled independently.
6. 6dB amp built in to video and audio systems.
7. Output voltage gain can be varied by mounting an external resistor on the audio input pin.
8. Slave address can be changed: 90H or 92H
9. Built-in 3-value identification function

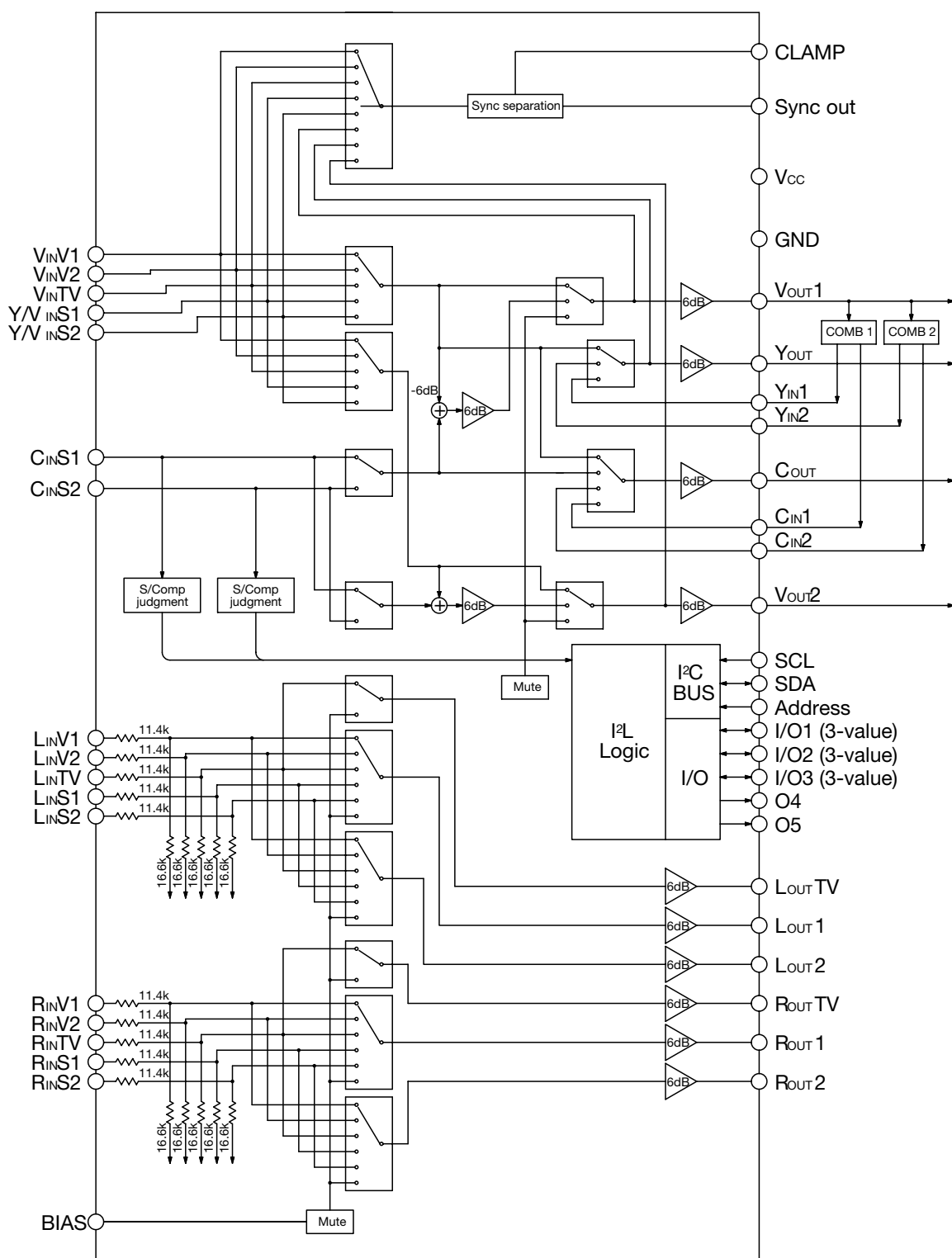
Package

SOP-44A (MM1495XF)
SDIP-42A (MM1495XD)

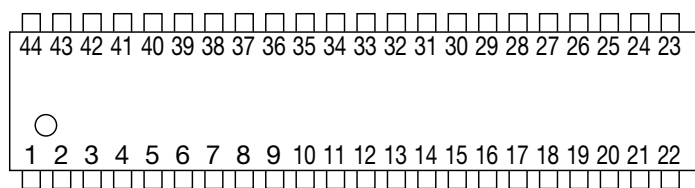
Applications

1. TV
2. Other video equipment

Block Diagram



Pin Assignment Typical model: MM1495XF



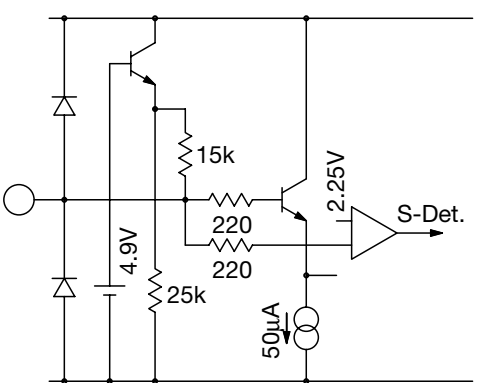
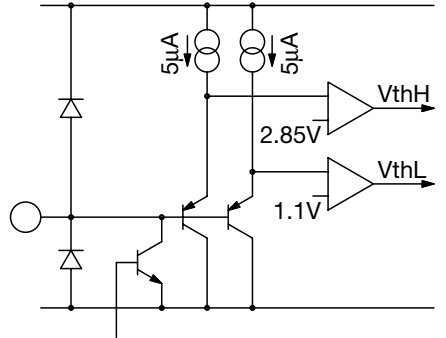
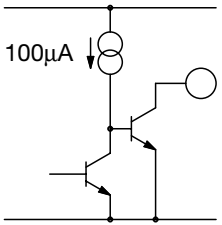
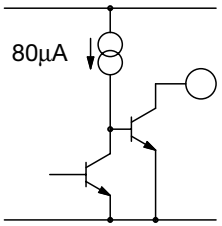
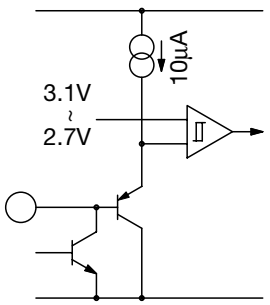
SOP-44A

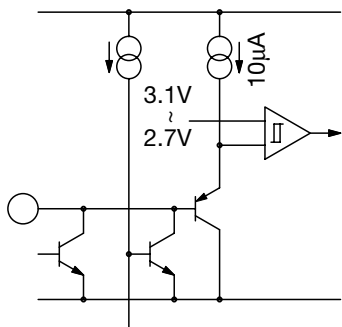
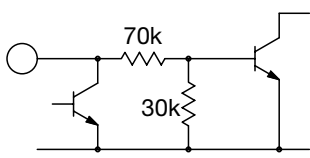
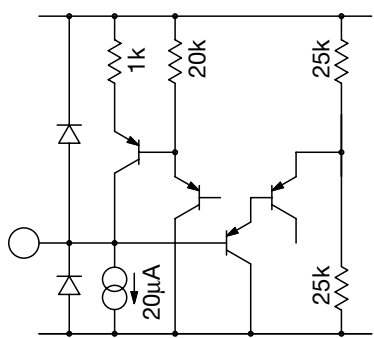
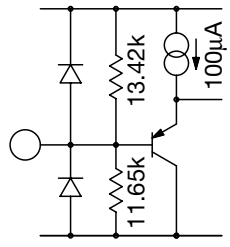
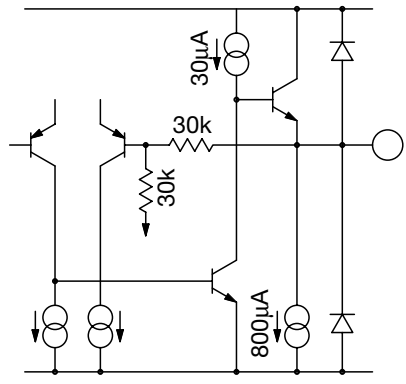
1	L _{IN} TV	12	L _{IN} S2	23	SCL	34	C _{IN} 2
2	R _{IN} TV	13	Y/V _{IN} S2	24	SDA	35	L _{OUT} 2
3	V _{IN} TV	14	R _{IN} S2	25	CLAMP	36	Y _{IN} 1
4	L _{IN} V1	15	C _{IN} S2	26	BIAS	37	V _{CC}
5	R _{IN} V1	16	I/O 2	27	Address	38	C _{IN} 1
6	V _{IN} V1	17	L _{IN} V2	28	R _{OUT} TV	39	R _{OUT} 1
7	L _{IN} S1	18	R _{IN} V2	29	L _{OUT} TV	40	V _{OUT} 1
8	Y/V _{IN} S1	19	V _{IN} V2	30	V _{OUT} 2	41	L _{OUT} 1
9	R _{IN} S1	20	I/O 3	31	GND	42	Y _{OUT}
10	C _{IN} S1	21	O4	32	Y _{IN} 2	43	O5
11	I/O 1	22	Sync _{COUT}	33	R _{OUT} 2	44	C _{OUT}

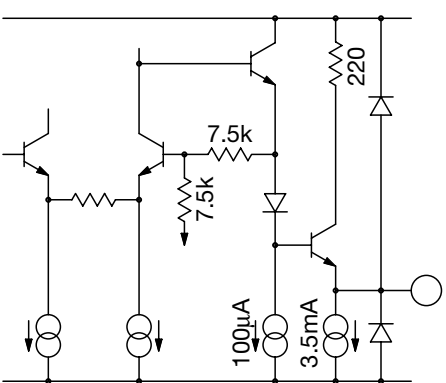
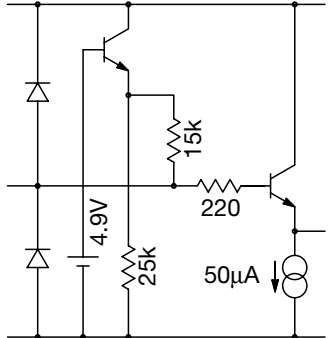
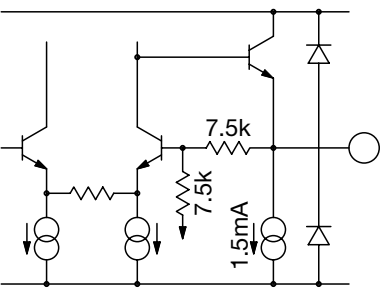
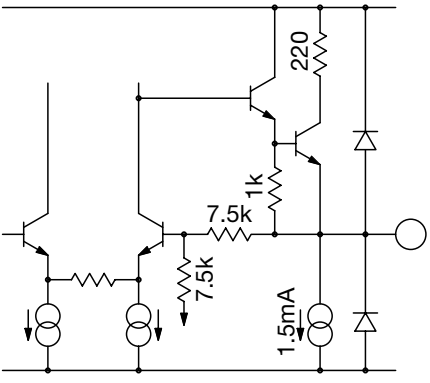
*XD has no O4 or Address pin.

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
1 2 4 5 7 9 12 14 17 18	L _{IN} TV R _{IN} TV L _{IN} V1 R _{IN} V1 L _{IN} S1 R _{IN} S1 L _{IN} S2 R _{IN} S2 L _{IN} V2 R _{IN} V2	Audio input	
3 6 8 13 19 32 36	V _{IN} TV V _{IN} V1 Y/V _{IN} S1 Y/V _{IN} S2 V _{IN} V2 Y _{IN} 2 Y _{IN} 1	Video input (Composite or Y) *Sync tip clamp	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
10 15	C _{INS1} C _{INS2}	Video input with S detector (Croma)	
11 16 20	I/O1 I/O2 I/O3	Input / Output port	
31	GND	GND	
37	V _{CC}	V _{CC}	
21 43	O4 O5	Output port	
22	Sync out	Sync separation output	
23	SCL	CLK input from I ² C	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
24	SDA	DATA input from I ² C	
27	Address	Address select	
25	CLAMP	Clamp capacitor	
26	BIAS	BIAS	
28 29 33 35 39 41	RoutTV LoutTV Rout2 Lout2 Rout1 Lout1	Audio output	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
30 40	V _{OUT2} V _{OUT1}	Video output (Composite)	
34 38	C _{IN2} C _{IN1}	Video input from comb-filter (Croma)	
42	Y _{OUT}	Video output (Y)	
44	C _{OUT}	Video output (Croma)	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+25	°C
Operating temperature	T _{OPR}	-20~+75	°C
Supply voltage	V _{CC} max.	12	V
Allowable loss	P _d	1100	mW

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T _{OPR}	-20~+75	°C
Operating voltage	V _{OP}	+8~+10	V

Electrical Characteristics Typical model: MM1495XF (Except where noted therwise, Ta=25°C, V_{CC}=9V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption	I _{CC}	No signal	41	58	75	mA
Terminal voltage						
Video input	V _{VIN}	3, 6, 8, 10, 13, 15, 19, 32, 34, 36, 38 pin	3.9	4.2	4.5	V
Composite video input	V _{VOUT}	30, 40 pin	1.9	2.1	2.3	V
S video input	V _{SOUT}	42, 44 pin	3.3	3.6	3.9	V
Audio input	V _{AIN}	1, 2, 4, 5, 7, 9, 12, 14, 17, 18 pin	3.2	3.5	3.8	V
Audio output	V _{AOOUT}	28, 29, 33, 35, 39, 41 pin	3.8	4.1	4.4	V
Input impedance						
Croma input	Z _{CIN}	10, 15, 34, 38 pin	10	15	20	kΩ
Audio L input	Z _{LIN}	1, 4, 7, 12, 17 pin	22	28	34	kΩ
Audio R input	Z _{RIN}	2, 5, 9, 14, 18 pin	22	28	34	kΩ
Threshold level						
S detect of C _{IN} S1	V _{thC1}		1.75	2.25	2.75	V
S detect of C _{IN} S2	V _{thC2}		1.75	2.25	2.75	V
Address detect	V _{thADR}		1.5	2.0	2.5	V
I/O1 port detect	L	V _{thI1L}	0.8	1.1	1.4	V
	H	V _{thI1H}	2.70	2.85	3.00	V
I/O2 port detect	L	V _{thI2L}	0.8	1.1	1.4	V
	H	V _{thI2H}	2.70	2.85	3.00	V
I/O3 port detect	L	V _{thI3L}	0.8	1.1	1.4	V
	H	V _{thI3H}	2.70	2.85	3.00	V
V _{OUT1}						
Voltage gain	G _{V1}	SIN wave: 1V 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{V1}	SIN wave: 1V 10MHz/100kHz	-1.0	0.0	1.0	dB
Differential gain	DG _{V1}	Staircase signal 1V	-3	0	3	%
Differential phase	DP _{V1}	Staircase signal 1V	-3	0	3	°
Input dynamic range	D _{V1}	SIN wave: 100kHz THD=1.0%	1.6	1.9		V
Output impedance	Z _{V1}			(50)		Ω
Crosstalk	CT _{V1}	use test circuit 2 3.58MHz, 1V		-60	-55	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V_{OUT2}						
Voltage gain	G _{V2}	SIN wave: 1V 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{V2}	SIN wave: 1V 10MHz/100kHz	-1.0	0.0	1.0	dB
Differential gain	DG _{V2}	Staircase signal 1V	-3	0	3	%
Differential phase	DP _{V2}	Staircase signal 1V	-3	0	3	°
Input dynamic range	D _{V2}	SIN wave: 100kHz THD=1.0%	1.6	1.9		V
Output impedance	Z _{V2}			(50)		Ω
Crosstalk	CT _{V2}	use test circuit 2 3.58MHz, 1V		-60	-55	dB
Y_{OUT}						
Voltage gain	G _{Y1}	SIN wave: 1V 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V 10MHz/100kHz	-1.0	0.0	1.0	dB
Differential gain	DG _{Y1}	Staircase signal 1V	-3	0	3	%
Differential phase	DP _{Y1}	Staircase signal 1V	-3	0	3	°
Input dynamic range	D _{Y1}	SIN wave: 100kHz THD=1.0%	1.6	1.9		V
Crosstalk	CT _{Y1}	use test circuit 2 3.58MHz, 1V		-60	-55	dB
C_{OUT}						
Voltage gain	G _{C1}	SIN wave: 1V 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{C1}	SIN wave: 1V 10MHz/100kHz	-1.0	0.0	1.0	dB
Differential gain (Note.1)	DG _{C1}	Staircase signal 1V	-3	0	3	%
Differential phase (Note.1)	DP _{C1}	Staircase signal 1V	-3	0	3	°
Input dynamic range	D _{C1}	SIN wave: 100kHz THD=1.0%	2.75	3.25		V
Crosstalk	CT _{C1}	use test circuit 2 3.58MHz, 1V		-60	-55	dB
Sync out						
Sync separation level	V _{SEPA}		30	60	90	mV
Sync out output voltage	L	V _{SOL} Sync out: sink 2mA			0.4	V
	H	V _{SOH}	4.8			V
L_{OUT1}						
Voltage gain	G _{L1}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f _{L1}	SIN wave: 1V (★1) 1MHz/1kHz	-1.0	0.0	1.0	dB
Total harmonic distortion	THD _{L1}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V _{OFFL1}	DC offset at the switching time	-30	0	30	mV
Output dynamic range	D _{L1}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT _{L1}	1kHz, 1V (★1)		-90	-80	dB
Ripple rejection	RR _{L1}	At 2.2kΩ terminal V _{CC} =9V+0.3V (100Hz: SIN wave)		-45	-40	dB
R_{OUT1}						
Voltage gain	G _{R1}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f _{R1}	SIN wave: 1V (★1) 1MHz/1kHz	-1.0	0.0	1.0	dB
Total harmonic distortion	THD _{R1}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V _{OFFR1}	DC offset at the switching time	-30	0	30	mV
Output dynamic range	D _{R1}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT _{R1}	1kHz, 1V (★1)		-90	-80	dB
Ripple rejection	RR _{R1}	At 2.2kΩ terminal V _{CC} =9V+0.3V (100Hz: SIN wave)		-45	-40	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
L_{OUT2}						
Voltage gain	G _{L2}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f _{L2}	SIN wave: 1V (★1) 1MHz/1kHz	-1.0	0.0	1.0	dB
Total harmonic distortion	THD _{L2}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V _{OFFL2}	DC offset at the switching time	-30	0	30	mV
Output dynamic range	D _{L2}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT _{L2}	1kHz, 1V (★1)		-90	-80	dB
Ripple rejection	RR _{L2}	At 2.2kΩ terminal V _{CC} =9V+0.3V (100Hz: SIN wave)		-45	-40	dB
R_{OUT2}						
Voltage gain	G _{R2}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f _{R2}	SIN wave: 1V (★1) 1MHz/1kHz	-1.0	0.0	1.0	dB
Total harmonic distortion	THD _{R2}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V _{OFFR2}	DC offset at the switching time	-30	0	30	mV
Output dynamic range	D _{R2}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT _{R2}	1kHz, 1V (★1)		-90	-80	dB
Ripple rejection	RR _{R2}	At 2.2kΩ terminal V _{CC} =9V+0.3V (100Hz: SIN wave)		-45	-40	dB
L_{OUTTV}						
Voltage gain	G _{LTV}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f _{LTV}	SIN wave: 1V (★1) 1MHz/1kHz	-1.0	0.0	1.0	dB
Total harmonic distortion	THD _{LTV}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V _{OFFLTV}	DC offset at the switching time	-30	0	30	mV
Output dynamic range	D _{LTV}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT _{LTV}	1kHz, 1V (★1)		-90	-80	dB
Ripple rejection	RR _{LTV}	At 2.2kΩ terminal V _{CC} =9V+0.3V (100Hz: SIN wave)		-45	-40	dB
R_{OUTTV}						
Voltage gain	G _{RTV}	SIN wave: 1V (★1) 1kHz	1.0	1.5	2.0	dB
Frequency characteristic	f _{RTV}	SIN wave: 1V (★1) 1MHz/1kHz	-1.0	0.0	1.0	dB
Total harmonic distortion	THD _{RTV}	SIN wave: 1V (★1) 1kHz		0.03	0.1	%
Output offset voltage	V _{OFFRTV}	DC offset at the switching time	-30	0	30	mV
Output dynamic range	D _{RTV}	SIN wave: 1kHz THD=0.5%	2.6	2.8		V (★1)
Crosstalk	CT _{RTV}	1kHz, 1V (★1)		-90	-80	dB
Ripple rejection	RR _{RTV}	At 2.2kΩ terminal V _{CC} =9V+0.3V (100Hz: SIN wave)		-45	-40	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I ² C condition (Note.2)						
Input voltage L	V _{IL}		0.0		1.5	V
Input voltage H	V _{IH}		3.0		5.0	V
Low level output voltage	V _{OL}	SDA sink 3mA	0.0		0.4	V
High level input current	I _{IH}	SDA, SCL=4.5V	-10		10	μA
Low level input current	I _{IL}	SDA, SCL=0.4V	-10		10	μA
Clock frequency	f _{SCL}				100	kHz
Data transfer wait time	t _{BUF}		4.7			μs
SCL start hold time	t _{HD} ; STA		4.0			μs
SCL low level hold time	t _{LOW}		4.7			μs
SCL high level hold time	t _{HIGH}		4.0			μs
SCL start setup time	t _{SU} ; STA		4.7			μs
SDA data hold time	t _{HD} ; DAT		200			ns
SDA data setup time	t _{SU} ; DAT		250			ns
SCL rise time	t _R				1000	ns
SCL fall time	t _F				300	ns
SCL stop setup time	t _{SU} ; STO		4.0			μs

() The inside of parentheses is design guarantee value.

(★1) Effective value

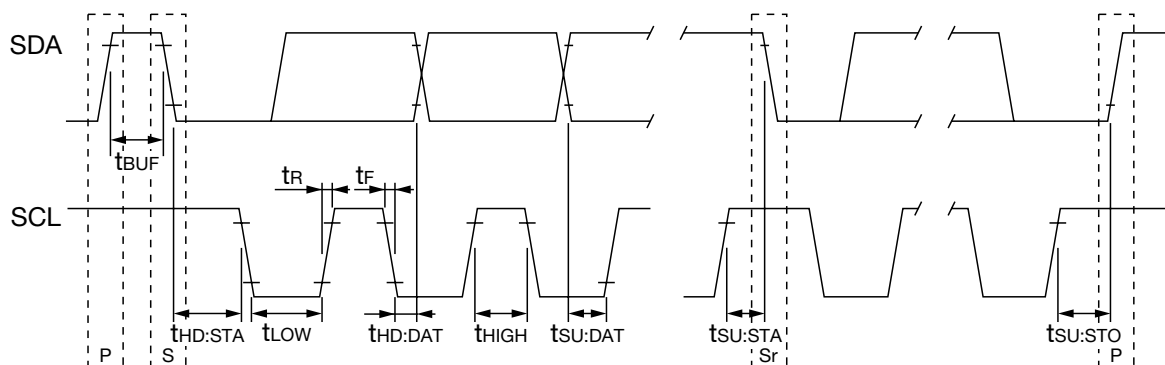
(Note.1) Differential gain and Differential phase of C_{OUT}.

The following combination is presumed as a case that a Y signal is left in the croma output terminal (C_{OUT}).

- { (1) At the time of the V-throughmode choice
- { (2) When a Y signal is left with comb-filter for C_{IN1}, the C_{IN2} input.

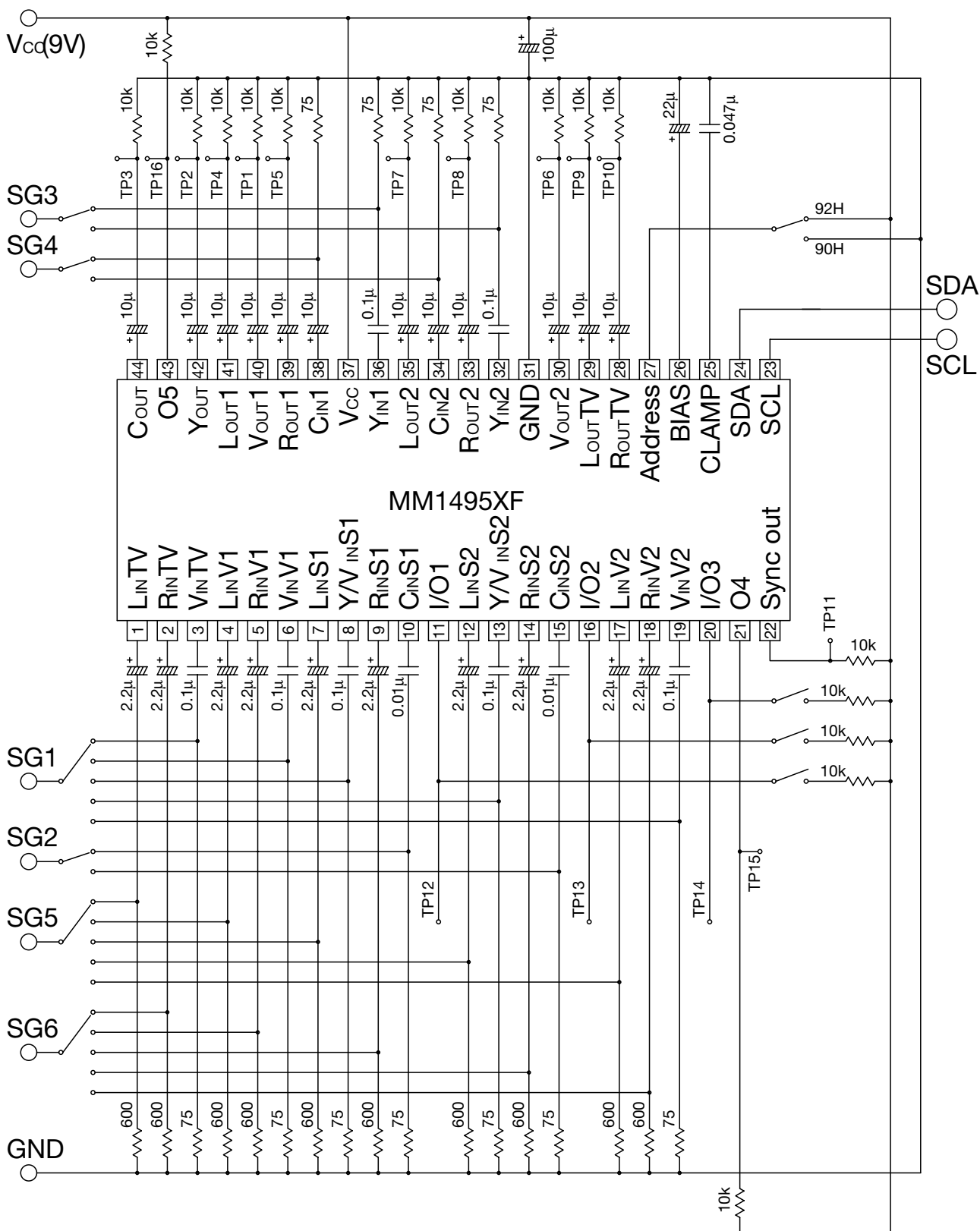
Do the measurement of differential-gain and differential-phase with the C_{OUT} terminal by the above mode.

(Note.2) I²C condition



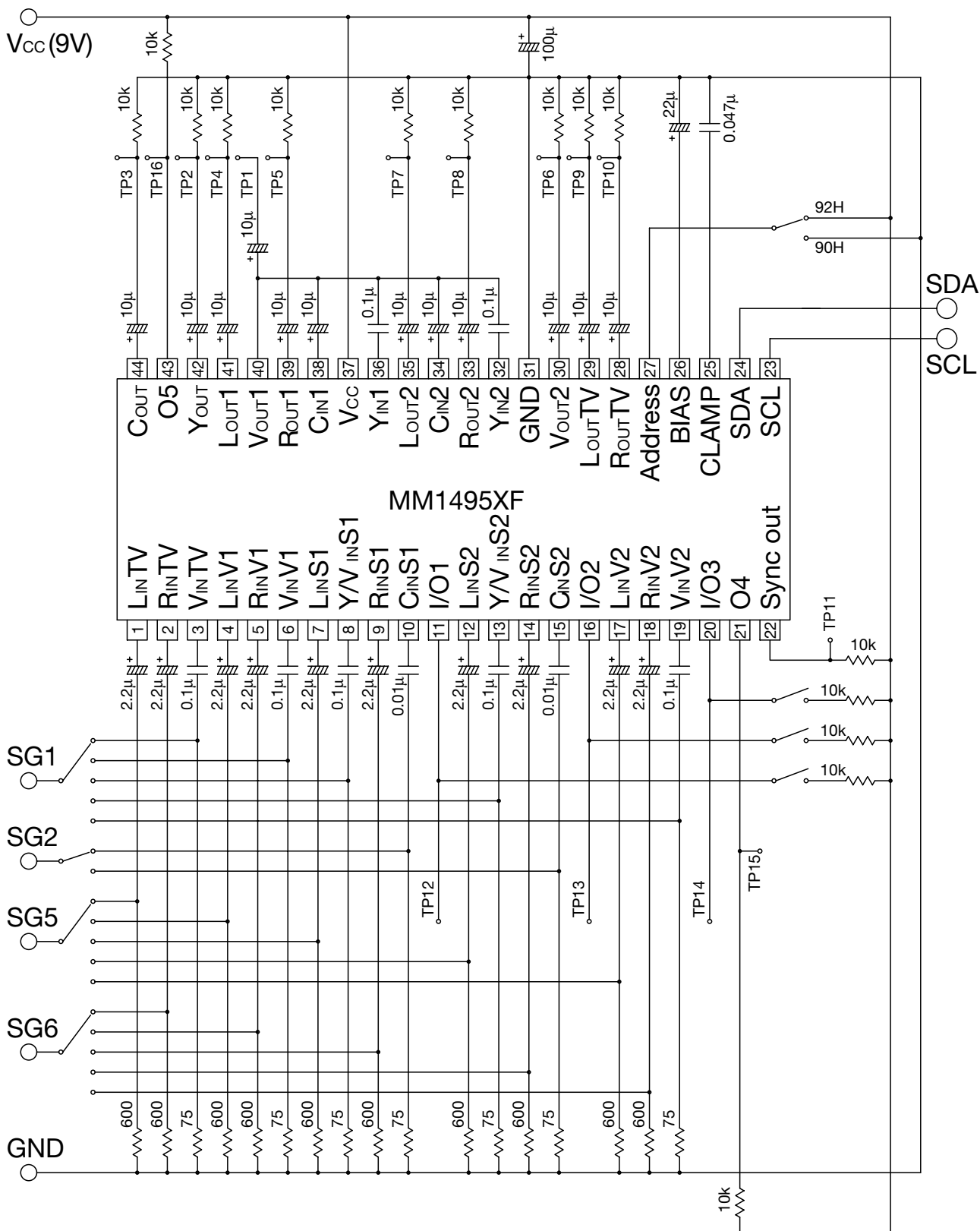
(Note.3) Video inputs

V_{IN}V1, V_{IN}V2, V_{IN}TV, Y/V_{IN}S1, Y/V_{IN}S2, Y_{IN}1 and Y_{IN}2 inputs are sync tip clamped, while C_{IN}S1, C_{IN}S2, C_{IN}1 and C_{IN}2 inputs are non-clamped.



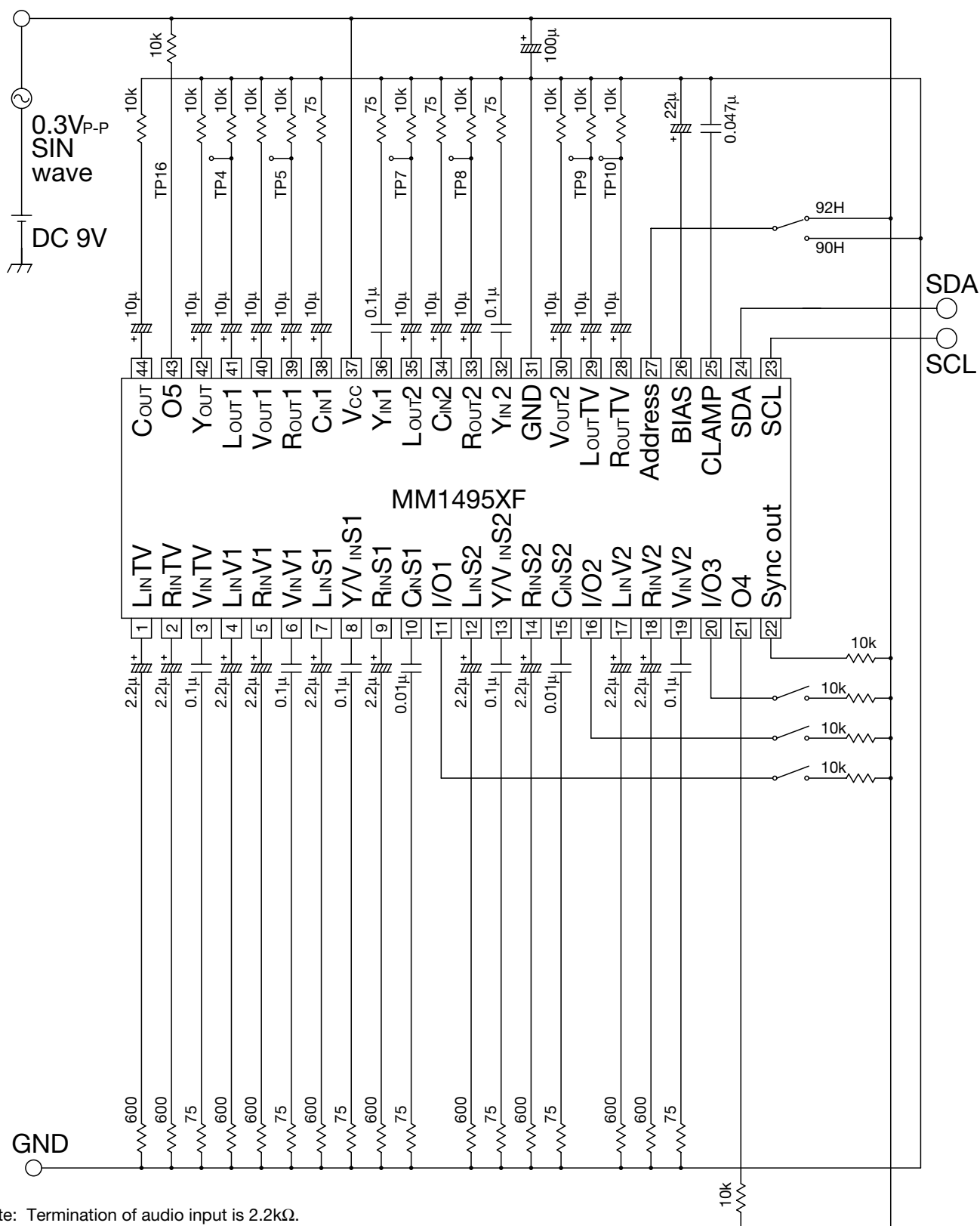
Measuring Circuit 2

For measuring crosstalk



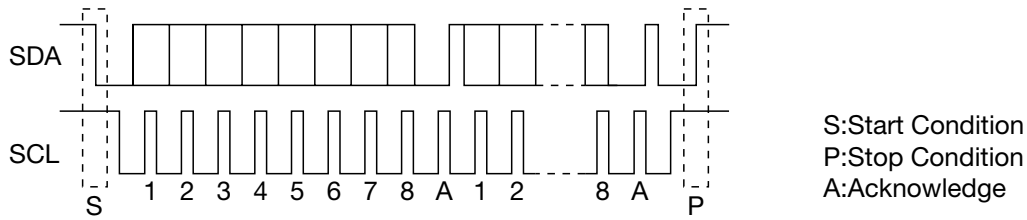
Measuring Circuit 3

For measuring ripple rejection



note: Termination of audio input is 2.2kΩ.

I²C BUS



I²C BUS is inter bus system controlled by 2 lines (SDA, SCL).

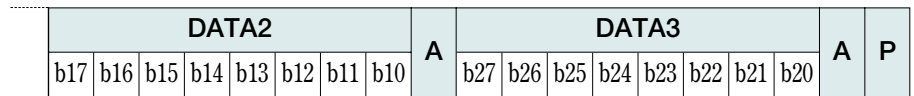
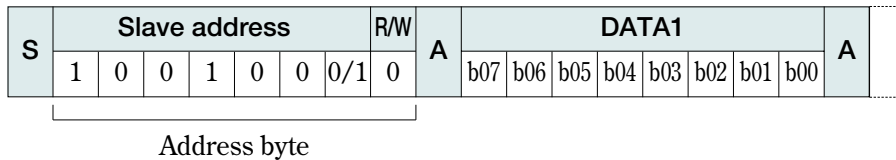
Data are transmitted and received in the units of byte and Acknowledge.

It is transmitted by MSB first from the Start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.

The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.

Set the R/W bit to 0 when data are used control registers.

As MM1495 slave address, either 90H or 92H can be selected according to the ADR terminal conditions. When ADR terminal is L, 90H is selected.

The following figure indicates the control contents of control registers and switches.

Each bit of control registers is reset to 0, when power-on.

No.	DATA condition							
DATA1	b07	b06	b05	b04	b03	b02	b01	b00
		Y/C select		Mute		Main V select		
		Y, C _{IN} 1/2	Y, C _{OUT}	L _{OUT} 1 R _{OUT} 1	V _{OUT} 1			
DATA2	b17	b16	b15	b14	b13	b12	b11	b10
			Mute			Sub V select		
			L _{OUT} TV R _{OUT} TV	L _{OUT} 2 R _{OUT} 2	V _{OUT} 2			
DATA3	b27	b26	b25	b24	b23	b22	b21	b20
	Output port select					Sync sepa select		
	O5	O4	O3	O2	O1			

MM1495 consists of one address byte and three control data bytes (4bytes in total).

All data over the limited length (5th and subsequent bytes) are fully neglected.

For details of the control contents of switches, refer to the separate table.

Switch Control Table

Main V select

Mode		Output	S detect		Bus data		
					Main select		
Input	S/V	V _{OUT1}	CS2	CS1	b02	b01	b00
S2	V	Y/V _{INS2}	Low	*	1	1	0
	S	Y/V _{INS2} +C _{INS2}	Open				1
	FV	Y/V _{INS2}					1
S1	V	Y/V _{INS1}	*	Low	1	0	0
	S	Y/V _{INS1} + C _{INS1}		Open			
	FV	Y/V _{INS1}					1
V2	V	V _{INV2}	*	*	0	1	1
V1	V	V _{INV1}	*	*	0	1	0
TV	V	V _{INTV}	*	*	0	0	*

*: Don't care

Main L / R select

Mode	Output		Bus data		
			Main select		
Input	L _{OUT1}	R _{OUT1}	b02	b01	b00
S2	L _{INS2}	R _{INS2}	1	1	*
S1	L _{INS1}	R _{INS1}	1	0	*
V2	L _{INV2}	R _{INV2}	0	1	1
V1	L _{INV1}	R _{INV1}	0	1	0
TV	L _{INTV}	R _{INTV}	0	0	*

Main Y/C select

Mode		Output		Main V select mode		Bus data	
						Y/C select	
Input	Through	Y _{OUT}	C _{OUT}			b05	b06
S2	Y/C _{IN}	Y _{IN1}	C _{IN1}	S2	V or FV	0	0
		Y _{IN2}	C _{IN2}			1	
	V through	Y/V _{IN} S2	Y/V _{IN} S2		1	*	
	S through	Y/V _{IN} S2	C _{IN} S2		S	*	*
S1	Y/C _{IN}	Y _{IN1}	C _{IN1}	S1	V or FV	0	0
		Y _{IN2}	C _{IN2}			1	1
	V through	Y/V _{IN} S1	Y/V _{IN} S1		1	*	
	S through	Y/V _{IN} S1	C _{IN} S1		S	*	*
V2	Y/C _{IN}	Y _{IN1}	C _{IN1}	V2	V	0	0
		Y _{IN2}	C _{IN2}			1	1
	V through	V _{IN} V2	V _{IN} V2			1	*
V1	Y/C _{IN}	Y _{IN1}	C _{IN1}	V1	V	0	0
		Y _{IN2}	C _{IN2}			1	1
	V through	V _{IN} V1	V _{IN} V1			1	*
TV	Y/C _{IN}	Y _{IN1}	C _{IN1}	TV	V	0	0
		Y _{IN2}	C _{IN2}			1	1
	V through	V _{IN} TV	V _{IN} TV			1	*

Sub V select

Mode		Output	S detect		Bus data		
					Main select		
Input	S/V	V _{OUT2}	CS2	CS1	b12	b11	b10
S2	V	Y/V _{INS2}	Low	*	1	1	0
	S	Y/V _{INS2} +C _{INS2}	Open				
	FV	Y/V _{INS2}					1
S1	V	Y/V _{INS1}	*	Low	1	0	0
	S	Y/V _{INS1} +C _{INS1}		Open			
	FV	Y/V _{INS1}					1
V2	V	V _{INV2}	*	*	0	1	1
V1	V	V _{INV1}	*	*	0	1	0
TV	V	V _{INTV}	*	*	0	0	*

Sub L / R select

Mode	Output		Bus data		
			Sub select		
Input	L _{OUT2}	R _{OUT2}	b12	b11	b10
S2	L _{INS2}	R _{INS2}	1	1	*
S1	L _{INS1}	R _{INS1}	1	0	*
V2	L _{INV2}	R _{INV2}	0	1	1
V1	L _{INV1}	R _{INV1}	0	1	0
TV	L _{INTV}	R _{INTV}	0	0	*

Video mute

Mode		Bus data	
Output	Mute	Video mute	
		b03	b13
V _{OUT1}	ON	0	*
	OFF	1	
V _{OUT2}	ON	*	0
	OFF		1

Audio mute

Mode		Bus data		
Output	Mute	Audio mute		
		b04	b14	b15
L _{OUT1}	ON	0	*	*
R _{OUT1}	OFF	1		
L _{OUT2}	ON	*	0	*
R _{OUT2}	OFF		1	
L _{OUTTV}	ON	*	*	0
R _{OUTTV}	OFF			1

■ Sync sepa select

Mode		Output	Bus data		
			Sync sepa select		
			b22	b21	b20
Video input	S2	Y/V _{INS2}	1	1	0
	S1	Y/V _{INS1}	1	0	0
	V2	V _{INV2}	0	1	1
	V1	V _{INV1}	0	1	0
	TV	V _{INTV}	0	0	0
Video output	V _{OUT2}	V _{OUT2}	1	1	1
	V _{OUT1}	V _{OUT1}	1	0	1
	Y _{OUT}	Y _{OUT}	0	0	1

■ Output port switching

Mode		Bus data				
		Output port switching				
Port	Condition	b27	b26	b25	b24	b23
I/O1	Open	*	*	*	*	0
	Low					1
I/O2	Open	*	*	*	0	*
	Low				1	
I/O3	Open	*	*	0	*	*
	Low			1		
O4	Open	*	0	*	*	*
	Low		1			
O5	Open	0	*	*	*	*
	Low	1				

[Status registers]

Status registers are data to inform the master of the device status.

The data format is set as shown in the following figure.

S	Slave address							R/W	A	Status register								NA	P
	1	0	0	1	0	0	0/1			1	b37	b36	b35	b34	b33	b32	b31		
Address byte									device status										

Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.

Set the R/W bit to 1 when data are used status registers.

As MM1495 slave address, either 91H or 93H can be selected according to the ADR terminal conditions.

When ADR terminal is L, 91H is selected.

Set the confirmation acknowledgement after the end of status register to non-acknowledgement.

The following figure shows the correspondence of the output data of status registers.

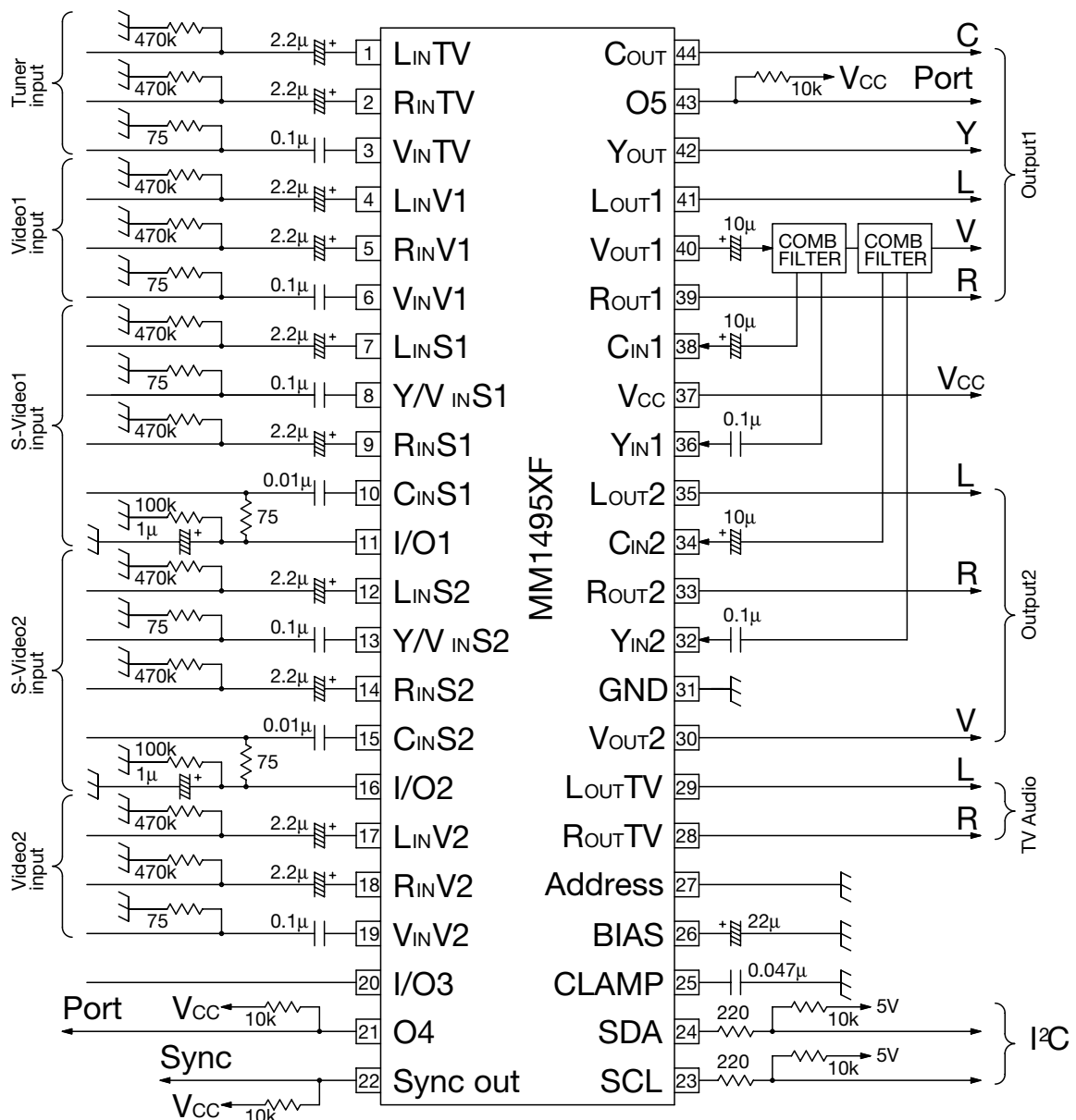
b37	b36	b35	b34	b33	b32	b31	b30
Input port detect						S detect	
I/O3 Low	I/O3 High	I/O2 Low	I/O2 High	I/O1 Low	I/O1 High	C _{INS2}	C _{INS1}

- Input port detect: I/O1~3 are identified by 3 values, and output according to the combinations shown in the following table.
- S detect: Judge the DC level of C_{IN}S1, the C_{IN}S2 terminal, and do the detection of the S input.

DC voltage of I/O1~3	I/O Low	I/O High
$DC \leq 0.8V$	1	1
$1.4V \leq DC \leq 2.7V$	1	0
$3.0V \leq DC$	0	0

C _{IN} Sn condition	b31 or b30
Internal voltage	1
$DC < 1.75V$	0

Application Circuit 1



Note.

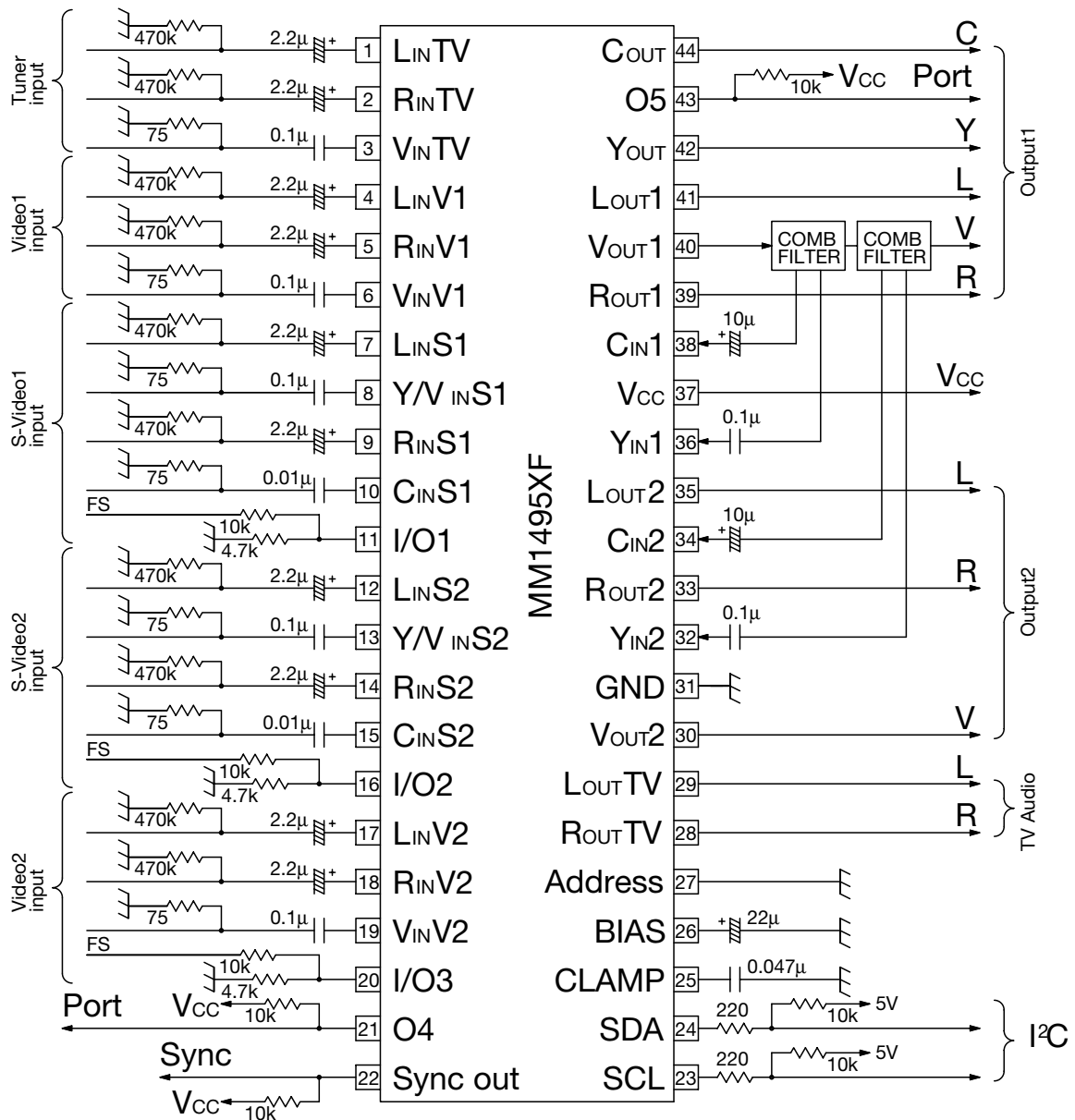
(1) V_{OUT} is set to 2.1V, while C_{IN} is set to 4.2V.

Be careful since the capacitor polarity may differ according to the comb filter bias.

(2) The case that a Y element is left by the Comb-filter character is presumed the condenser of C_{IN}1, C_{IN}2, and there is it as 10μF.

You can use 0.01μF when a Y element isn't left in the chroma output of Comb-filter.

Application Circuit 2



Note.

(1) V_{OUT} is set to 2.1V, while C_{IN} is set to 4.2V.

Be careful since the capacitor polarity may differ according to the comb filter bias.

(2) The case that a Y element is left by the Comb-filter character is presumed the condenser of C_{IN1}, C_{IN2}, and there is it as 10μF.

You can use 0.01μF when a Y element isn't left in the chroma output of Comb-filter.