

2Mx16 Flash MODULE, SMD 5962-97610

FEATURES

- Access Times of 90, 120, 150ns
- Packaging:
 - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207).
 - Fits standard 56 SSOP footprint.
 - 44 pin Ceramic SOJ (Package 102)**
 - 44 lead Ceramic Flatpack (Package 208)**
- Sector Architecture
 - 32 equal size sectors of 64KBytes each
 - Any combination of sectors can be erased.
 - Also supports full chip erase.
- Minimum 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx16; User Configurable as 2 x 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5 Volt Read and Write. 5V $\pm$ 10% Supply.

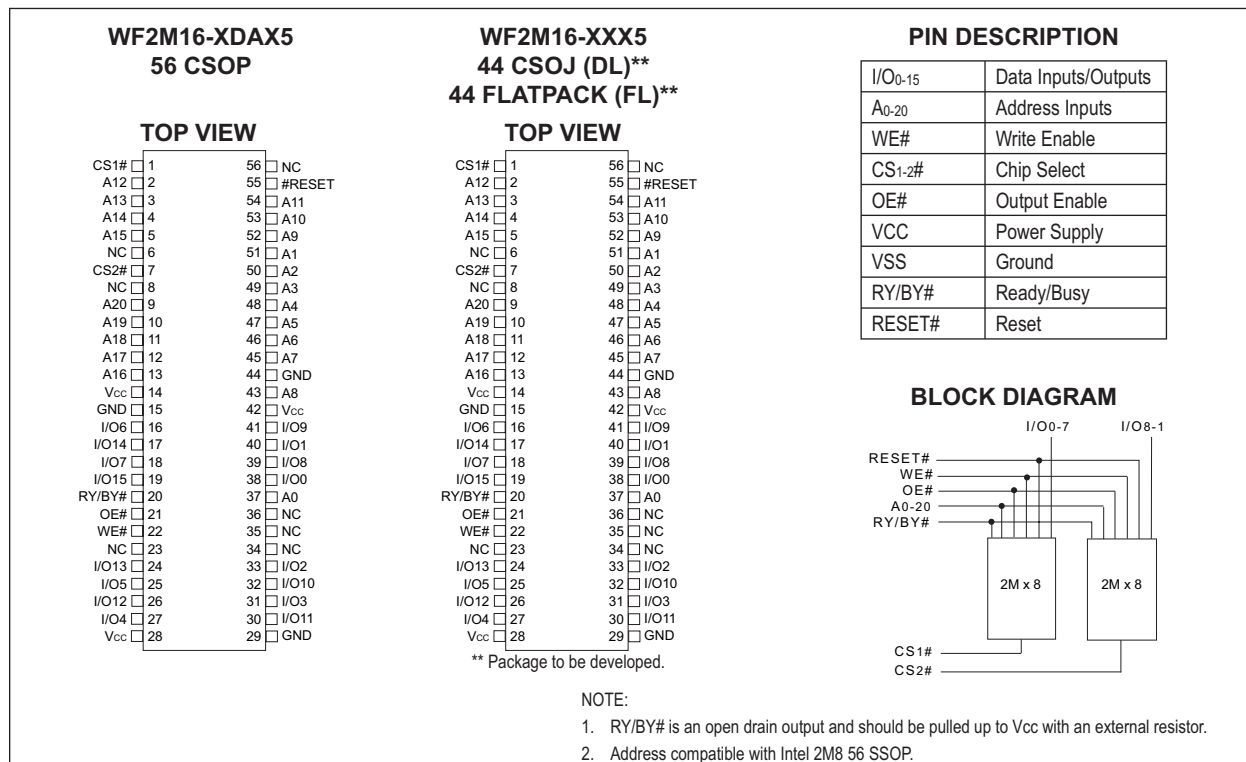
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation.
- RESET# pin resets internal state machine to the read mode.
- Ready/Busy (RY#/BY#) output for detection of program or erase cycle completion.
- Multiple Ground Pins for Low Noise Operation

* This product is under development, is not qualified or characterized and is subject to change without notice.

** Package to be developed.

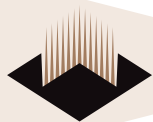
Note: For programming information refer to Flash Programming 16M5 Application Notes.

FIGURE 1 – PIN CONFIGURATIONS



NOTE:

1. RY/BY# is an open drain output and should be pulled up to Vcc with an external resistor.
2. Address compatible with Intel 2M8 56 SSOP.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-2.0 to +7.0	V
Power Dissipation	P _T	8	W
Storage Temperature	T _{STG}	-65 to +125	°C
Short Circuit Output Current	I _{OS}	100	mA
Data Retention (Mil Temp)		20	years
Endurance — write/erase cycles	(Mil Temp)	100,000 min.	cycles

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C _{OE}	V _{IN} = 0V, f = 1.0 MHz	25	pF
WE# capacitance	C _{WE}	V _{IN} = 0V, f = 1.0 MHz	25	pF
CS# capacitance	C _{CS}	V _{IN} = 0V, f = 1.0 MHz	15	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0V, f = 1.0 MHz	15	pF
Address input capacitance	C _{AD}	V _{IN} = 0V, f = 1.0 MHz	25	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	—	+0.8	V
Operating Temperature (Mil.)	T _A	-55	—	+125°C	°C
Operating Temperature (Ind.)	T _A	-40	—	+85	°C

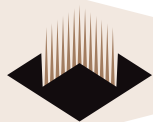
DC CHARACTERISTICS - CMOS COMPATIBLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz		80	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	CS# = V _{IL} , OE# = V _{IH}		120	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = 5.5, CS# = V _{IH} , f = 5MHz, RESET# = V _{CC} ± 0.3V		4.0	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85xV _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



AC Characteristics – Write/Erase/Program Operations - WE# Controlled

$V_{CC} = 5.0V$, $V_{SS} = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	45		50		50		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	μs
Sector Erase (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t_{GHWL}		0		0		0		μs
V _{CC} Setup Time	t_{VCS}		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEHL}	10		10		10		ns
RESET# Pulse Width		t_{RP}	500		500		500		ns

NOTES:

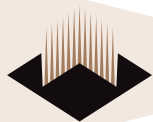
1. Typical value for t_{WHWH1} is 7 μs .
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

$V_{CC} = 5.0V$, $V_{SS} = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	T_{AVAV}	T_{RC}	90		120		150		ns
Address Access Time	T_{AVQV}	T_{ACC}		90		120		150	ns
Chip Select Access Time	T_{ELQV}	T_{CE}		90		120		150	ns
Output Enable to Output Valid	T_{GLQV}	T_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	T_{EHQZ}	T_{DF}		20		30		35	ns
Output Enable High to Output High Z (1)	T_{GHQZ}	T_{DF}		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	T_{AXQX}	T_{OH}	0		0		0		ns
RESET# Low to Read Mode (1)		T_{READY}		20		20		20	μs

1. Guaranteed by design, not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,CS# CONTROLLED

$V_{CC} = 5.0V$, $V_{SS} = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-90		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV} , t _{WC}	90		120		150		ns
Write Enable Setup Time	t _{WLEL} , t _{WS}	0		0		0		ns
Chip Select Pulse Width	t _{LELH} , t _{CP}	45		50		50		ns
Address Setup Time	t _{AVEL} , t _{AS}	0		0		0		ns
Data Setup Time	t _{DVEH} , t _{DS}	45		50		50		ns
Data Hold Time	t _{EHDX} , t _{DH}	0		0		0		ns
Address Hold Time	t _{ELAX} , t _{AH}	45		50		50		ns
Chip Select Pulse Width High	t _{EHEL} , t _{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}		300		300		300	μs
Sector Erase Time (2)	t _{WHWH2}		15		15		15	sec
Read Recovery Time	t _{GHEL}	0		0		0		μs
Chip Programming Time			44		44		44	sec
Chip Erase Time (3)			256		256		256	sec
Output Enable Hold Time (4)	t _{OEH}	10		10		10		ns

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 2 – AC TEST CIRCUIT

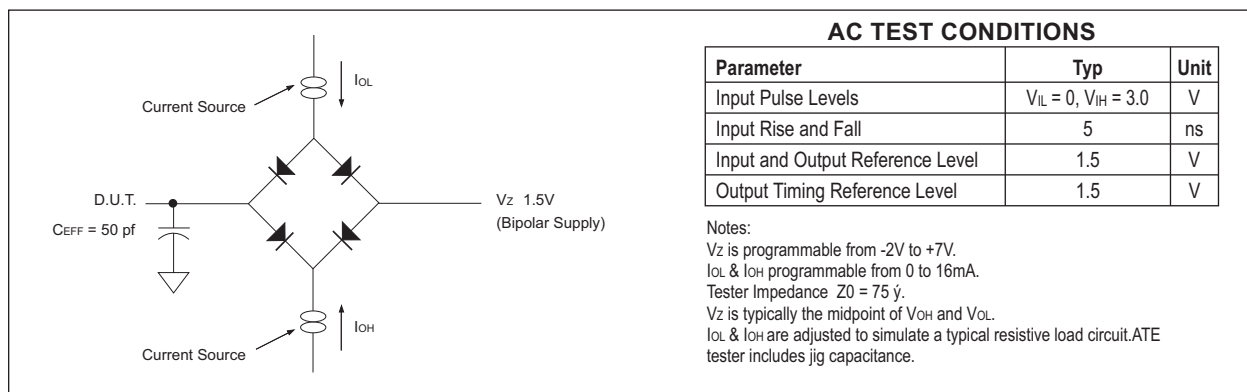


FIGURE 3 – RESET TIMING DIAGRAM

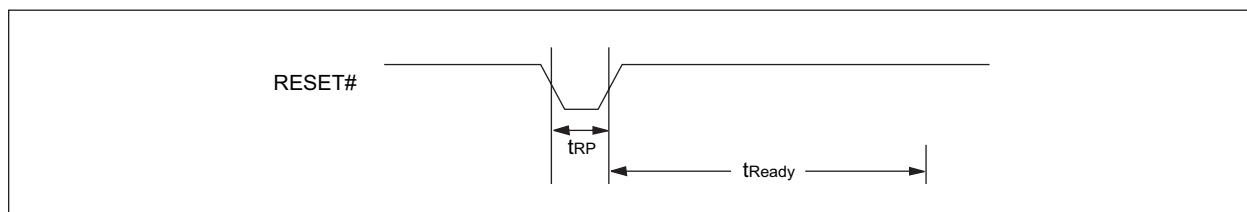
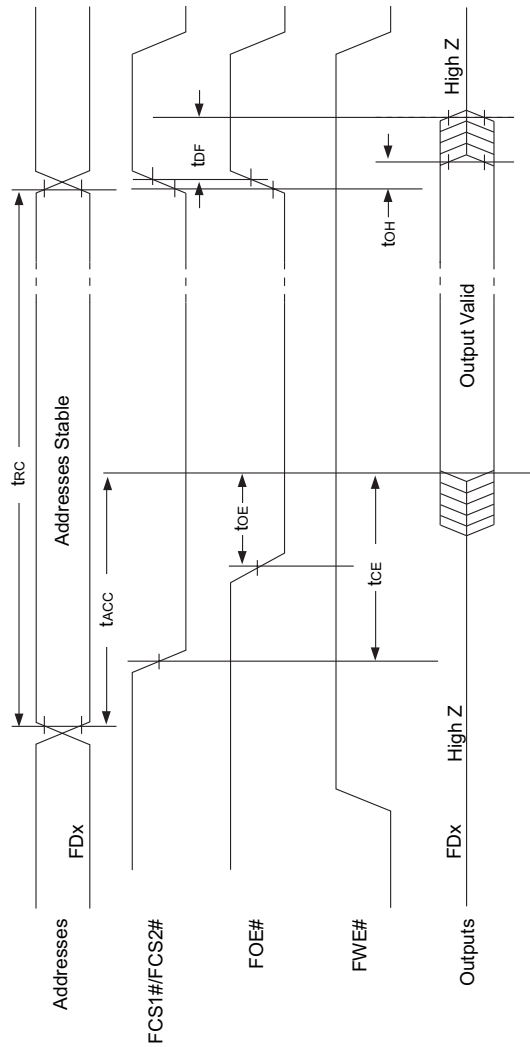




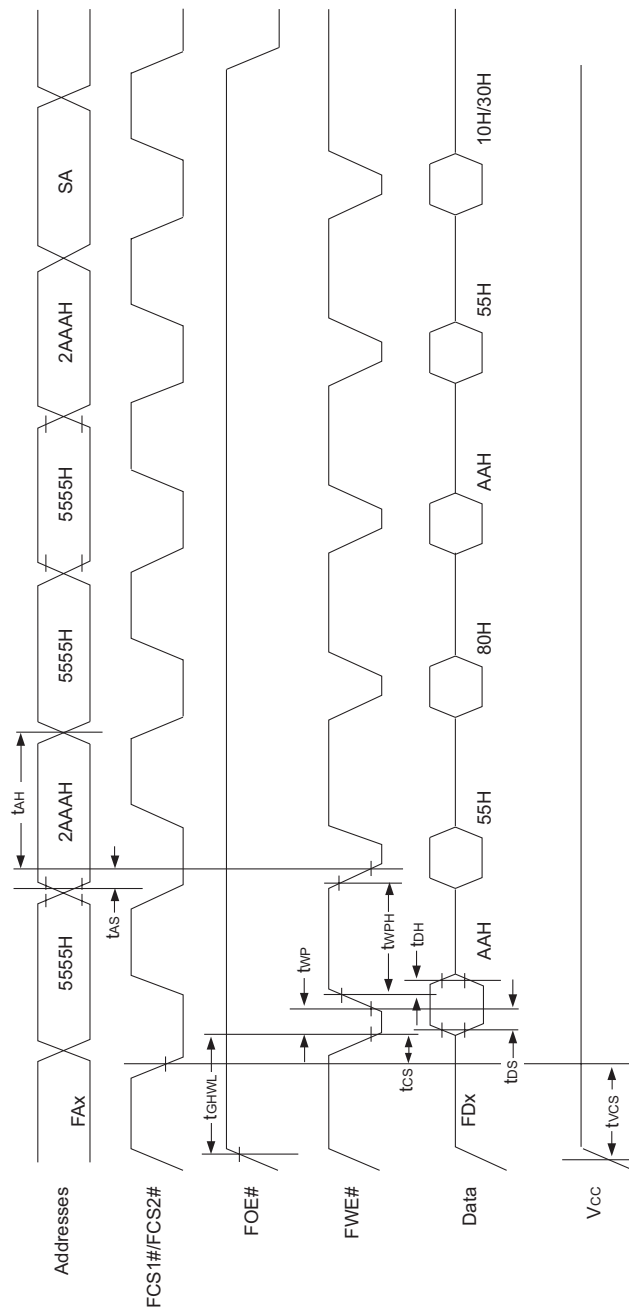
FIGURE 3 – AC WAVEFORMS FOR READ OPERATIONS



[illegible]



FIGURE 5 – AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTE:

1. SA is the sector address for Sector Erase.



FIG. 6 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS

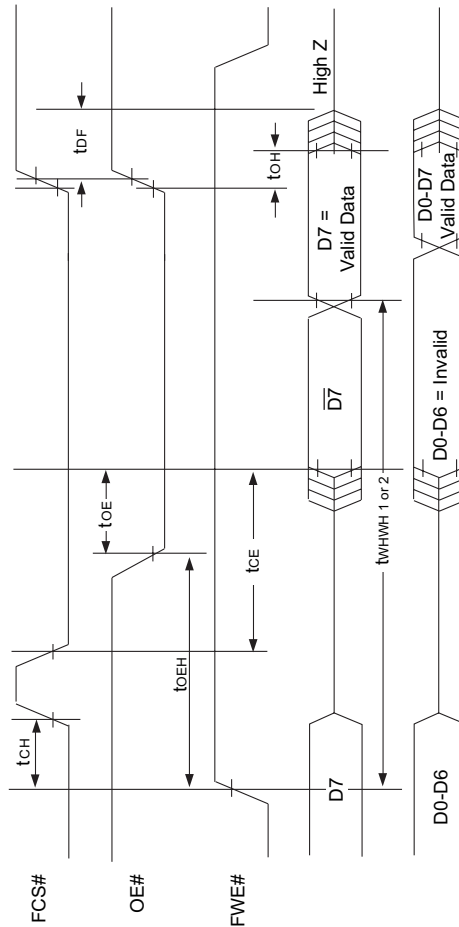
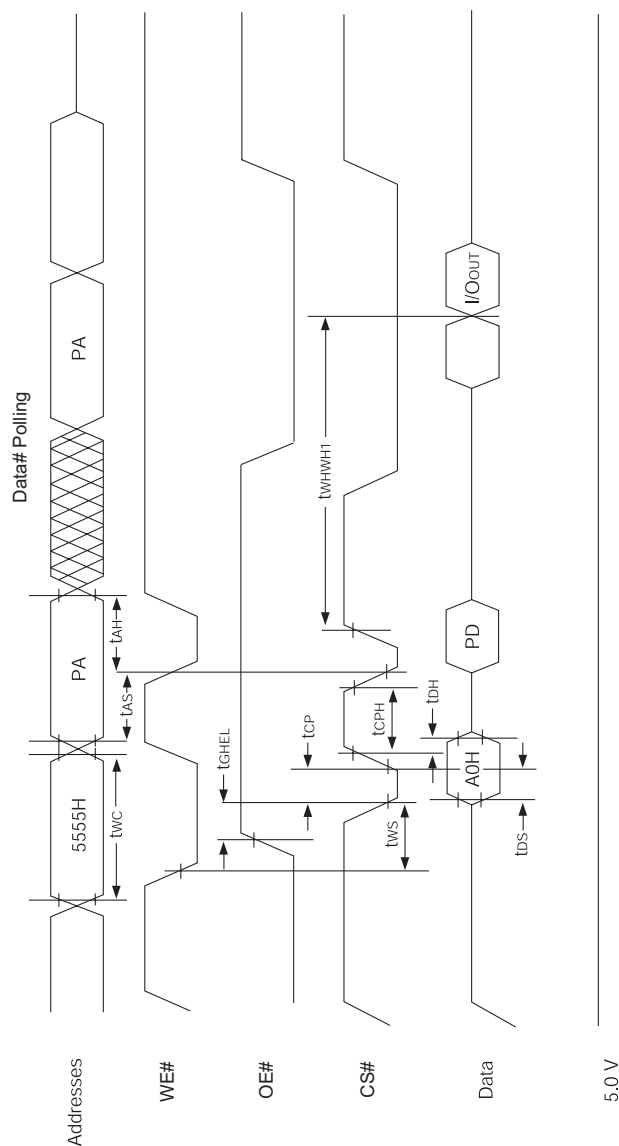




FIGURE 7 – ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS

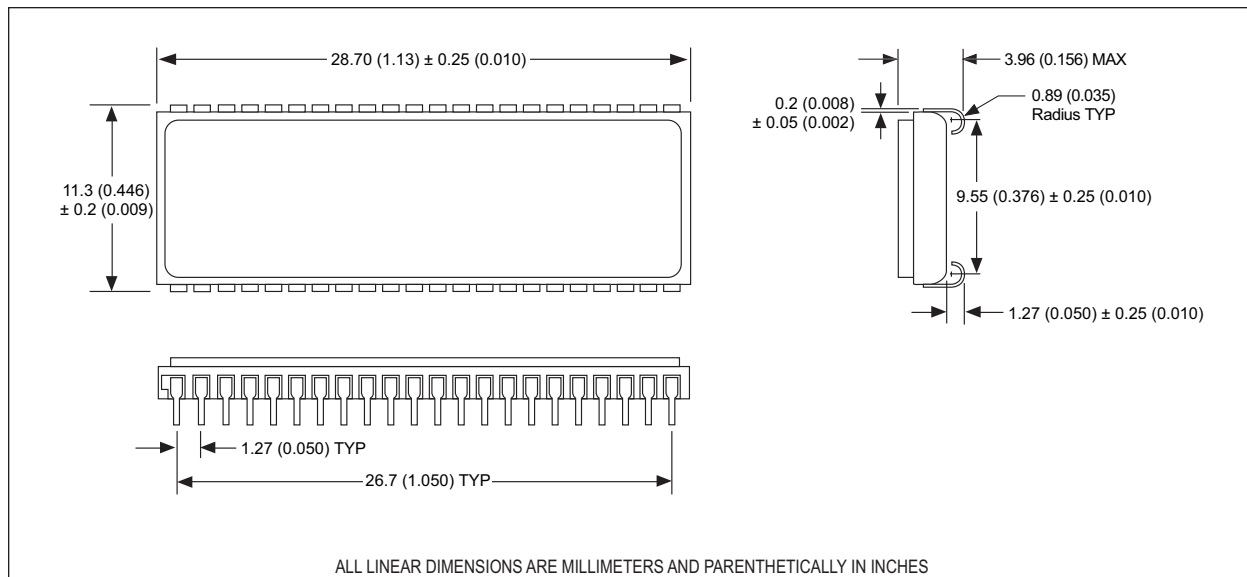


NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

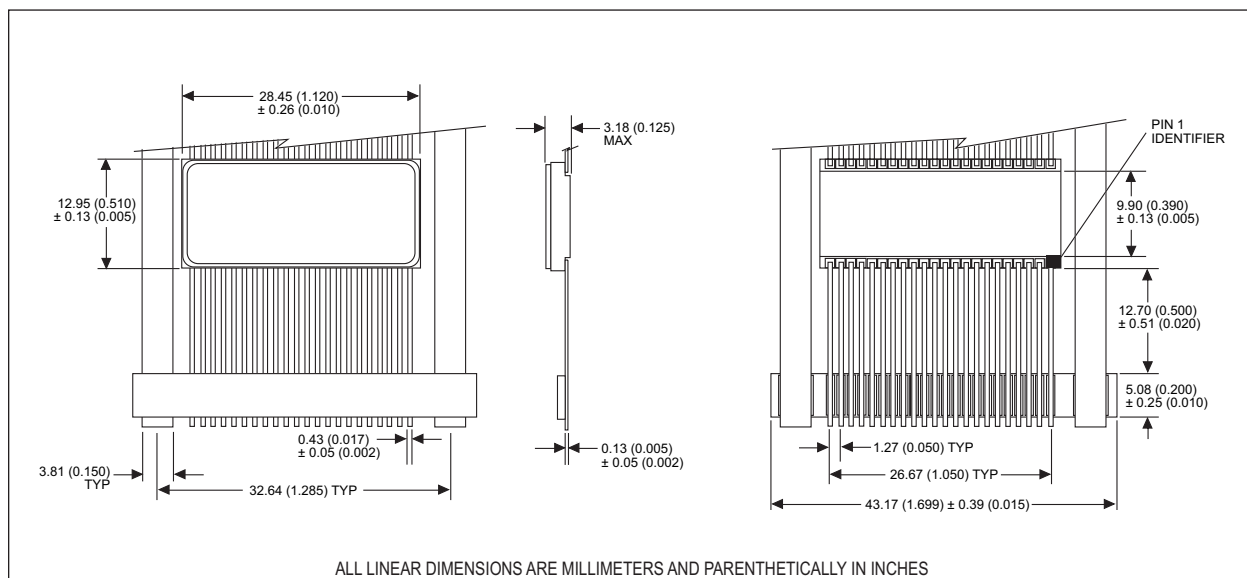


PACKAGE 102: 44 LEAD, CERAMIC SOJ**



** Package to be developed.

PACKAGE 208: 44 LEAD, CERAMIC FLAT PACK**



** Package to be developed.



PACKAGE 207: 56 LEAD, CERAMIC SOP*

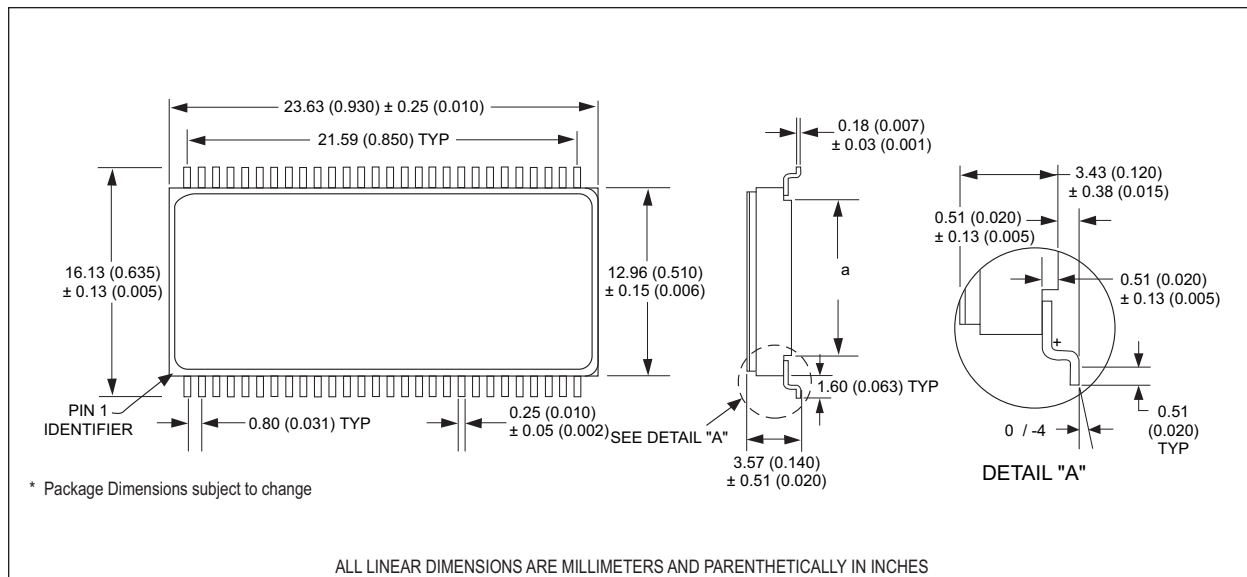
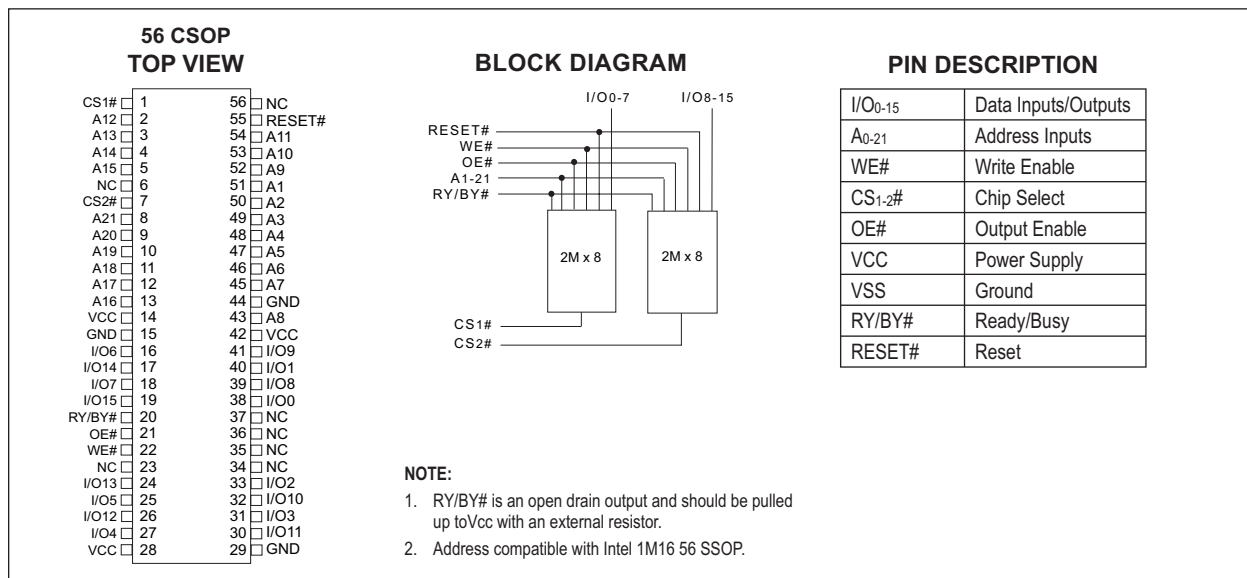
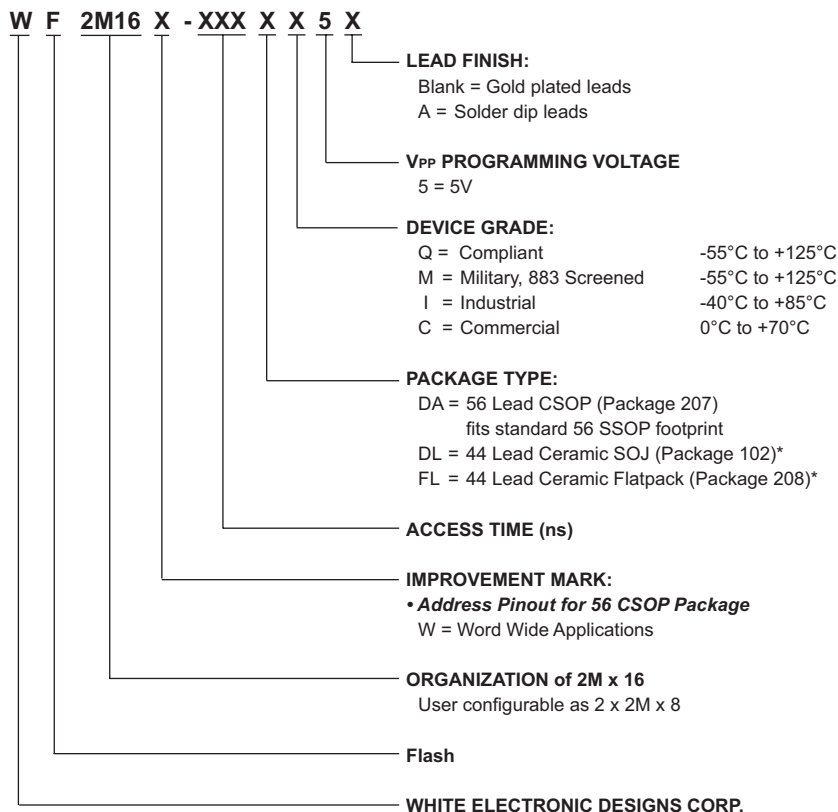


FIGURE 8 – ALTERNATE PIN CONFIGURATION FOR WF2M16W-XDAX5





ORDERING INFORMATION



* Package to be developed.

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
2M x 16 Flash MCP		150ns		5962-97610 04HXX
2M x 16 Flash MCP		120ns		5962-97610 05HXX
2M x 16 Flash MCP		90ns		5962-97610 06HXX