

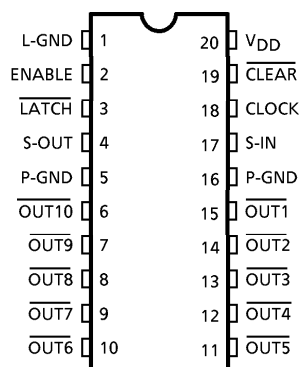
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

**TB62702P, TB62702F****10BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER / LATCH / 10SEGMENT LED DRIVERS**

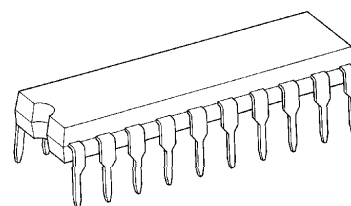
The TB62702P, TB62702F are specifically designed for 10-Segment LED Drivers and LED display. And these are monolithic integrated circuits designed to be used together with Bi-CMOS (DMOS) integrated circuit. The devices consist of a 10bit shift Register and 10bit Latches, and 10bit DMOS structures.

**FEATURES**

- 10bit serial-in parallel-out shift register / latch / 10segment LED driver (Bi-CMOS process)
- CMOS compatible inputs
- Open-drain DMOS outputs
- Low steady-state power consumption
- Serial data output for cascade operation
- Package ; P-type DIP-20-P-300A  
F-type SOP-20-P-300

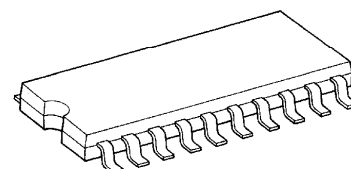
**PIN CONNECTION (TOP VIEW)**

TB62702P



DIP20-P-300-2.54A

TB62702F



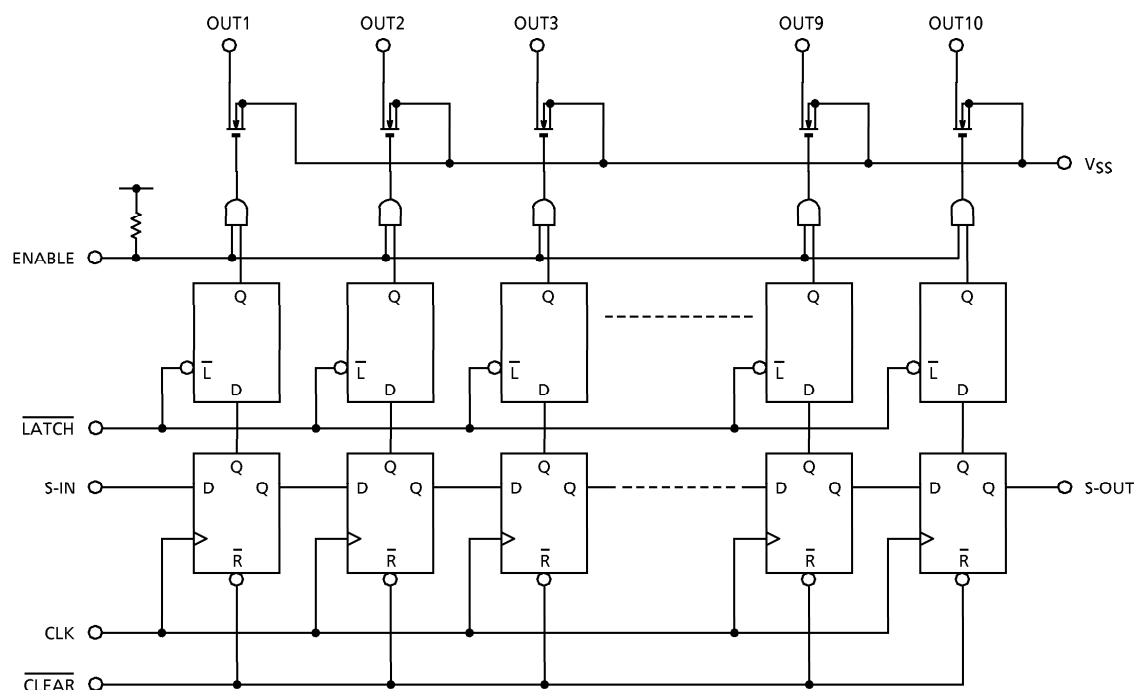
SOP20-P-300-1.27

**Weight**

DIP20-P-300-2.54A : 2.25g (Typ.)  
SOP20-P-300-1.27 : 0.48g (Typ.)

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**BLOCK DIAGRAM**

**MAXIMUM RATINGS** ( $T_a = 25^{\circ}\text{C}$ ,  $V_{SS} = 0\text{V}$ )

| CHARACTERISTIC              |   | SYMBOL            | RATING                   | UNIT               |
|-----------------------------|---|-------------------|--------------------------|--------------------|
| Supply Voltage              |   | $V_{DD}$          | $-0.3 \sim 7.0$          | V                  |
| Input Voltage               |   | $V_{IN}$          | $-0.3 \sim V_{DD} + 0.3$ | V                  |
| Output Drain-Source Voltage |   | $V_{OUT}$         | $-0.4 \sim 30$           | V                  |
| Input Current               |   | $I_{OUT}$         | 30                       | mA / bit           |
| Power Dissipation           | P | $P_D$<br>(Note 1) | 1.47                     | W                  |
|                             | F |                   | 0.96 (Note 2)            |                    |
| Operating Temperature       |   | $T_{opr}$         | $-40 \sim 85$            | $^{\circ}\text{C}$ |
| Storage Temperature         |   | $T_{stg}$         | $-55 \sim 150$           | $^{\circ}\text{C}$ |

(Note 1) Delated above  $25^{\circ}\text{C}$  in the proportion of  $11.7\text{mW}/^{\circ}\text{C}$  (P-type),  $7.7\text{mW}/^{\circ}\text{C}$  (F-type).

(Note 2) On Glass Epoxy ( $50 \times 50 \times 1.6\text{mm}$  Cu 40%)

RECOMMENDED OPERATING CONDITIONS ( $T_a = -40 \sim 85^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ )

| CHARACTERISTIC              |           | SYMBOL    | CONDITION                         | MIN.         | TYP. | MAX.         | UNIT    |
|-----------------------------|-----------|-----------|-----------------------------------|--------------|------|--------------|---------|
| Supply Voltage              |           | $V_{DD}$  | —                                 | 4.5          | 5    | 5.5          | V       |
| Input Current               | "H" Level | $V_{IH}$  | —                                 | $0.7 V_{DD}$ | —    | $V_{DD}$     | V       |
|                             | "L" Level | $V_{IL}$  | —                                 | 0            | —    | $0.3 V_{DD}$ |         |
| Output Drain-Source Voltage |           | $V_{OUT}$ | —                                 | —            | —    | 30           | V       |
| Output Current              |           | $I_{OUT}$ | Duty = 100%, All output "L" level | —            | —    | 24           | mA / ch |
| Power Dissipation           | P         | $P_D$     | —                                 | —            | —    | 760          | mW      |
|                             | F         |           | (Note 1)                          | —            | —    | 470          |         |

(Note 1) On Glass Epoxy (50×50×1.6mm Cu 40%)

ELECTRICAL CHARACTERISTICS ( $T_a = -40 \sim 85^\circ\text{C}$ ,  $V_{DD} = 4.5 \sim 5.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

| CHARACTERISTIC           |           | SYMBOL    | TEST CIR-CUIT | TEST CONDITION                                           | MIN.         | TYP.  | MAX.         | UNIT          |
|--------------------------|-----------|-----------|---------------|----------------------------------------------------------|--------------|-------|--------------|---------------|
| Output Voltage           | "L" Level | $V_{DS1}$ | —             | $I_{OUT} = 15\text{mA}$ , $T_a = 25^\circ\text{C}$       | —            | —     | 0.18         | V             |
|                          | "L" Level | $V_{DS1}$ | —             | $I_{OUT} = 15\text{mA}$                                  | —            | —     | 0.27         |               |
|                          | "L" Level | $V_{DS2}$ | —             | $I_{OUT} = 26\text{mA}$ , $T_a = 25^\circ\text{C}$       | —            | —     | 0.31         |               |
|                          | "L" Level | $V_{DS2}$ | —             | $I_{OUT} = 26\text{mA}$                                  | —            | —     | 0.47         |               |
| Output Resistor          |           | $R_{ON}$  | —             | $T_a = 25^\circ\text{C}$ , $I_{OUT} = 26\text{mA}$       | —            | —     | 12           | $\Omega$      |
| Output Current           |           | $I_{OZ1}$ | —             | $V_{OUT} = 30\text{V}$ , $EN = "L"$<br>1bit              | —            | —     | 10           | $\mu\text{A}$ |
|                          |           | $I_{OZ2}$ | —             | $V_{OUT} = 30\text{V}$ , $EN = "L"$<br>10bit             | —            | —     | $\pm 1$      |               |
| Input Current            |           | $I_{IN}$  | —             | $V_{IN} = V_{DD}$ or $V_{SS}$                            | —            | —     | $\pm 1$      | $\mu\text{A}$ |
|                          |           | $I_{IL}$  | —             | ENABLE, $V_{IN} = V_{SS}$                                | -27.5        | -55.0 | -110.0       |               |
| Output Current           | "H" Level | $I_{OH}$  | —             | S-OUT<br>$V_{DS} = 4.6\text{V}$ , $V_{DD} = 5.0\text{V}$ | -400         | -600  | —            | $\mu\text{A}$ |
|                          | "L" Level | $I_{OL}$  | —             | S-OUT<br>$V_{DS} = 0.4\text{V}$ , $V_{DD} = 5.0\text{V}$ | 400          | 600   | —            |               |
| Input Voltage            | "H" Level | $V_{IH}$  | —             | —                                                        | $0.7 V_{DD}$ | —     | $V_{DD}$     | V             |
|                          | "L" Level | $V_{IL}$  | —             | —                                                        | 0            | —     | $0.3 V_{DD}$ |               |
| Operating Supply Current |           | $I_{DD1}$ | —             | $f_{CLK} = 5\text{MHz}$<br>NO loads, 1bit                | —            | —     | 1500         | $\mu\text{A}$ |
| Supply Current           |           | $I_{DD2}$ | —             | —                                                        | —            | —     | 500          |               |

## SWITCHING CHARACTERISTICS

(Ta = 25°C, V<sub>DD</sub> = 5V, V<sub>OUT</sub> = 30V, R<sub>L</sub> = 1150Ω, C<sub>L</sub> = 15pF, "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>)

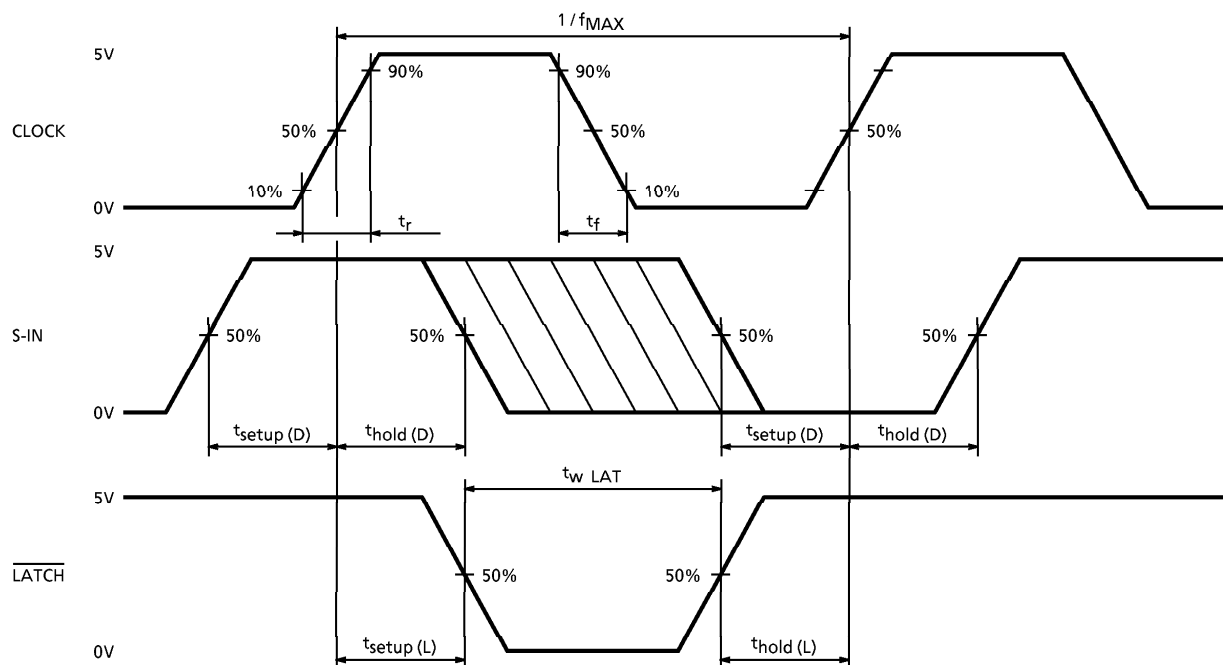
| CHARACTERISTIC                       | SYMBOL              | TEST CONDITION                 | MIN. | TYP. | MAX. | UNIT |
|--------------------------------------|---------------------|--------------------------------|------|------|------|------|
| Propagation Delay Time (Low-to-High) | CLK-OUTn            | LAT = "H", CLR = "H", EN = "H" | —    | —    | 250  | ns   |
|                                      | CLK-OUTn            |                                |      |      | 250  |      |
|                                      | LAT-OUTn            |                                |      |      | 200  |      |
|                                      | EN-OUTn             |                                |      |      | 150  |      |
| Propagation Delay Time (High-to-Low) | CLK-OUTn            | LAT = "H", CLR = "H", EN = "H" | —    | —    | 250  | ns   |
|                                      | LAT-OUTn            |                                |      |      | 200  |      |
|                                      | EN-OUTn             |                                |      |      | 150  |      |
|                                      | EN-OUTn             |                                |      |      | 150  |      |
| Set Up Time                          | CLK-LAT             | t <sub>setup</sub> (L)         | —    | —    | 50   | ns   |
|                                      | CLK-S-IN            | t <sub>setup</sub> (D)         | —    | —    | 35   |      |
| Hold Time                            | CLK-LAT             | t <sub>hold</sub> (L)          | —    | —    | 105  |      |
|                                      | CLK-S-IN            | t <sub>hold</sub> (D)          | —    | —    | 50   |      |
| Clock Pulse Width                    | t <sub>w</sub> CLK  | —                              | —    | —    | 100  | ns   |
| Latch Pulse Width                    | t <sub>w</sub> LATn | —                              | —    | —    | 50   |      |
| Clear Pulse Width                    | t <sub>w</sub> CLR  | —                              | —    | —    | 50   |      |
| Enable Pulse Width                   | t <sub>w</sub> EN   | —                              | —    | —    | 400  |      |
| Output Rise Time                     | t <sub>or</sub>     | OUTn                           | —    | —    | 1000 | ns   |
|                                      | t <sub>r</sub>      | S-OUT, V <sub>SS</sub> = 0V    | —    | —    | 50   |      |
| Output Fall Time                     | t <sub>of</sub>     | OUTn                           | —    | —    | 150  |      |
|                                      | t <sub>f</sub>      | S-OUT, V <sub>SS</sub> = 0V    | —    | —    | 50   |      |
| Maximum Clock Frequency              | f <sub>MAX1</sub>   | Duty = 50% Cascade connected   | 5    | 8    | —    | MHz  |
|                                      | f <sub>MAX2</sub>   | Duty = 50%                     | 6    | 12   | —    |      |

RECOMMENDED TIMING CONDITIONS (Ta = -40~85°C, V<sub>DD</sub> = 4.5~5.5V, V<sub>SS</sub> = 0)

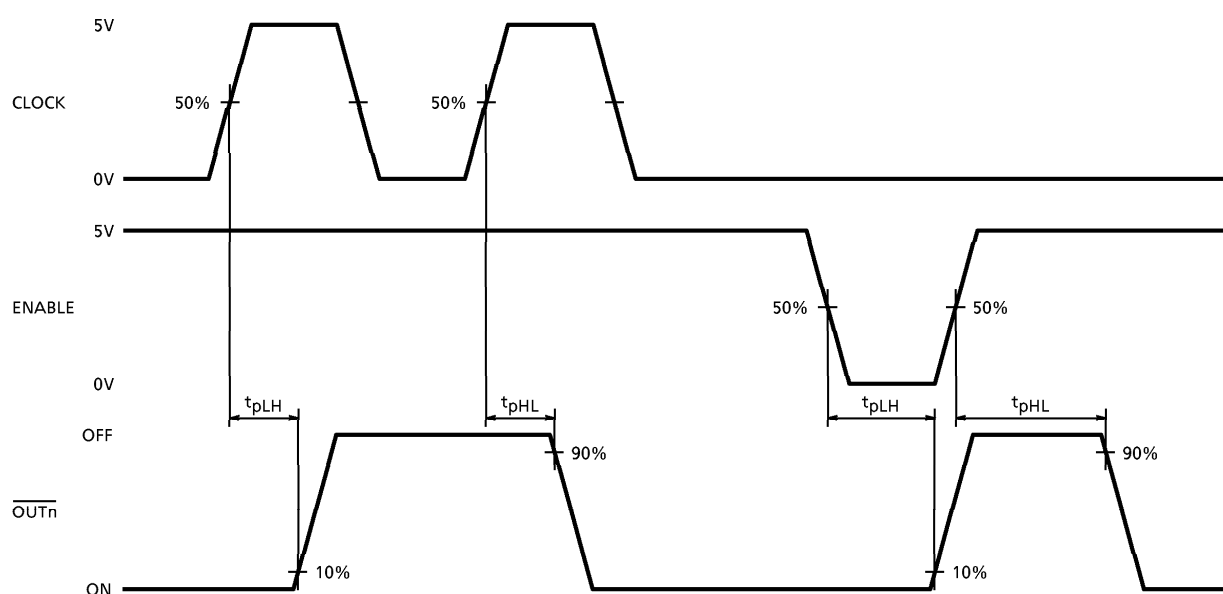
| CHARACTERISTIC     | SYMBOL             | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------------------|--------------------|----------------|------|------|------|------|
| Clock Pulse Width  | t <sub>w</sub> CLK | —              | 100  | —    | —    | ns   |
| Enable Pulse Width | t <sub>w</sub> EN  | —              | 400  | —    | —    | μs   |
| Latch Pulse Width  | t <sub>w</sub> LAT | —              | 100  | —    | —    | ns   |
| Clear Pulse Width  | t <sub>w</sub> CLR | —              | 100  | —    | —    | ns   |
| Data Set Up Time   | t <sub>setup</sub> | —              | 100  | —    | —    | ns   |
| Data Hold Time     | t <sub>hold</sub>  | —              | 150  | —    | —    | ns   |

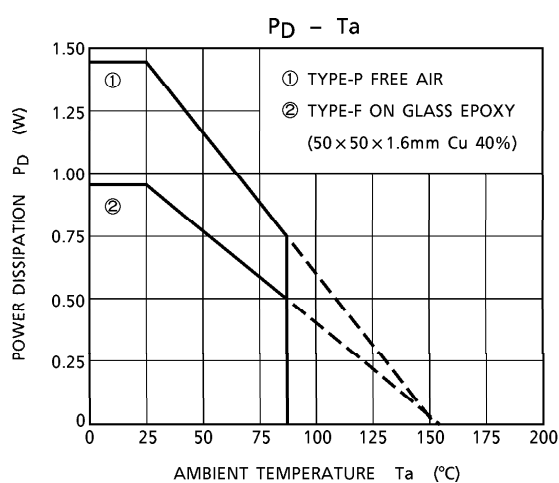
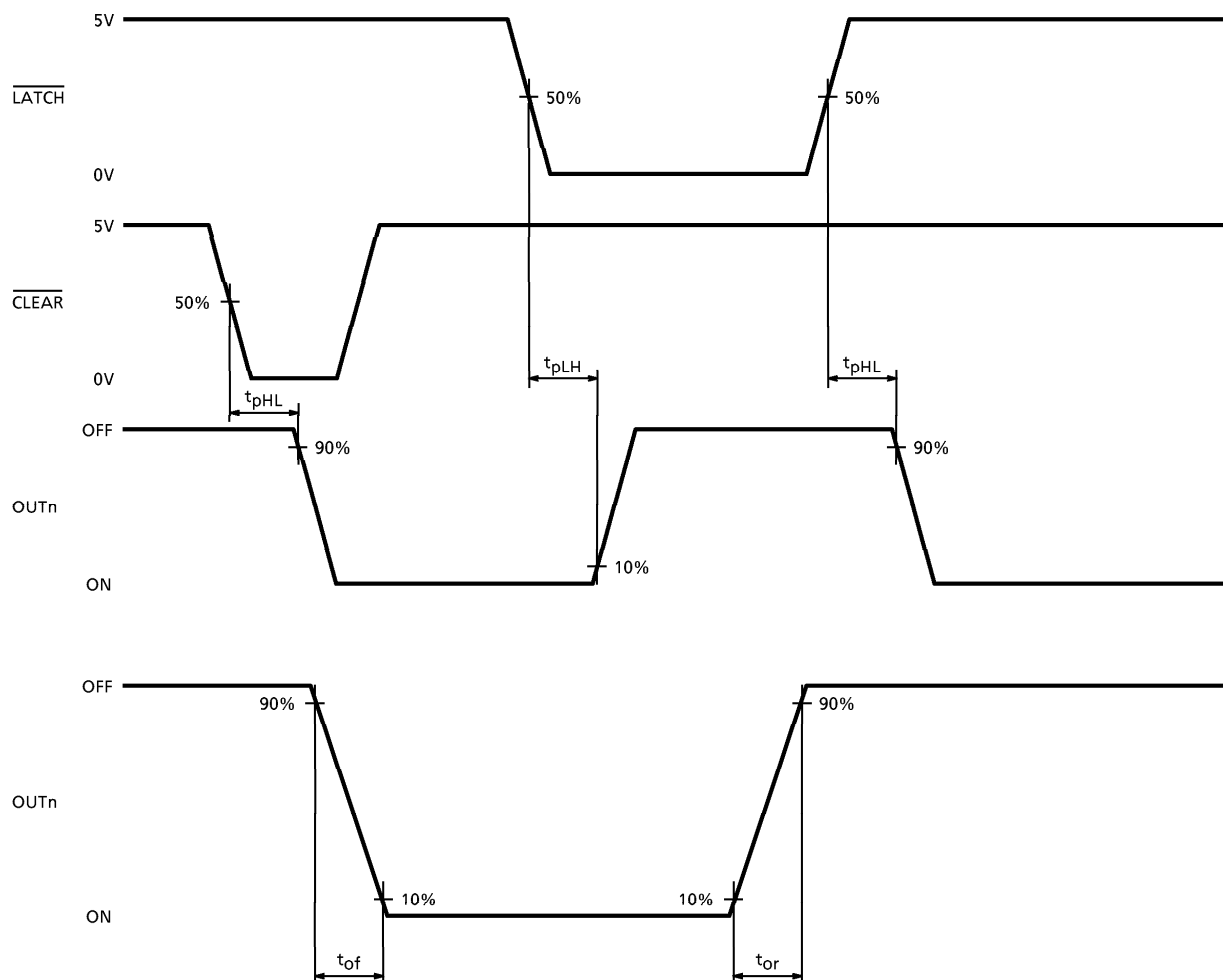
## TIMING DIAGRAM

## 1. Input timing diagram



## 2. Propagation delay time



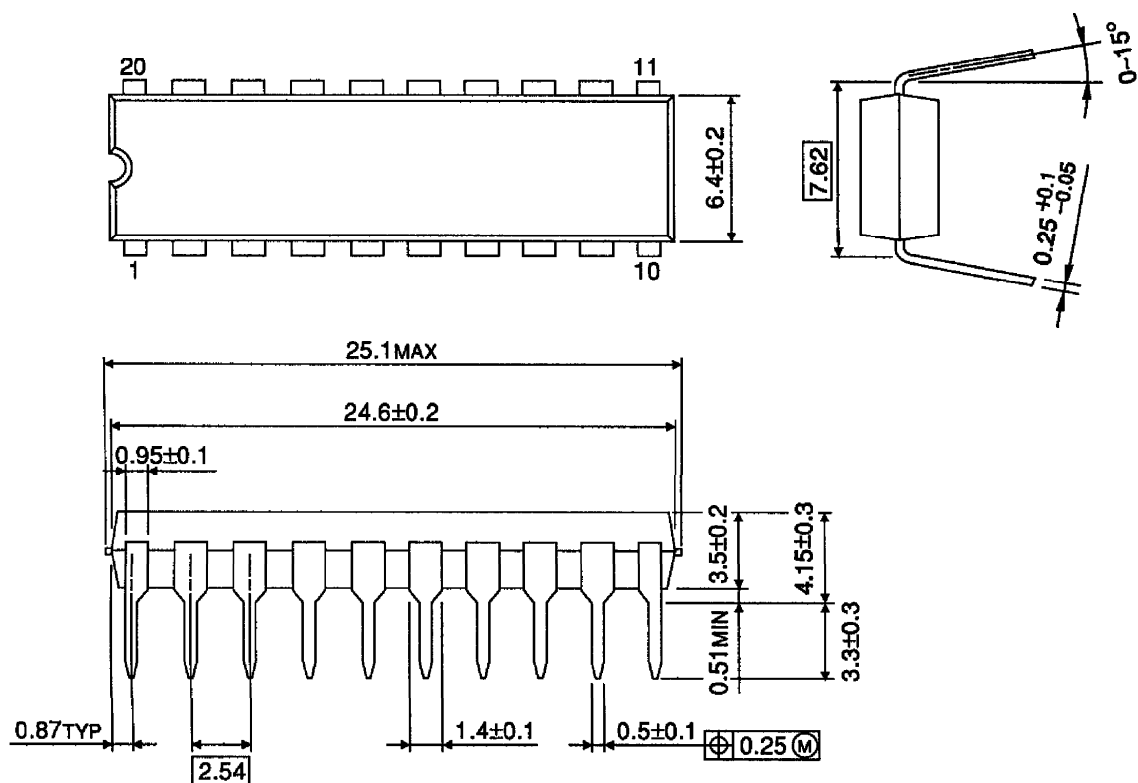


#### PRECAUTIONS for USING

Utmost care is necessary in the design of the output line,  $V_{CC}$  ( $V_{DD}$ ) and GND (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

**OUTLINE DRAWING**  
DIP20-P-300-2.54A

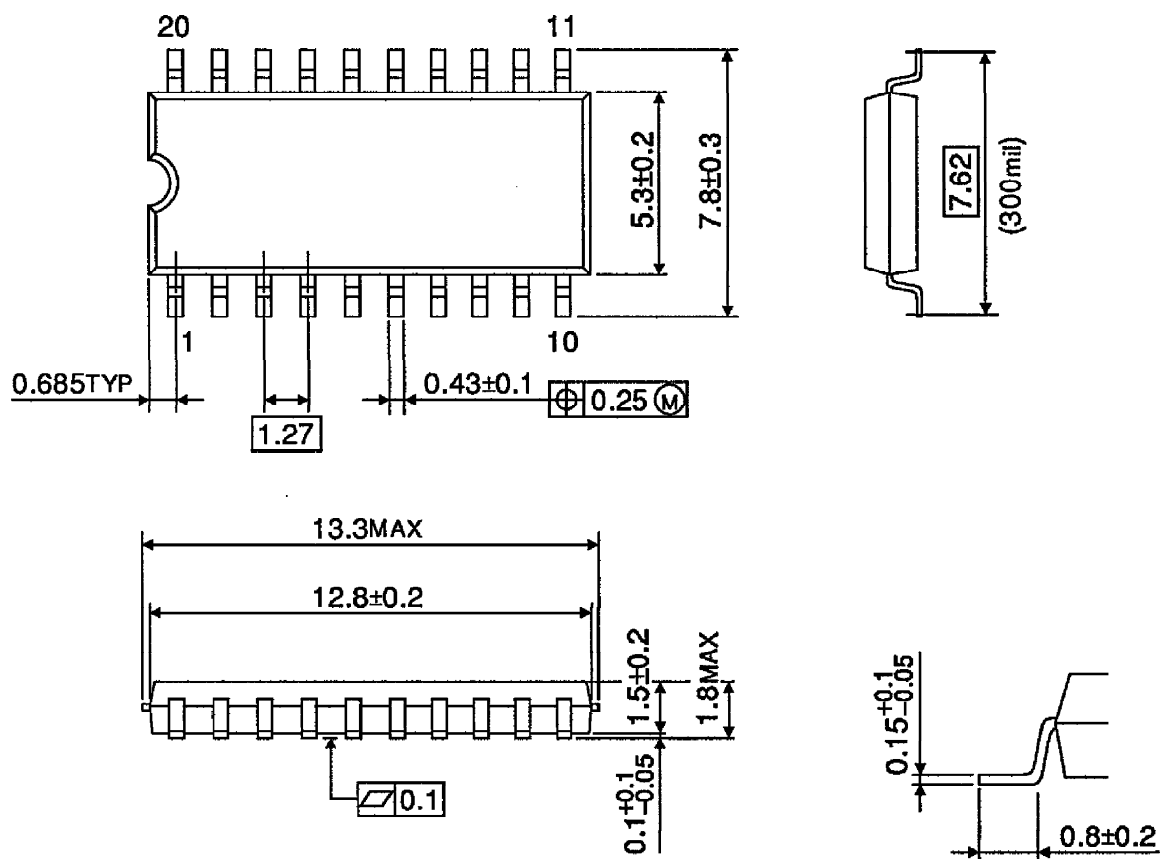
Unit : mm



Weight : 2.25g (Typ.)

**OUTLINE DRAWING**  
SOP20-P-300-1.27

Unit : mm



Weight : 0.48g (Typ.)