Low-Voltage, Low R_{ON} Quad SPST Analog Switch

DESCRIPTION

The DG2041/2042/2043 are quad single-pole/single-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, fast switching, low on-resistance ($R_{DS(on)}$: 1 Ω at 2.7 V) and small physical size, the DG2041/2042/2043 are ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2041/2042/2043 are built on Vishay Siliconix's new high density low voltage process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - $R_{DS(on)}$: 1 Ω
- Fast Switching - 14 ns t_{ON}
- Low Charge Injection - Q_{INJ}: 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- TSSOP-16 and QFN-16 Packages
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

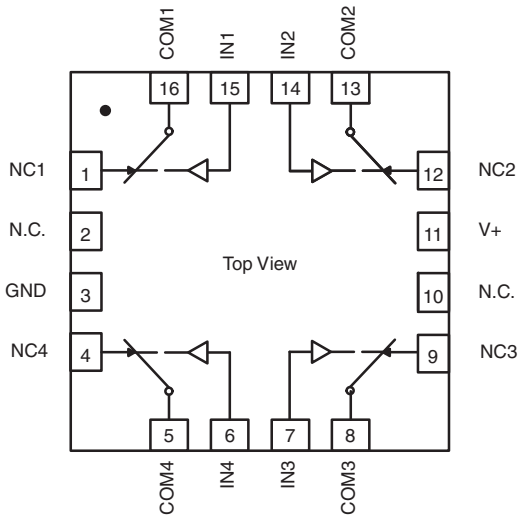
- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

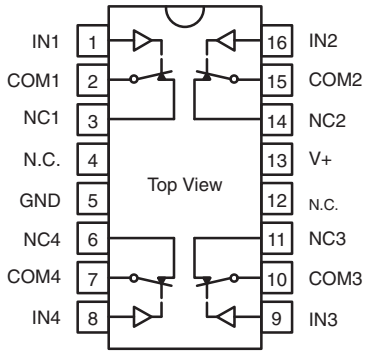
- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG2041

DG2041DN
QFN-16 (4 x 4)



DG2041DQ
TSSOP



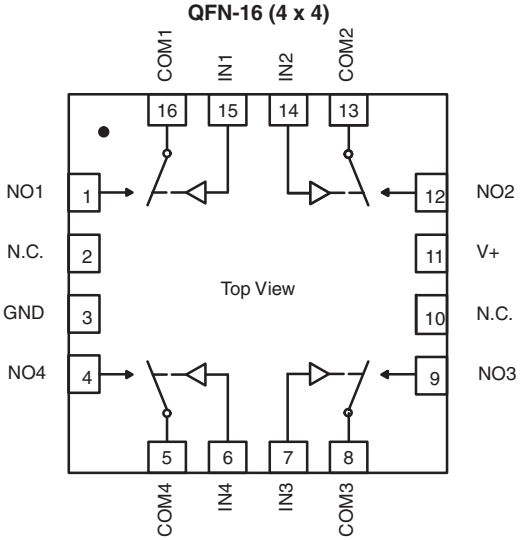
TRUTH TABLE - DG2041	
Logic	**Switch**
0	On
1	Off

Switches Shown for Logic "0" Input

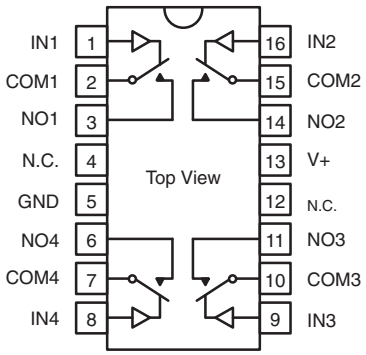
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FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG2042, DG2043

DG2042DN
QFN-16 (4 x 4)



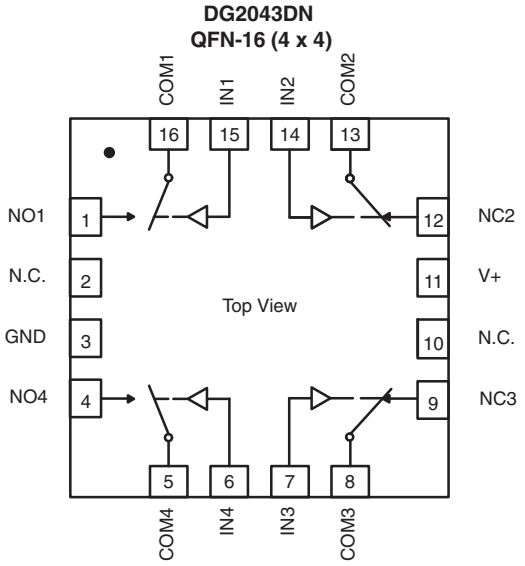
DG2042DQ
TSSOP



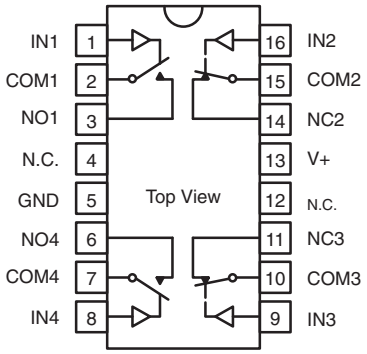
TRUTH TABLE - DG2042	
Logic	**Switch**
0	Off
1	On

Switches Shown for Logic “0” Input

DG2043DN
QFN-16 (4 x 4)



DG2043DQ
TSSOP



TRUTH TABLE - DG2043		
Logic	**Switches 1, 4**	**Switches 2, 3**
0	Off	On
1	On	Off

Switches Shown for Logic”0” Input

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ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 °C to 85 °C	TSSOP-16	DG2041DQ-T1
		DG2041DQ-T1-E3
		DG2042DQ-T1
		DG2042DQ-T1-E3
		DG2043DQ-T1
		DG2043DQ-T1-E3
	QFN-16 (4 mm x 4 mm) (Variation 1)	DG2041DN-T1-E4
		DG2042DN-T1-E4
		DG2043DN-T1-E4

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Limit	Unit
Reference V+ to GND			- 0.3 to + 6	V
IN, COM, NC, NO[a]			- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)			± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)			± 200	
Storage Temperature (D Suffix)			- 65 to 150	°C
Power Dissipation (Packages)[b]	TSSOP-16[c]		450	mW
	QFN-16 (4 mm x 4 mm)[d]		1880	

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 5.6 mW/°C above 70 °C
d. Derate 23.5 mW/°C above 70 °C
e. Manual soldering with soldering iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 2 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2 V, V_{IN} = 0.4 V or 1.6 V[e]	Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On- Resistance	R_{ON}	V+ = 2 V, V_{COM} = 0.2 V/1.2 V, I_{NO}, I_{NC} = 10 mA	Room Full		3	6.3 6.3	Ω
R_{ON} Flatness[d]	R_{ON} Flatness	V+ = 2 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room			4.2	
R_{ON} Match Between Channels	ΔR_{ON}		Room			0.4	
Switch Off Leakage Current[f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 2.2 V V_{NO}, V_{NC} = 0.2 V/2 V, V_{COM} = 2 V/0.2 V	Room Full[d]	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full[d]	- 1 - 10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 2.2 V, V_{NO}, V_{NC} = V_{COM} = 0.2 V/2 V	Room Full[d]	- 1 - 10		1 10	

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SPECIFICATIONS (V+ = 2 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 2 V, V_{IN} = 0.4 V or 1.6 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Digital Control							
Input High Voltage	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance[d]	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF fig. 1 and 2	Room Full[d]		30	81 82	ns
Turn-Off Time	t_{OFF}		Room Full[d]		22	41 42	
Break-Before-Make Time Delay	t_D	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF (DG2043 Only)	Room	5			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, fig. 2	Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 63		dB
Crosstalk[d]	X_{TALK}		Room		- 95		
NO, NC Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room		24		pF
Channel-On Capacitance[d]	C_{ON}		Room		48		
Power Supply							
Power Supply Current[d]	I+	V_{IN} = 0 V or V+			0.001	1	µA

SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 2 V[e]	**Temp.[a]**	**Limits - 40 to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 0.7 V/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		1.6	2.1 2.2	Ω
R_{ON} Flatness[d]	R_{ON} Flatness	V+ = 2.7 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room			0.7	
R_{ON} Match Between Channels	ΔR_{ON}		Room			0.3	
Switch Off Leakage Current[f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 0.3 V/3 V, V_{COM} = 3 V/0.3 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage[d]	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance[d]	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	- 1		1	µA

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SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 2 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF fig. 1 and 2	Room Full		19	51 52	ns
Turn-Off Time[d]	t_{OFF}		Room Full		17	36 37	
Break-Before-Make Time Delay	t_D	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF (DG2043 Only)	Room	2			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, fig. 2	Room		3		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 63		dB
Crosstalk[d]	X_{TALK}		Room		- 94		
NO, NC Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room		25		pF
Channel-On Capacitance[d]	C_{ON}		Room		49		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 V or V+			0.001	1	µA

SPECIFICATIONS (V+ = 5 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 4.5 V, V_{COM} = 0.7 V/2.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		1	1.5 1.6	Ω
R_{ON} Flatness[d]	R_{ON} Flatness	V+ = 4.5 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room			0.7	
R_{ON} Match Between Channels	ΔR_{ON}		Room			0.3	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	2.4			V
Input Low Voltage	V_{INL}		Full			0.8	
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	- 1		1	µA

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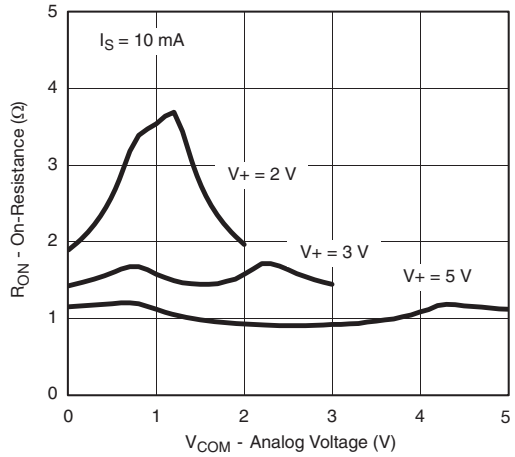
SPECIFICATIONS (V+ = 5 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** Min.[b]	Typ.[c]	Max.[b]	**Unit**
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF fig. 1 and 2	Room Full		13	42 43	ns
Turn-Off Time[d]	t_{OFF}		Room Full		19	32 33	
Break-Before-Make Time Delay	t_D	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF (DG2043 Only)	Room	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, fig. 2	Room		3		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 63		dB
Crosstalk[d]	X_{TALK}		Room		- 93		
Source-Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room		26		pF
Channel-On Capacitance[d]	C_{ON}		Room		49		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 V or V+			0.001	1	µA

Notes:
a. Room = 25 °C, full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

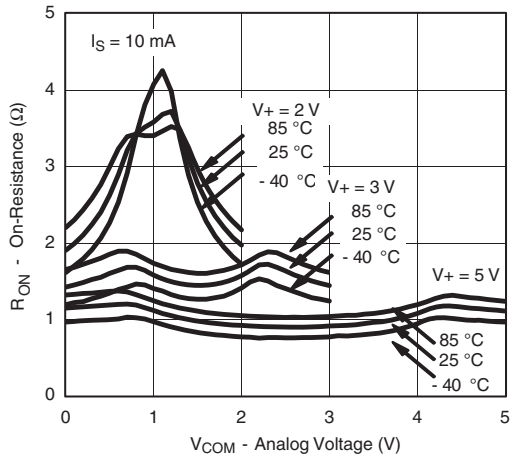
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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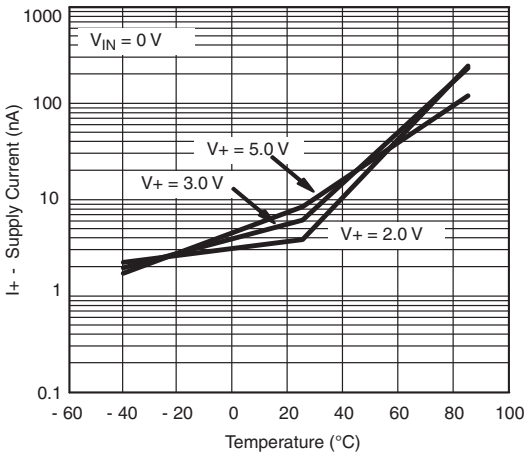
TYPICAL CHARACTERISTICS (25 °C unless noted)



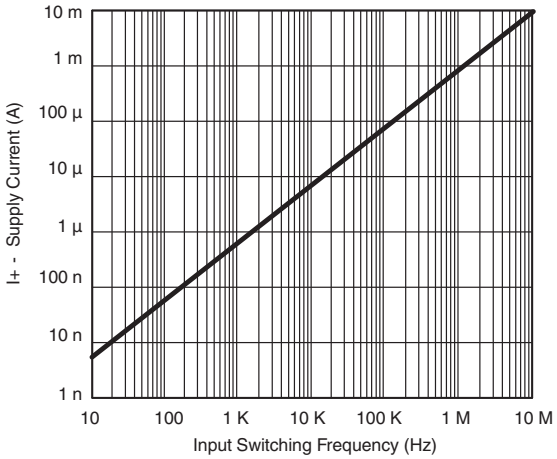
R_{ON} vs. V_{COM} and Supply Voltage



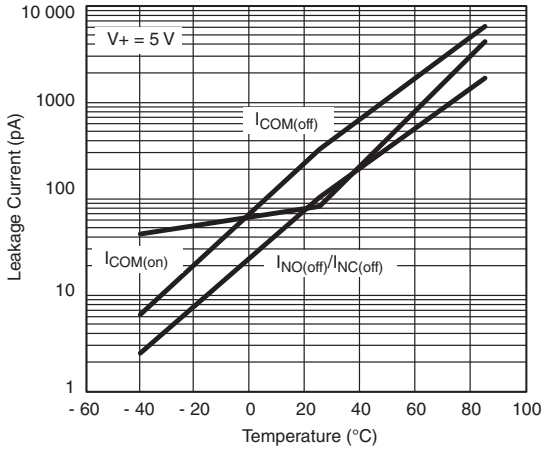
R_{ON} vs. Analog Voltage and Temperature



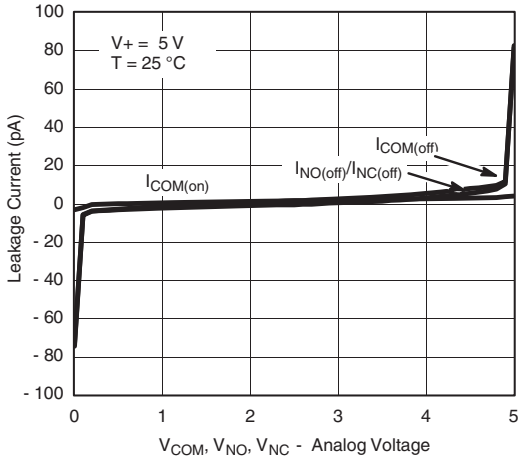
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency



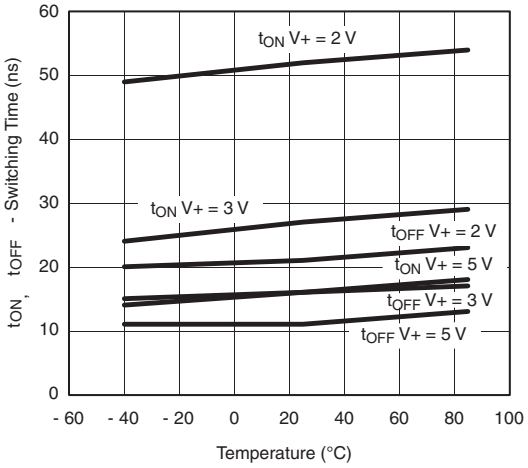
Leakage Current vs. Temperature



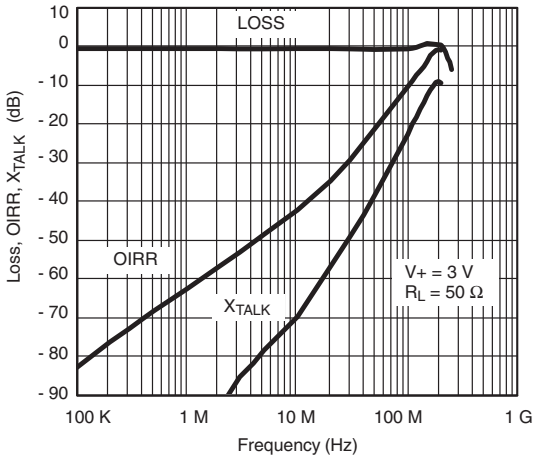
Leakage vs. Analog Voltage

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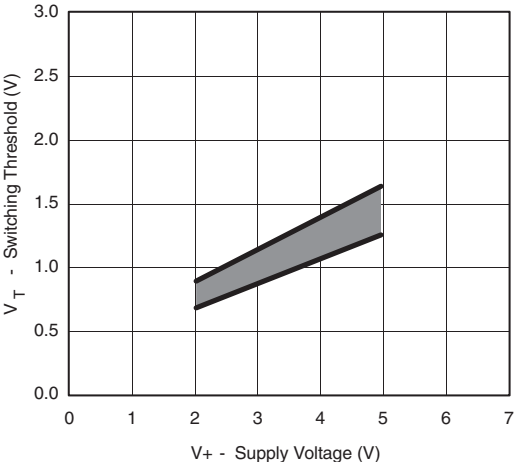
TYPICAL CHARACTERISTICS (25 °C unless noted)



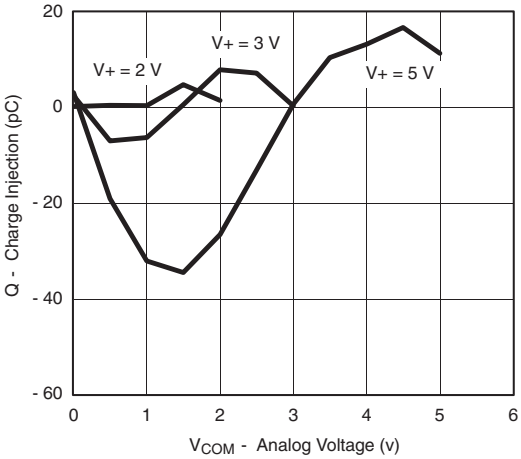
Switching Time vs. Temperature and Supply Voltage



Insertion Loss, Off-Isolation Crosstalk vs. Frequency



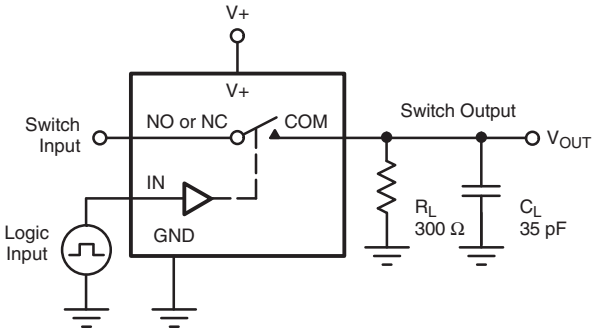
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

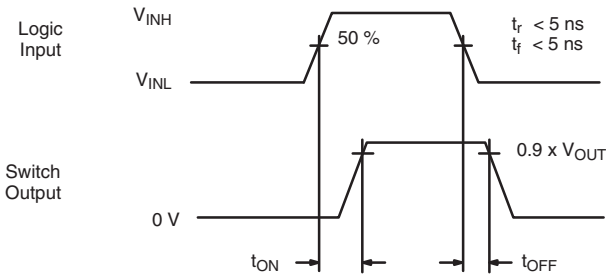
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TEST CIRCUITS



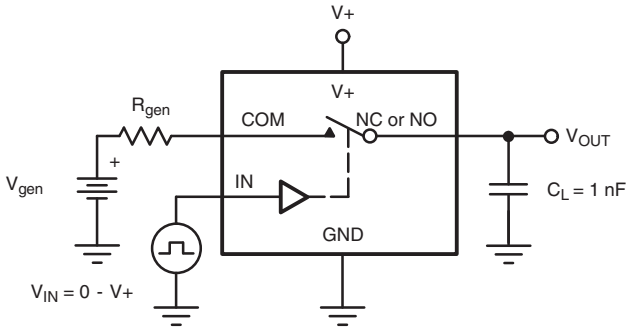
C_L (includes fixture and stray capacitance)

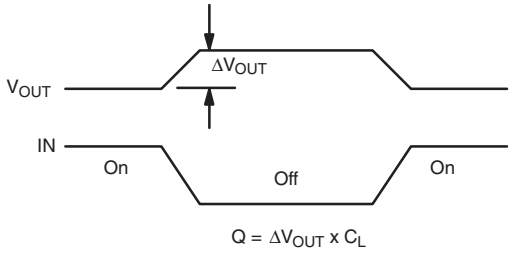
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

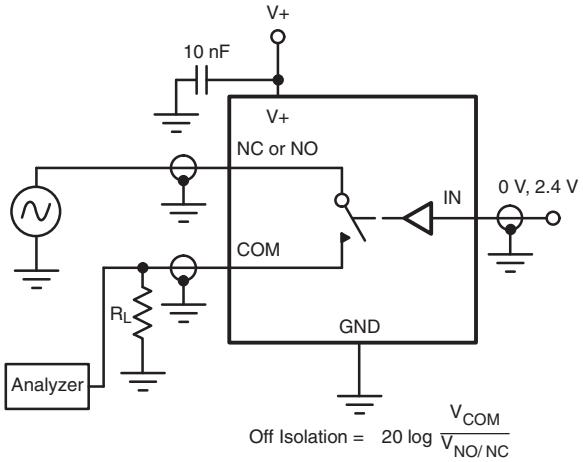




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2. Charge Injection



$$\text{Off Isolation} = 20 \log \frac{V_{COM}}{V_{NO/NC}}$$

Figure 3. Off-Isolation

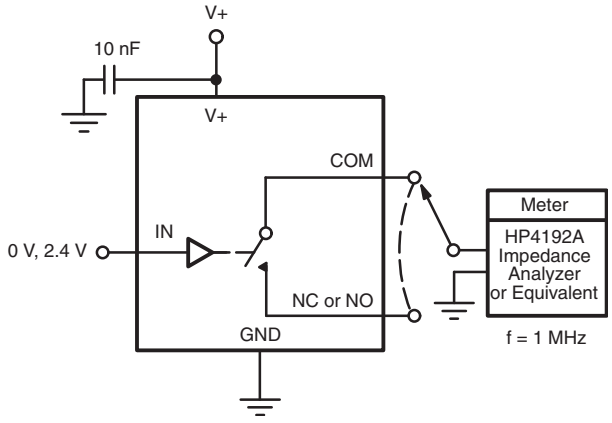
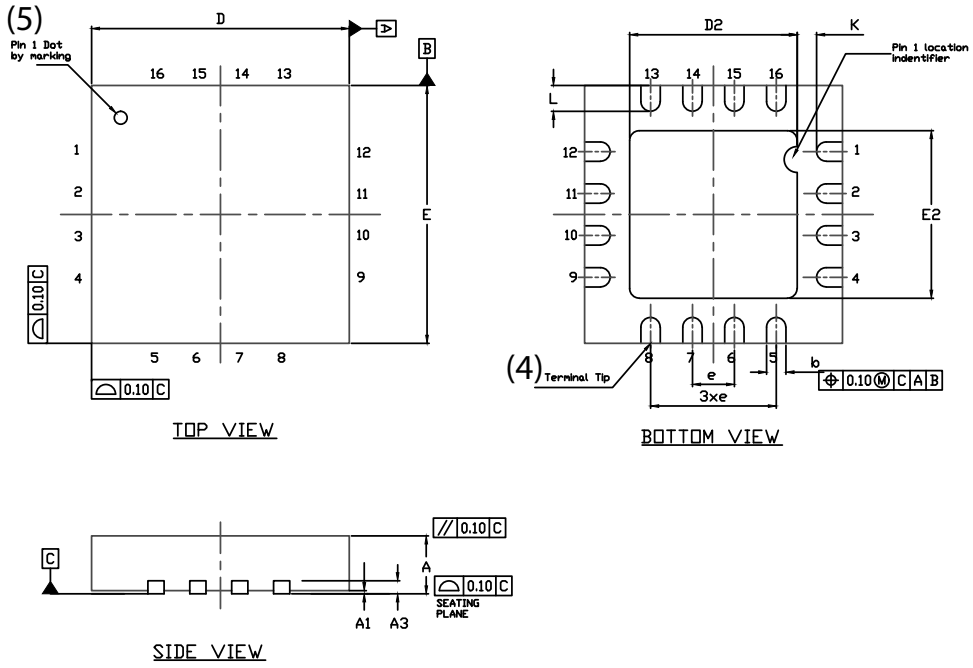


Figure 4. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72091.

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QFN 4x4-16L Case Outline



DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS[1]			INCHES			MILLIMETERS[1]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N[3]	16			16			16			16		
Nd[3]	4			4			4			4		
Ne[3]	4			4			4			4		

Notes

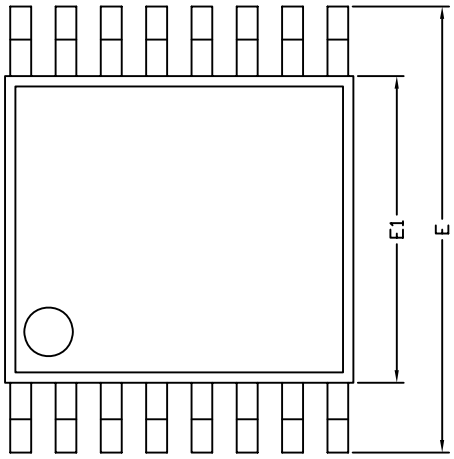
(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

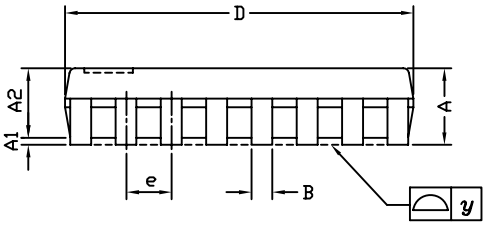
ECN: S13-0893-Rev. B, 22-Apr-13
DWG: 5890

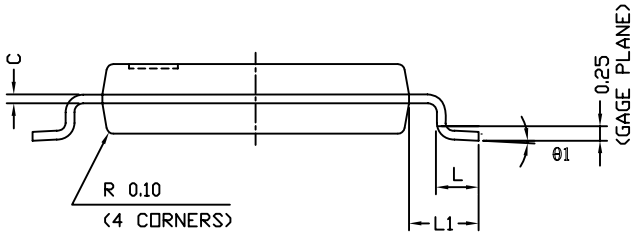
For technical questions, contact: powerictechsupport@vishay.com

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TSSOP: 16-LEAD

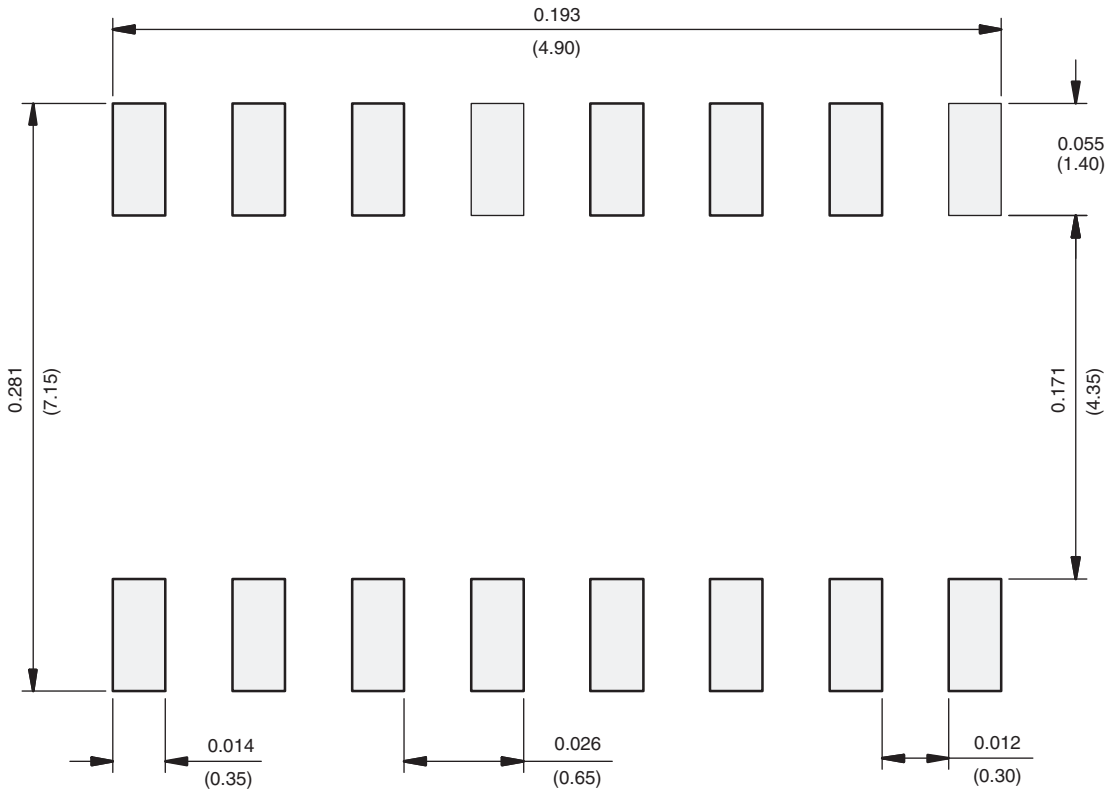






Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

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