

TLV970x Low Noise, Rail-to-Rail Output Operational Amplifiers

1 Features

- Output Swing Includes Both Supply Rails
- Low Noise: 15 nV/√Hz at f = 1 kHz (Typical)
- Low Input Bias Current: 1 pA (Typical)
- Low Power: 230 μA/Channel
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage: 400 μV at T_A = 25°C

2 Applications

- AC Inverter and VF Drives
- Currency Counters
- Servo Drives and Motion Control
- Smoke Detectors
- Test Equipment
- Oscilloscopes
- Appliances
- Industrial Automation

3 Description

The dual-channel TLV9702 and quad-channel TLV9704 operational amplifiers (op amps) provide rail-to-rail output performance to increase dynamic range in single or split-supply applications. The devices offer low supply current for battery-powered applications, while providing adequate AC performance for applications such as passive safety or other near-DC applications. The TLV9702 and TLV9704 devices feature excellent low noise performance across a wide range of supply voltages. [Equivalent Input Noise Voltage vs Frequency](#) shows the low level of noise voltage for this CMOS amplifier, with only 230 μA (typical) of supply current per amplifier.

The TLV9702 and TLV9704 devices exhibit high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. The micropower dissipation levels of the family help reduce power consumption in handheld monitoring and remote sensing applications. The op amps feature rail-to-rail output with single or split supplies for driving analog-to-digital converters (ADCs). The TLV970x family has a maximum input offset voltage of 1.1 mV and is fully characterized at 5 V and ±5 V.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV9702	SOIC (8)	4.90 mm × 3.91 mm
	TSSOP (8)	3.00 mm × 4.40 mm
TLV9704	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Equivalent Input Noise Voltage vs Frequency

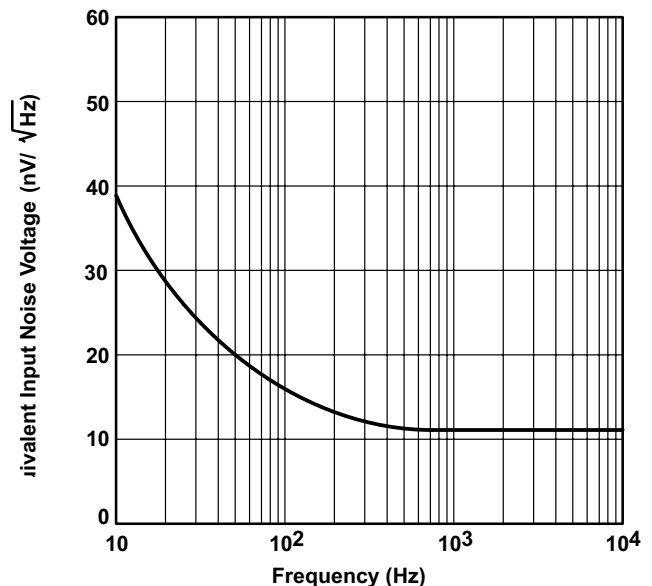


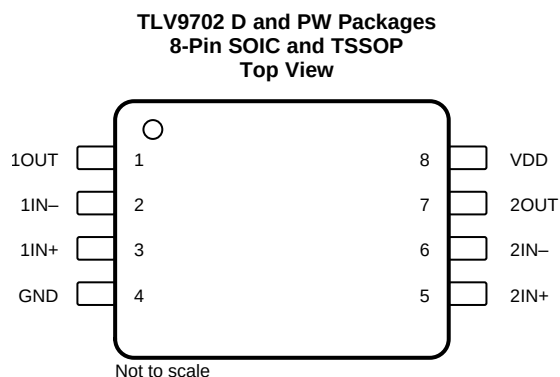
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4 Revision History

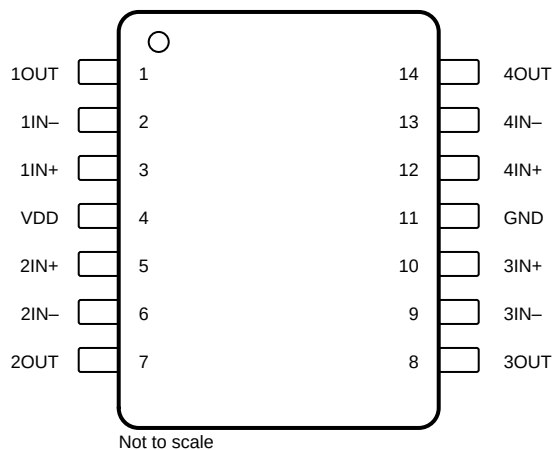
DATE	REVISION	NOTES
January 2018	*	Initial release.

5 Pin Configuration and Functions



Pin Functions: TLV9702

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input, channel 1
1IN+	3	I	Noninverting input, channel 1
1OUT	1	O	Output, channel 1
2IN+	5	I	Noninverting input, channel 2
2IN–	6	I	Inverting input, channel 2
2OUT	7	O	Output, channel 2
GND	4	—	Ground connection
VDD	8	—	Positive power supply

**TLV9704 D and PW Packages
14-Pin SOIC and TSSOP
Top View**

Pin Functions: TLV9704

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input, channel 1
1IN+	3	I	Noninverting input, channel 1
1OUT	1	O	Output, channel 1
2IN+	5	I	Noninverting input, channel 2
2IN–	6	I	Inverting input, channel 2
2OUT	7	O	Output, channel 2
3IN–	9	I	Inverting input, channel 3
3IN+	10	I	Noninverting input, channel 3
3OUT	8	O	Output, channel 3
4IN–	13	I	Inverting input, channel 4
4IN+	12	I	Noninverting input, channel 4
4OUT	14	I	Output, channel 4
GND	11	—	Ground connection
VDD	4	—	Positive power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V_{DD+} ⁽²⁾		8	V
Supply voltage, V_{DD-} ⁽²⁾		–8	V
Differential input voltage, V_{ID} ⁽³⁾		±16	V
Input voltage, V_I (any input) ⁽²⁾	$V_{DD-} - 0.3$	V_{DD+}	V
Input current, I_I (each input)		±5	mA
Output current, I_O		±50	mA
Total current into V_{DD+}		±50	mA
Total current out of V_{DD-}		±50	mA
Duration of short-circuit current at (or below) 25°C ⁽⁴⁾	Unlimited		
Operating free-air temperature, T_A	–40	125	°C
Storage temperature, T_{stg}	–60	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
- (3) Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
- (4) The output may be shorted to either supply. Temperature or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
$V_{DD\pm}$ Supply voltage	±2.2		±8	V
V_I Input voltage	V_{DD-}		$V_{DD+} - 1.5$	V
V_{IC} Common-mode input voltage	V_{DD-}		$V_{DD+} - 1.5$	V

6.4 Thermal Information: TLV9702

THERMAL METRIC ⁽¹⁾		TLV9702		UNIT
		D (SOIC)	PW (TSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136.1	149	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.3	—	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.2	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.0	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.7	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: TLV9704

THERMAL METRIC ⁽¹⁾		TLV9704		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.1	110.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.7	28.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.3	59.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.4	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.6	56.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 TLV970x Electrical Characteristics: $V_{DD} = 5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$ $V_{IC} = 0$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		400	1100	μV
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			1600	
αV_{IO}	Temperature coefficient of input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$ $V_{IC} = 0$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C to } 85^\circ\text{C}$		2		$\mu\text{V}/^\circ\text{C}$
	Input offset voltage long-term drift ⁽²⁾	$V_{DD\pm} = \pm 2.5\text{ V}$ $V_{IC} = 0$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		0.003		$\mu\text{V}/\text{mo}$
I_{IO}	Input offset current	$V_{DD\pm} = \pm 2.5\text{ V}$ $V_{IC} = 0$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		0.5		pA
			$T_A = 85^\circ\text{C}$			150	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			800	
I_{IB}	Input bias current	$V_{DD\pm} = \pm 2.5\text{ V}$ $V_{IC} = 0$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$		1		pA
			$T_A = 85^\circ\text{C}$			170	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			800	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$ $ V_{IO} \leq 5\text{ mV}$	$T_A = 25^\circ\text{C}$	0 to 4	-0.3 to 4.2		V
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -400\ \mu\text{A}$	$T_A = 25^\circ\text{C}$		4.99		V
			$T_A = 25^\circ\text{C}$	4.85	4.94		
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	4.82			
			$T_A = 25^\circ\text{C}$	4.7	4.85		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5\text{ V}$ $I_{OL} = 50\ \mu\text{A}$ $V_{IC} = 2.5\text{ V}$ $I_{OL} = 500\ \mu\text{A}$ $V_{IC} = 2.5\text{ V}$ $I_{OL} = 4\text{ mA}$	$T_A = 25^\circ\text{C}$		0.01		V
			$T_A = 25^\circ\text{C}$		0.09	0.15	
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			0.15	V
			$T_A = 25^\circ\text{C}$		0.7	1	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$ $V_O = 1\text{ V to } 4\text{ V}$	$R_L = 50\text{ k}\Omega$ ⁽³⁾	$T_A = 25^\circ\text{C}$	80	170	V/mV
				$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	50		
			$R_L = 1\text{ M}\Omega$, $T_A = 25^\circ\text{C}$ ⁽³⁾		550		
r_{id}	Differential input resistance	$T_A = 25^\circ\text{C}$			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance	$T_A = 25^\circ\text{C}$			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10\text{ kHz}$, P package $T_A = 25^\circ\text{C}$			8		pF
z_o	Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$ $T_A = 25^\circ\text{C}$			240		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.7\text{ V}$ $V_O = 2.5\text{ V}$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	70	80		dB
			$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	70			

(1) The full temperature range is $-40^\circ\text{C to } +125^\circ\text{C}$.

(2) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated at $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

(3) Referenced to 2.5 V

6.7 TLV970x Operating Characteristics: $V_{DD} = 5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$ $V_{IC} = V_{DD} / 2$ No load	$T_A = 25^\circ\text{C}$	80	95		dB
			$T_A = -40^\circ\text{C to }+125^\circ\text{C}$	80			
I_{DD}	Supply current per channel	$V_O = 2.5\text{ V (no load)}$	$T_A = 25^\circ\text{C}$		230	270	μA
			$T_A = -40^\circ\text{C to }+125^\circ\text{C}$			280	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}$ $C_L = 100\text{ pF}^{(2)}$ $R_L = 50\text{ k}\Omega^{(2)}$	$T_A = 25^\circ\text{C}$	0.3	0.45		$\text{V}/\mu\text{s}$
			$T_A = -40^\circ\text{C to }+125^\circ\text{C}$	0.25			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	$T_A = 25^\circ\text{C}$		40		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	$T_A = 25^\circ\text{C}$		15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	$T_A = 25^\circ\text{C}$		0.7		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	$T_A = 25^\circ\text{C}$		1.3		
I_n	Equivalent input noise current	$T_A = 25^\circ\text{C}$			0.6		$\text{fA}/\sqrt{\text{Hz}}$
	Total harmonic distortion plus noise (THD + N)	$V_O = 0.5\text{ V to }2.5\text{ V}$ $f = 20\text{ kHz}$ $R_L = 50\text{ k}\Omega^{(2)}$ $T_A = 25^\circ\text{C}$	$A_V = 1$		0.02%		
			$A_V = 10$		0.03%		
	Gain-bandwidth product	$f = 50\text{ kHz}$ $C_L = 100\text{ pF}^{(2)}$ $R_L = 50\text{ k}\Omega^{(2)}$ $T_A = 25^\circ\text{C}$			800		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$ $R_L = 50\text{ k}\Omega^{(2)}$ $A_V = 1$ $C_L = 100\text{ pF}^{(2)}$ $T_A = 25^\circ\text{C}$			185		kHz
t_S	Settling time	$A_V = -1$ Step = $0.5\text{ V to }2.5\text{ V}$ $R_L = 50\text{ k}\Omega^{(2)}$ $C_L = 100\text{ pF}^{(2)}$ $T_A = 25^\circ\text{C}$	To 0.1%		6.5		μs
			To 0.01%		15		
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^{(2)}$ $C_L = 100\text{ pF}^{(2)}$ $T_A = 25^\circ\text{C}$			56°		
	Gain margin				11		

(1) The full temperature range is $-40^\circ\text{C to }+125^\circ\text{C}$.

(2) Referenced to 2.5 V

6.8 TLV970x Electrical Characteristics: $V_{DD\pm} = \pm 5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$ $R_S = 50\ \Omega$ $V_O = 0$	$T_A = 25^\circ\text{C}$		400	1100	μV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			1600	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0$ $R_S = 50\ \Omega$ $V_O = 0$ $T_A = 25^\circ\text{C}$ to 85°C			2		$\mu\text{V}/^\circ\text{C}$
	Input offset voltage long-term drift ⁽²⁾	$V_{IC} = 0$ $R_S = 50\ \Omega$ $V_O = 0$ $T_A = 25^\circ\text{C}$			0.003		$\mu\text{V}/\text{mo}$
I_{IO}	Input offset current	$V_{IC} = 0$ $R_S = 50\ \Omega$ $V_O = 0$	$T_A = 25^\circ\text{C}$		0.5		pA
			$T_A = 85^\circ\text{C}$			150	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			800	
I_{IB}	Input bias current	$V_{IC} = 0$ $R_S = 50\ \Omega$ $V_O = 0$	$T_A = 25^\circ\text{C}$		1		pA
			$T_A = 85^\circ\text{C}$			170	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			800	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	$T_A = 25^\circ\text{C}$	-5 to 4	-5.3 to 4.2		V
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	$I_{OH} = -20\ \mu\text{A}$	$T_A = 25^\circ\text{C}$		4.99		V
			$T_A = 25^\circ\text{C}$	4.85	4.94		
		$I_{OH} = -100\ \mu\text{A}$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	4.82			
			$T_A = 25^\circ\text{C}$	4.7	4.85		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	4.5			
V_{OM-}	Maximum negative peak output voltage	$V_{IC} = 0$ $I_O = 50\ \mu\text{A}$	$T_A = 25^\circ\text{C}$		-4.99		V
			$T_A = 25^\circ\text{C}$	-4.85	-4.91		
		$V_{IC} = 0$ $I_O = 500\ \mu\text{A}$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-4.85			
			$T_A = 25^\circ\text{C}$	-4	-4.3		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-3.8			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 50\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	80	200	V/mV
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	50		
			$R_L = 1\text{ M}\Omega$ $T_A = 25^\circ\text{C}$		1000		
$r_{i(d)}$	Differential input resistance	$T_A = 25^\circ\text{C}$			10 ₁₂		Ω
$r_{i(c)}$	Common-mode input resistance	$T_A = 25^\circ\text{C}$			10 ₁₂		Ω
$C_{i(c)}$	Common mode input capacitance	$f = 10\text{ kHz}$, P package $T_A = 25^\circ\text{C}$			8		pF
Z_o	Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$ $T_A = 25^\circ\text{C}$			220		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = -5\text{ V}$ to 2.7 V $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25^\circ\text{C}$	75	80		dB
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	75			

(1) The full temperature range is -40°C to $+125^\circ\text{C}$.

(2) Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6.9 TLV970x Operating Characteristics: $V_{DD\pm} = \pm 5\text{ V}$

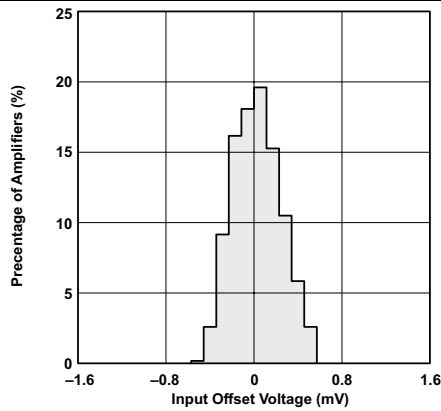
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP	MAX	UNIT
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$ $V_{IC} = V_{DD} / 2$ (no load)	$T_A = 25^\circ\text{C}$	80	95		dB
			$T_A = -40^\circ\text{C to }+125^\circ\text{C}$	80			
I_{DD}	Supply current	$V_O = 2.5\text{ V}$ (no load)	$T_A = 25^\circ\text{C}$		425	500	μA
			$T_A = -40^\circ\text{C to }+125^\circ\text{C}$			500	
SR	Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$ $C_L = 100\text{ pF}$ $R_L = 50\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	0.35	0.55		$\text{V}/\mu\text{s}$
			$T_A = -40^\circ\text{C to }+125^\circ\text{C}$	0.25			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$, $T_A = 25^\circ\text{C}$			43		$\text{nV} / \sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$, $T_A = 25^\circ\text{C}$			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$, $T_A = 25^\circ\text{C}$			0.8		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$, $T_A = 25^\circ\text{C}$			1.3		
I_n	Equivalent input noise current	$T_A = 25^\circ\text{C}$			0.6		$\text{fA}/\sqrt{\text{Hz}}$
	Total harmonic distortion plus noise (THD + N)	$V_O = \pm 2.3\text{ V}$ $R_L = 50\text{ k}\Omega$ $f = 20\text{ kHz}$	$A_V = 1$		0.018%		
			$A_V = 10$		0.027%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$, $R_L = 50\text{ k}\Omega$, $T_A = 25^\circ\text{C}$			0.73		MHz
B_{OM}	Maximum output swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$, $A_V = 1$, $C_L = 100\text{ pF}$			85		kHz
t_s	Settling time	$A_V = -1$ $-2.3\text{-V to }2.3\text{-V step}$ $R_L = 50\text{ k}\Omega$ $C_L = 100\text{ pF}$ $T_A = 25^\circ\text{C}$	To 0.1%		7.5		μs
			To 0.01%		17		
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_A = 25^\circ\text{C}$			57°		
	Gain margin				11		dB

(1) The full temperature range is -40°C to $+125^\circ\text{C}$.

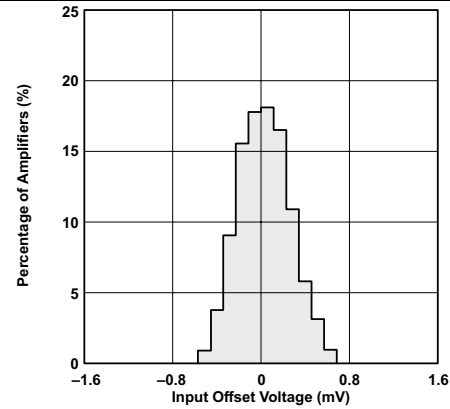
6.10 Typical Characteristics

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



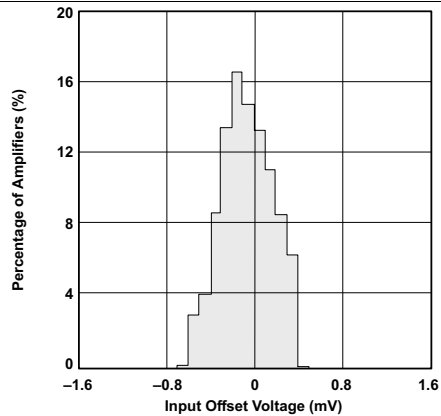
1274 amplifiers
from 2 wafer lots $V_{DD\pm} = \pm 2.5\text{ V}$ $T_A = 25^\circ\text{C}$

Figure 1. Distribution of TLV9702 Input Offset Voltage



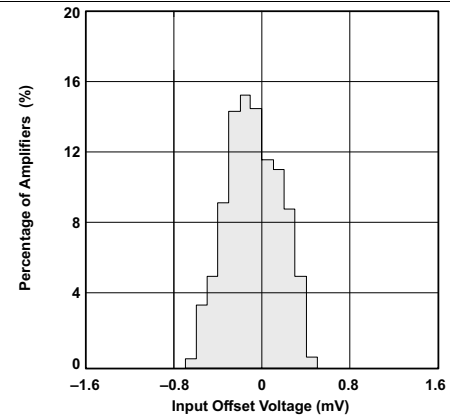
1274 amplifiers
from 2 wafer lots $V_{DD\pm} = \pm 5\text{ V}$ $T_A = 25^\circ\text{C}$

Figure 2. Distribution of TLV9702 Input Offset Voltage



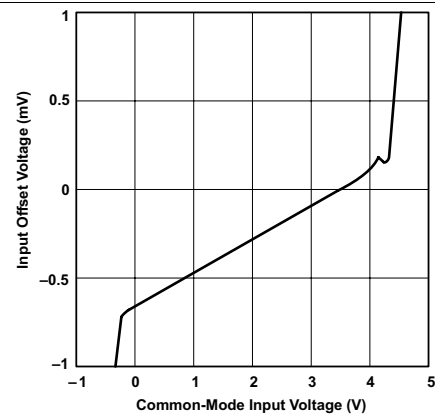
2272 amplifiers
from 2 wafer lots $V_{DD\pm} = \pm 5\text{ V}$ $T_A = 25^\circ\text{C}$

Figure 3. Distribution of TLV9704 Input Offset Voltage



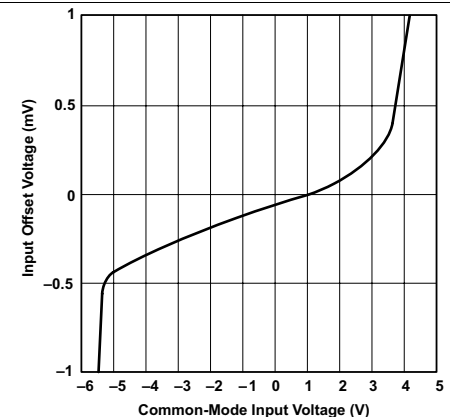
2272 amplifiers
from 2 wafer lots $V_{DD\pm} = \pm 5\text{ V}$ $T_A = 25^\circ\text{C}$

Figure 4. Distribution of TLV9704 Input Offset Voltage



$V_{DD} = 5\text{ V}$ $R_S = 50\ \Omega$ $T_A = 25^\circ\text{C}$

Figure 5. Input Offset Voltage vs Common-Mode Input Voltage

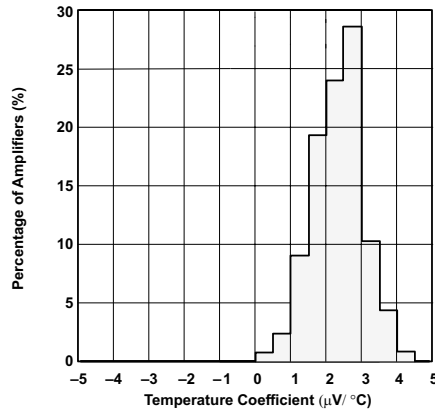


$V_{DD\pm} = \pm 5\text{ V}$ $R_S = 50\ \Omega$ $T_A = 25^\circ\text{C}$

Figure 6. Input Offset Voltage vs Common-Mode Input Voltage

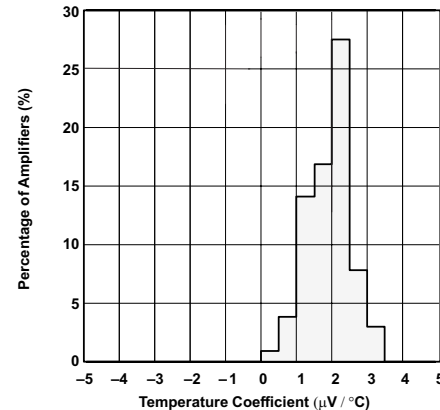
Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



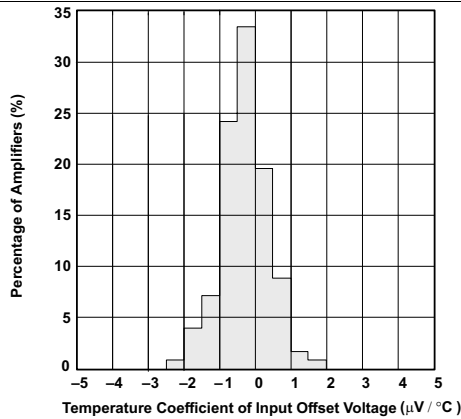
128 amplifiers from 2 wafer lots, $V_{DD\pm} = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ to 125°C , P package only

Figure 7. Distribution of TLV9702 Input Offset Voltage Temperature Coefficient



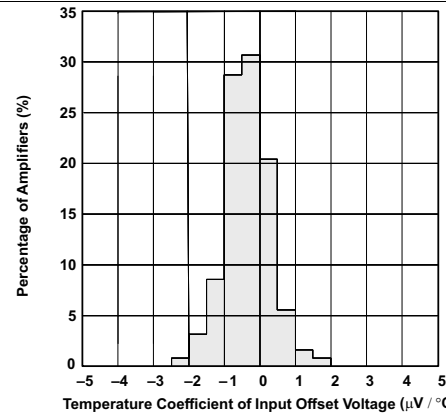
128 amplifiers from 2 wafer lots, $V_{DD\pm} = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ to 125°C , P package only

Figure 8. Distribution of TLV9702 Input Offset Voltage Temperature Coefficient



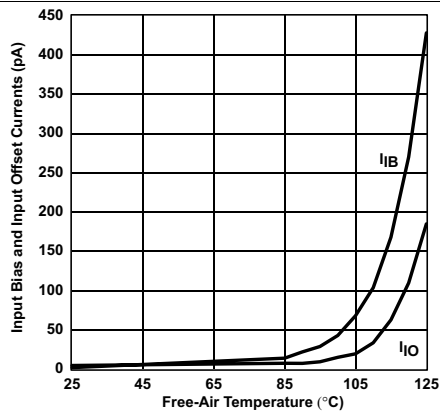
128 amplifiers from 2 wafer lots, $V_{DD\pm} = \pm 2.5\text{ V}$, $T_A = 25^\circ\text{C}$ to 125°C , P package only

Figure 9. Distribution of TLV9704 Input Offset Voltage Temperature Coefficient



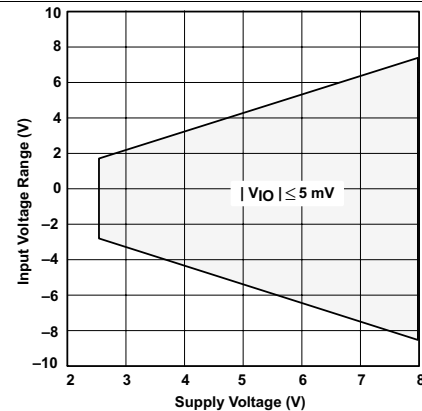
128 amplifiers from 2 wafer lots, $V_{DD\pm} = \pm 2.5\text{ V}$, $T_A = 25^\circ\text{C}$ to 125°C , N package only

Figure 10. Distribution of TLV9704 Input Offset Voltage Temperature Coefficient



$V_O = 0$, $V_{IC} = 0\text{ V}$, $V_{DD\pm} = \pm 2.5\text{ V}$, $R_S = 50\ \Omega$

Figure 11. Input Bias and Input Offset Currents vs Free-Air Temperature



$R_S = 50\ \Omega$

$T_A = 25^\circ\text{C}$

Figure 12. Input Voltage Range vs Supply Voltage

Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

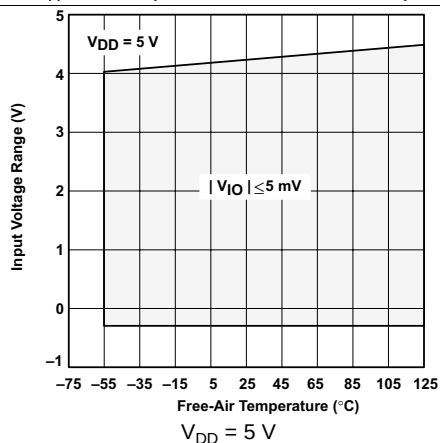


Figure 13. Input Voltage Range vs Free-Air Temperature

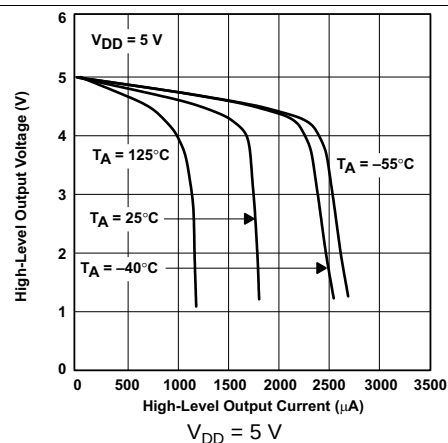


Figure 14. High-Level Output Voltage vs High-Level Output Current

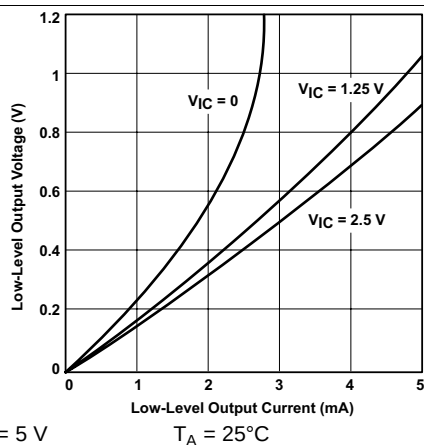


Figure 15. Low-Level Output Voltage vs Low-Level Output Current

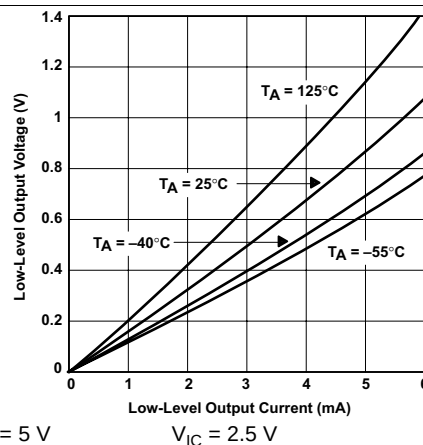


Figure 16. Low-Level Output Voltage vs Low-Level Output Current

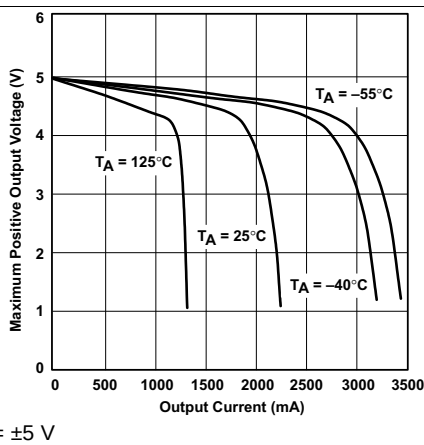


Figure 17. Maximum Positive Output Voltage vs Output Current

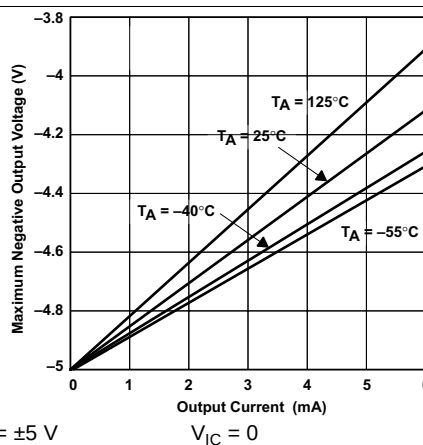


Figure 18. Maximum Negative Output Voltage vs Output Current

Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

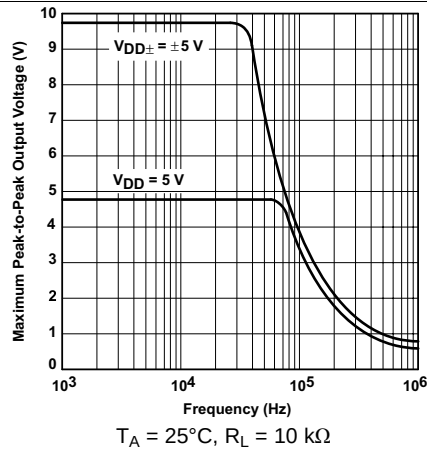


Figure 19. Maximum Peak-to-Peak Output Voltage vs Frequency

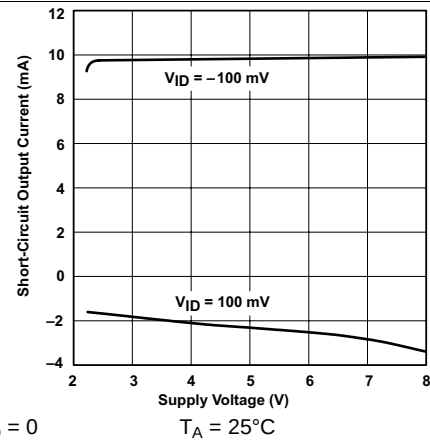


Figure 20. Short-Circuit Output Current vs Supply Voltage

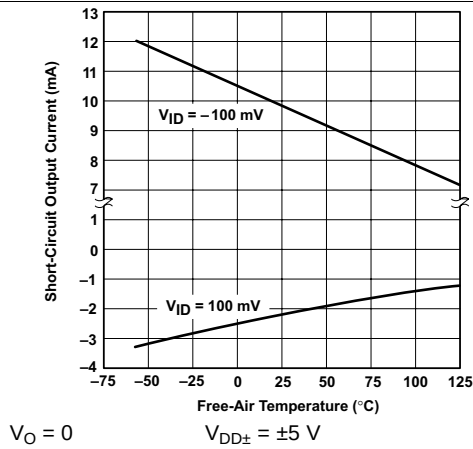


Figure 21. Short-Circuit Output Current vs Free-Air Temperature

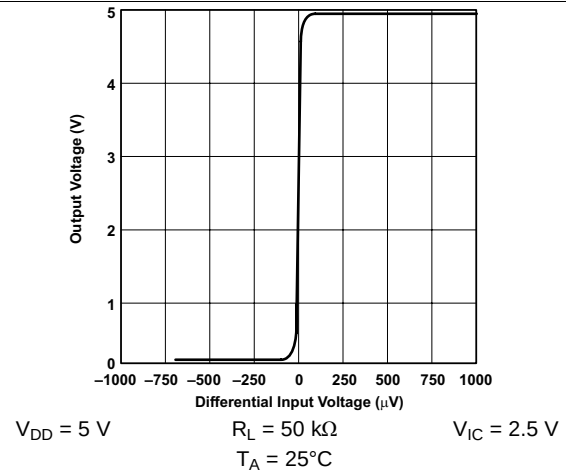


Figure 22. Output Voltage vs Differential Input Voltage

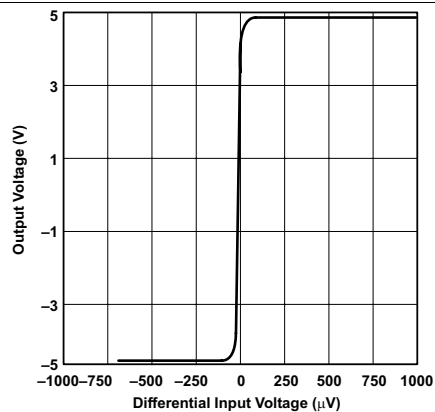


Figure 23. Output Voltage vs Differential Input Voltage

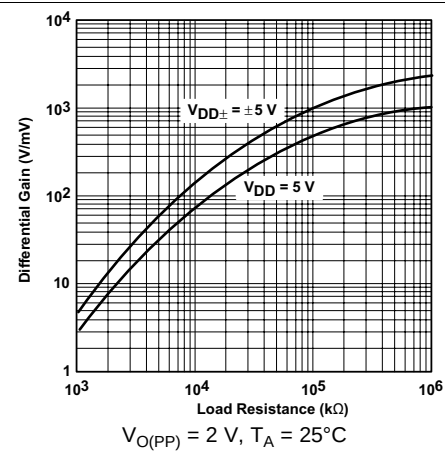


Figure 24. Differential Gain vs Load Resistance

Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

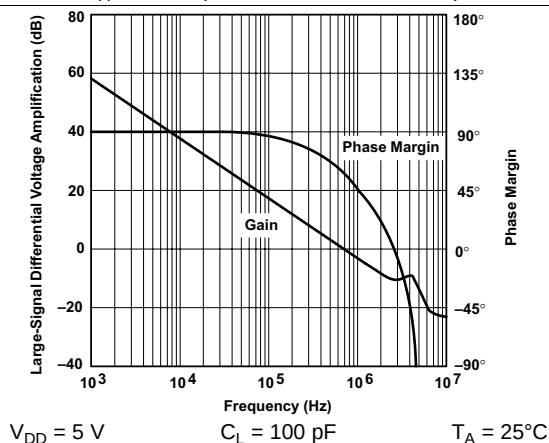


Figure 25. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

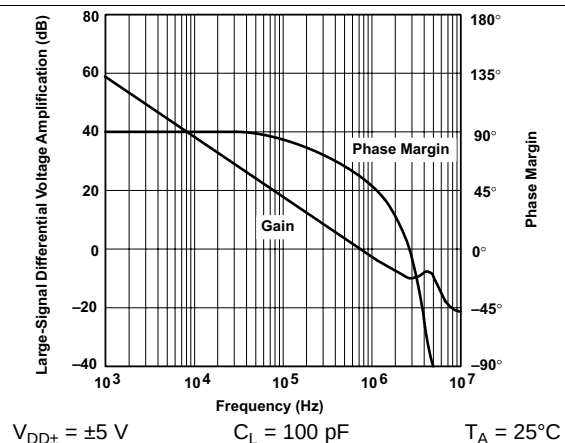


Figure 26. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

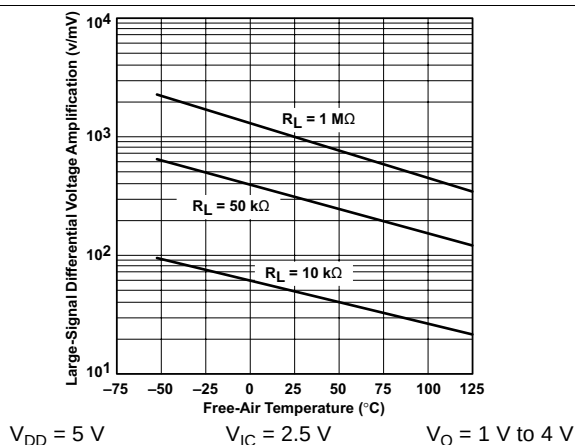


Figure 27. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

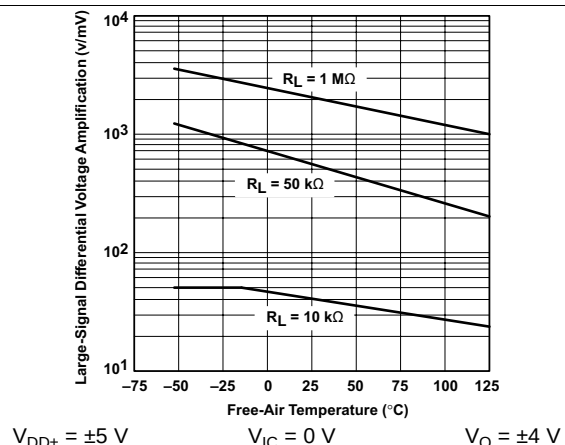


Figure 28. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

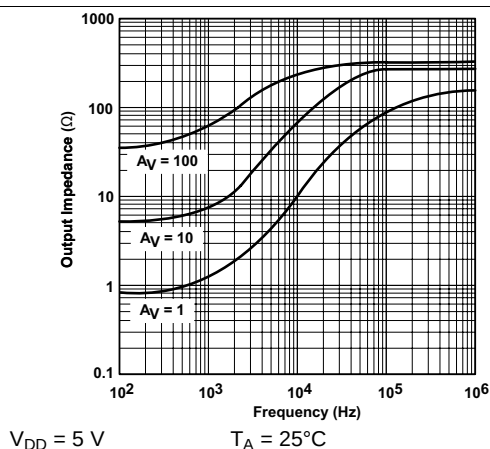


Figure 29. Output Impedance vs Frequency

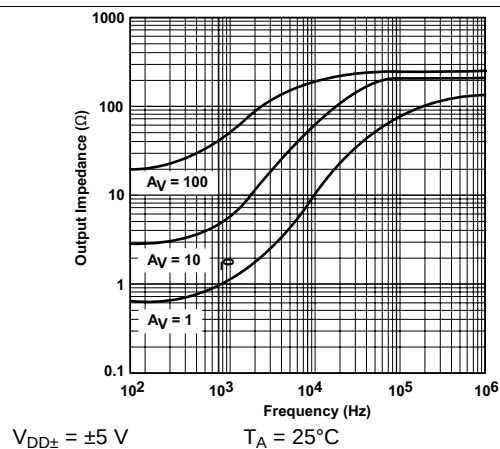


Figure 30. Output Impedance vs Frequency

Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

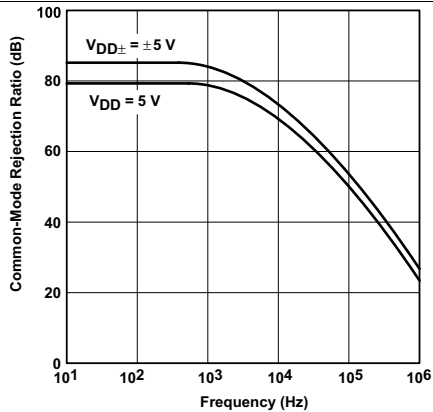


Figure 31. Common-Mode Rejection Ratio vs Frequency

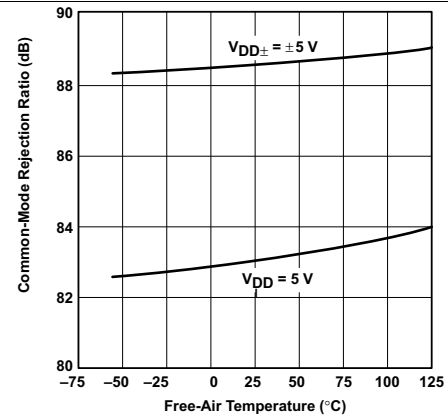


Figure 32. Common-Mode Rejection Ratio vs Free-Air Temperature

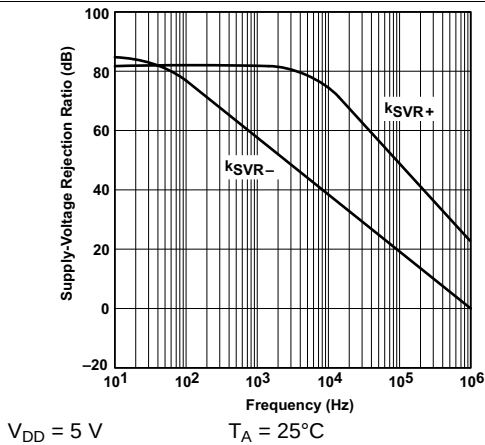


Figure 33. Supply-Voltage Rejection Ratio vs Frequency

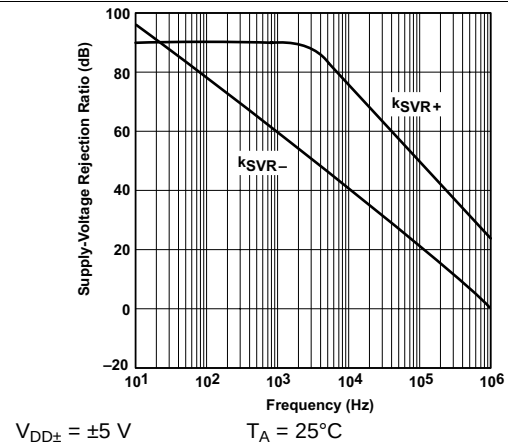


Figure 34. Supply-Voltage Rejection Ratio vs Frequency

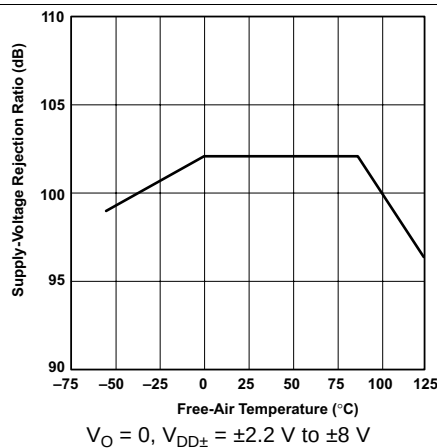


Figure 35. Supply-Voltage Rejection Ratio vs Free-Air Temperature

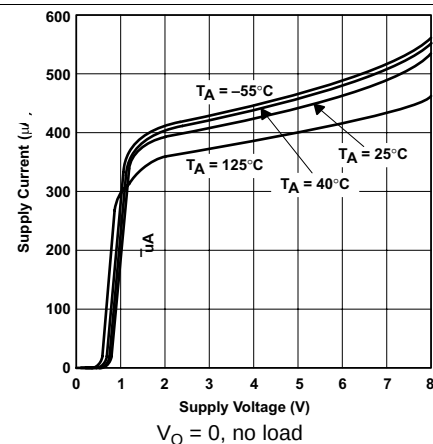


Figure 36. TLV9702 Supply Current vs Supply Voltage

Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

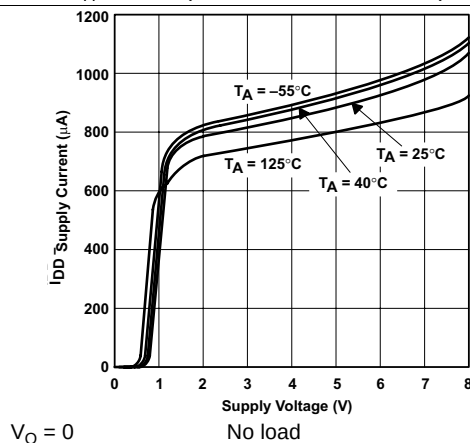


Figure 37. TLV9704 Supply Current vs Supply Voltage

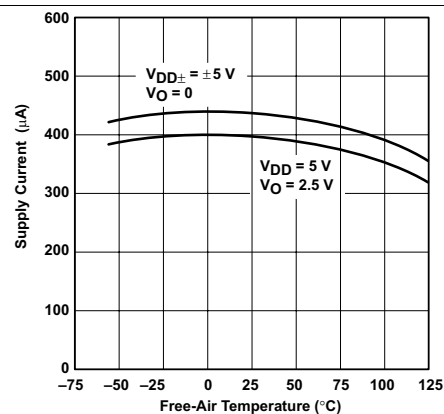


Figure 38. TLV9702 Supply Current vs Free-Air Temperature

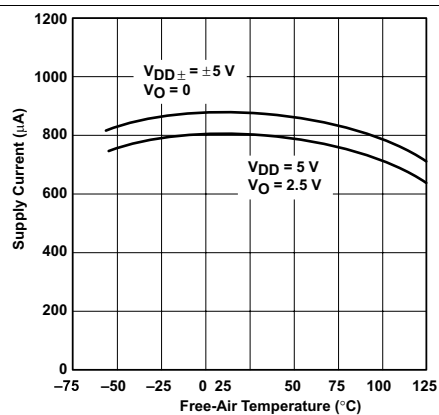


Figure 39. TLV9704 Supply Current vs Free-Air Temperature

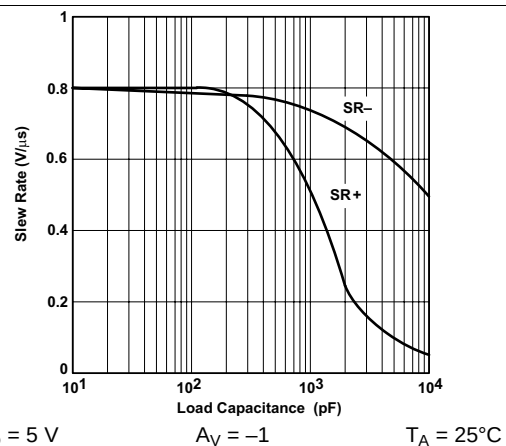


Figure 40. Slew Rate vs Load Capacitance

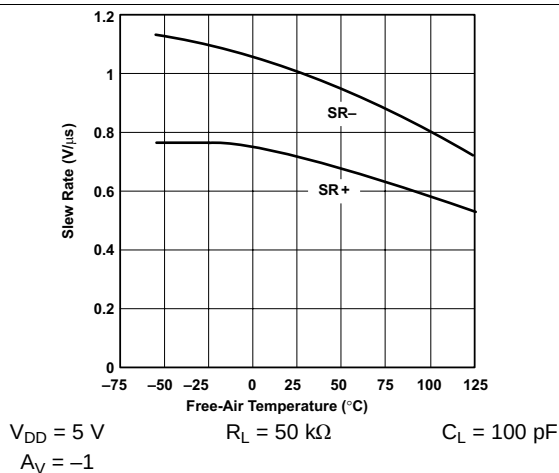


Figure 41. Slew Rate vs Free-Air Temperature

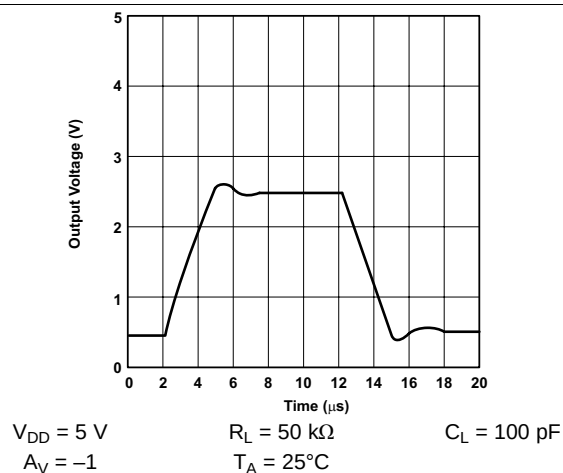
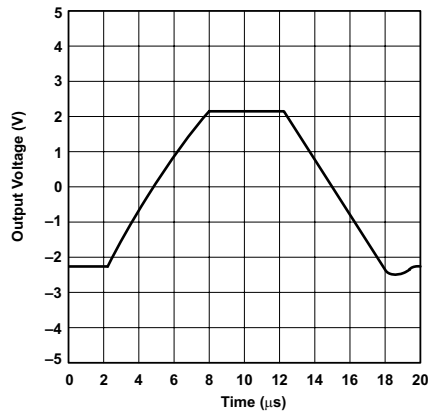


Figure 42. Inverting Large-Signal Pulse Response

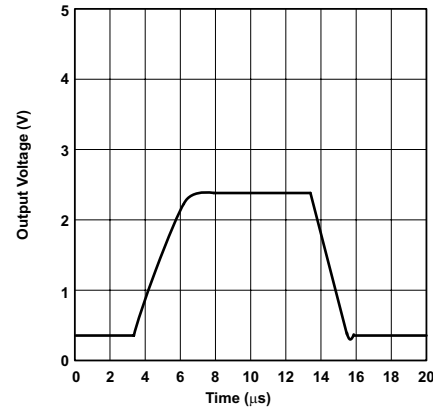
Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



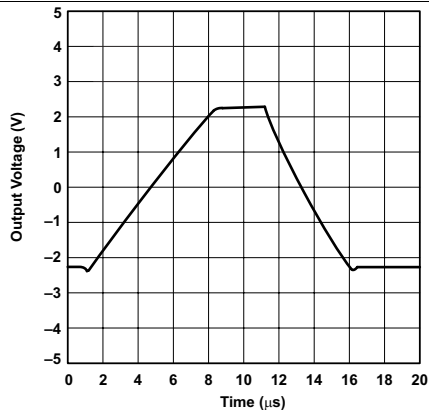
$V_{DD} = 5\text{ V}$ $R_L = 50\text{ k}\Omega$ $C_L = 100\text{ pF}$
 $A_V = -1$ $T_A = 25^\circ\text{C}$

Figure 43. Inverting Large-Signal Pulse Response



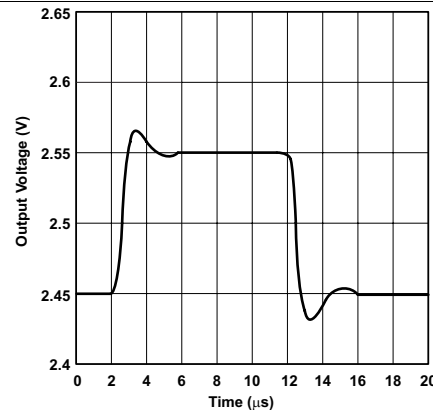
$V_{DD} = 5\text{ V}$ $R_L = 50\text{ k}\Omega$ $C_L = 100\text{ pF}$
 $A_V = 1$ $T_A = 25^\circ\text{C}$

Figure 44. Voltage-Follower Large-Signal Pulse Response



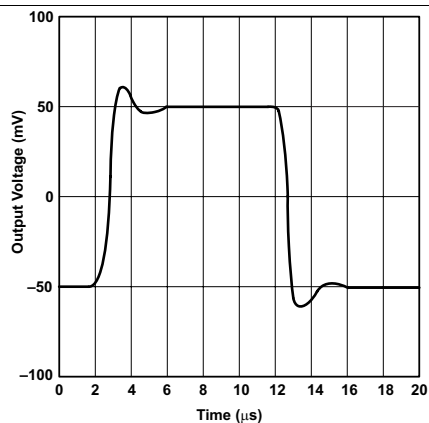
$V_{DD\pm} = \pm 5\text{ V}$ $R_L = 50\text{ k}\Omega$ $C_L = 100\text{ pF}$
 $A_V = 1$ $T_A = 25^\circ\text{C}$

Figure 45. Voltage-Follower Large-Signal Pulse Response



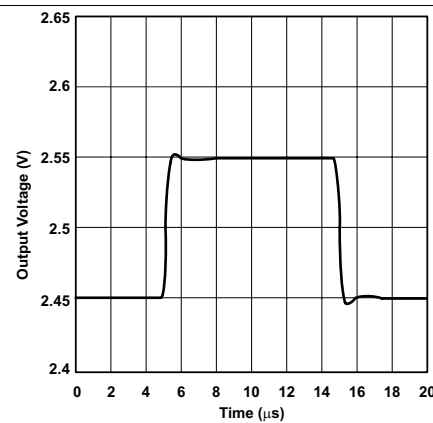
$V_{DD} = 5\text{ V}$ $R_L = 50\text{ k}\Omega$ $C_L = 100\text{ pF}$
 $A_V = -1$ $T_A = 25^\circ\text{C}$

Figure 46. Inverting Small-Signal Pulse Response



$V_{DD\pm} = \pm 5\text{ V}$ $R_L = 50\text{ k}\Omega$ $C_L = 100\text{ pF}$
 $A_V = -1$ $T_A = 25^\circ\text{C}$

Figure 47. Inverting Small-Signal Pulse Response

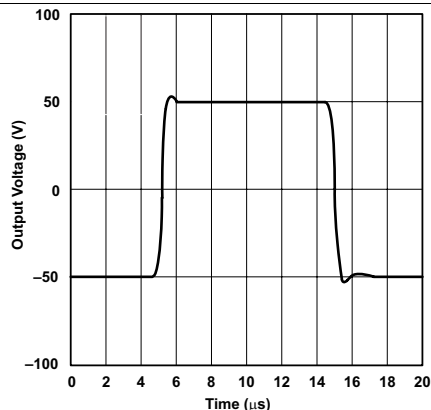


$V_{DD} = 5\text{ V}$ $R_L = 50\text{ k}\Omega$ $C_L = 100\text{ pF}$
 $A_V = 1$ $T_A = 25^\circ\text{C}$

Figure 48. Voltage-Follower Small-Signal Pulse Response

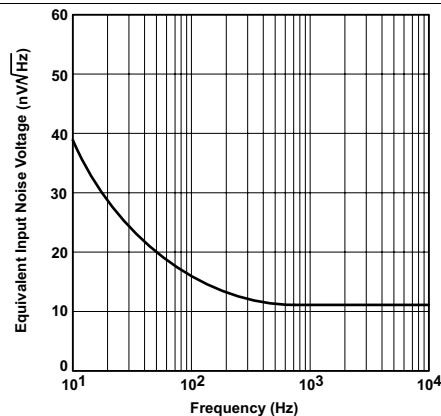
Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)



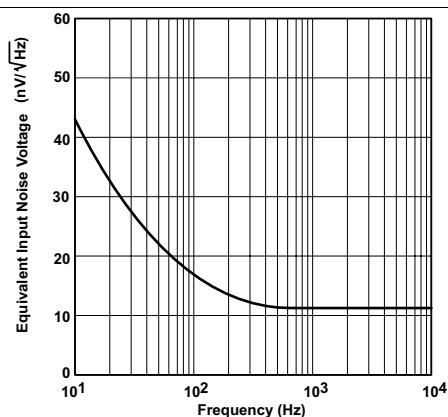
$V_{DD\pm} = \pm 5\text{ V}$, $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = 1$, $T_A = 25^\circ\text{C}$

Figure 49. Voltage-Follower Small-Signal Pulse Response



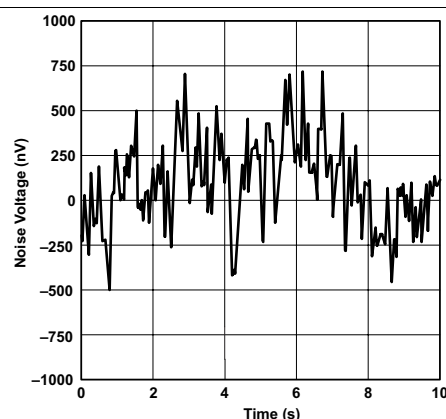
$V_{DD} = 5\text{ V}$, $R_S = 20\text{ }\Omega$, $T_A = 25^\circ\text{C}$

Figure 50. Equivalent Input Noise Voltage vs Frequency



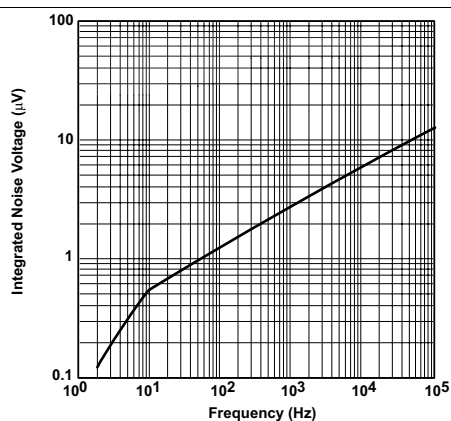
$V_{DD\pm} = \pm 5\text{ V}$, $R_S = 20\text{ }\Omega$, $T_A = 25^\circ\text{C}$

Figure 51. Equivalent Input Noise Voltage vs Frequency



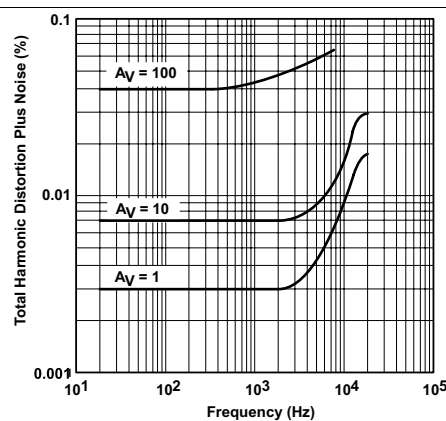
$V_{DD} = 5\text{ V}$, $f = 0.1\text{ Hz to }10\text{ Hz}$, $T_A = 25^\circ\text{C}$

Figure 52. Equivalent Input Noise Voltage Over a 10-Second Period



Calculated using ideal pass-band filter
Low frequency = 1 Hz
 $T_A = 25^\circ\text{C}$

Figure 53. Integrated Noise Voltage vs Frequency



$V_{DD} = 5\text{ V}$, $R_L = 50\text{ k}\Omega$, $T_A = 25^\circ\text{C}$

Figure 54. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

at $V_S = \pm 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

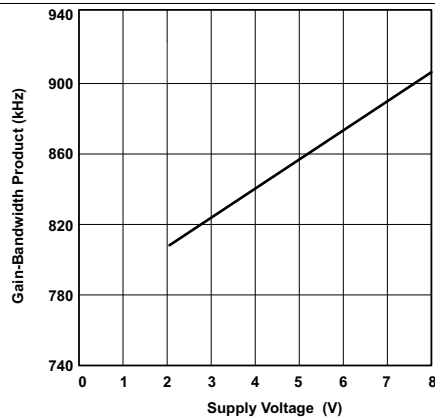


Figure 55. Gain-Bandwidth Product vs Supply Voltage

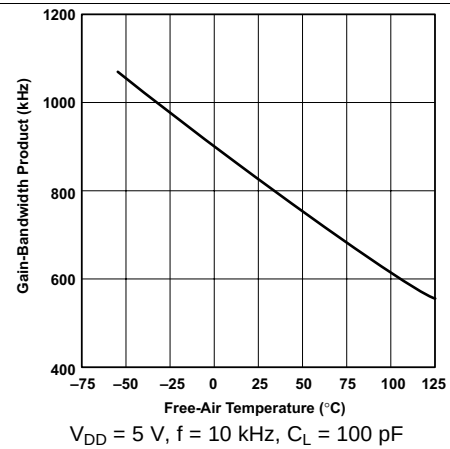


Figure 56. Gain-Bandwidth Product vs Free-Air Temperature

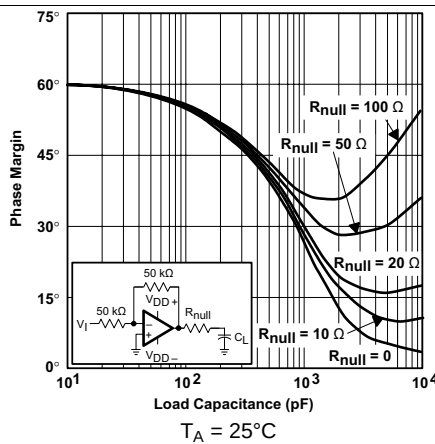


Figure 57. Phase Margin vs Load Capacitance

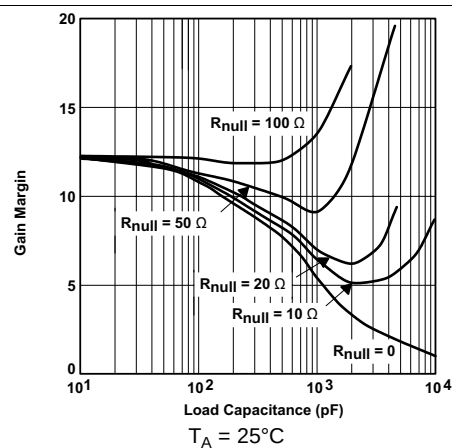


Figure 58. Gain Margin vs Load Capacitance

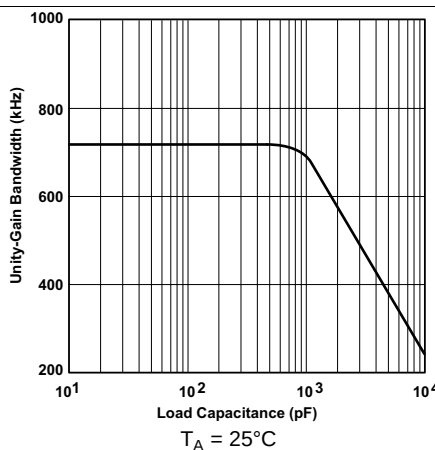


Figure 59. Unity-Gain Bandwidth vs Load Capacitance

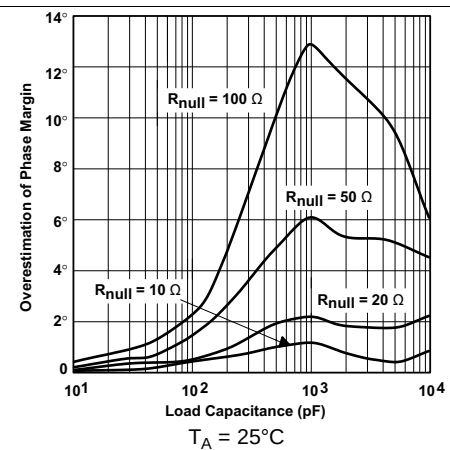


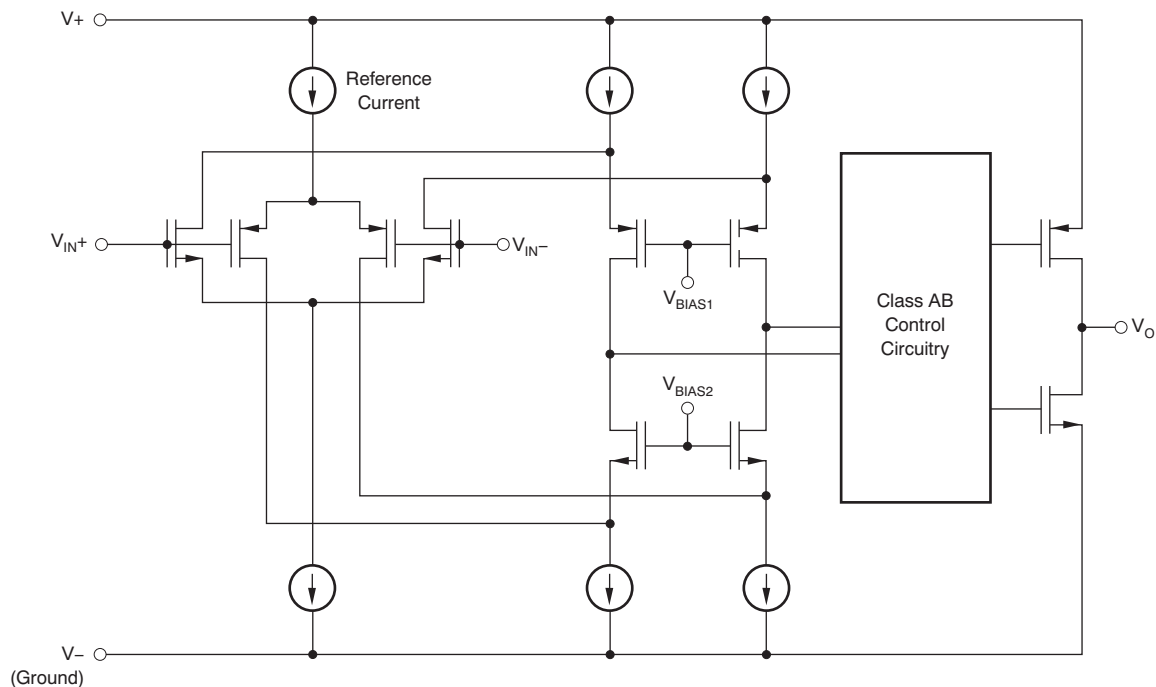
Figure 60. Overestimation of Phase Margin vs Load Capacitance

7 Detailed Description

7.1 Overview

The TLV970x single-supply CMOS operational amplifiers provide rail-to-rail input and output capability with 3-MHz bandwidth. Consuming 550 μ A, the TLV970x is designed for portable and battery-operated applications. The maximum recommended supply voltage is 16 V, which allows the devices to operate from ($\pm$ 8-V supplies down to $\pm$ 1.35 V) a variety of rechargeable cells. The recommended supply voltage is from 2.7 V to 16 V ($\pm$ 1.35 V to $\pm$ 8 V), which allows the devices to operate from a variety of rechargeable cells. The rail-to-rail inputs with high input impedance make the TLV970x an option for sensor signal-conditioning applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Driving Large Capacitive Loads

The TLV970x is designed to drive larger capacitive loads than most CMOS operational amplifiers. [Figure 57](#) and [Figure 58](#) show that the devices drive loads greater than 400 pF, while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{NULL}) at the output of the device (see [Figure 61](#)) improves the gain and phase margins when driving large capacitive loads. [Figure 57](#) and [Figure 58](#) show the effects of adding series resistances of 10 Ω , 20 Ω , 50 Ω , and 100 Ω . The addition of this series resistor has two effects: the resistor adds a zero to the transfer function, and reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, use [Equation 1](#).

$$\Delta\theta_{m1} = \tan^{-1}(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L)$$

where

- $\Delta\theta_{m1}$ = improvement in phase margin
- UGBW = unity-gain bandwidth frequency
- R_{null} = output series resistance

Feature Description (continued)

- C_L = load capacitance (1)

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 59). To use Equation 1, UGBW must be approximated from Figure 59.

Using Equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 60. The overestimation is caused by the decrease in the frequency of the pole associated with the load, which provides additional phase shift and reducing the overall improvement in phase margin. The factor calculated in Equation 2 reduces the pole associated with the load.

$$F = 1 / (1 + g_m \times R_{null})$$

where

- F = factor reducing frequency of pole
- g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
- R_{null} = output series resistance (2)

For the TLV970x, the pole associated with the load is typically 7 MHz with a 100-pF load capacitance. This value varies inversely with C_L : at $C_L = 10$ pF, use 70 MHz; at $C_L = 1000$ pF, use 700 kHz, and so forth.

Reducing the pole associated with the load introduces phase shift, which reduces phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (see Equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of Equation 1 to better approximate the improvement in phase margin.

$$\Delta\theta_{m2} = \tan^{-1} [UGBW / (F \times P_2)] - \tan^{-1} (UGBW / P_2)$$

where

- $\Delta\theta_{m2}$ = reduction in phase margin
- UGBW = unity-gain bandwidth frequency
- F = factor from Equation 2
- P_2 = unadjusted pole (70 MHz at 10 pF, 7 MHz at 100 pF, and so forth.) (3)

Using these equations with Figure 59 and Figure 60 enables the designer to select the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

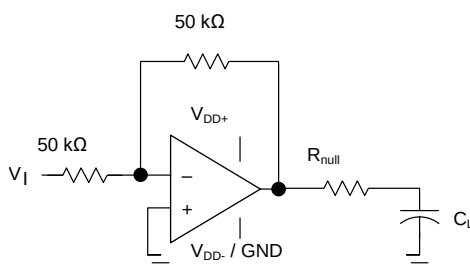


Figure 61. Series-Resistance Circuit

7.4 Device Functional Modes

The TLV970x devices have a single functional mode. These devices are operable as long as the power-supply voltage is between 2.7 V (± 1.35 V) and 16 V (± 8 V).

8 Application and Implementation

NOTE

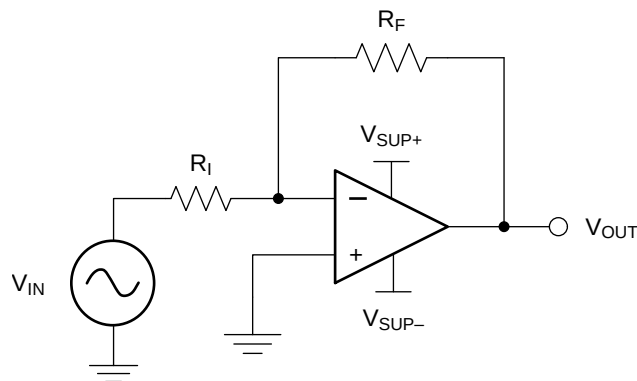
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When designing for low power, select system components carefully. To minimize current consumption, select large-value resistors. Any resistors react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations affect the stability of the overall system. Use of a feedback capacitor assures stability and limits overshoot or gain peaking.

8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in [Figure 62](#). An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier makes negative input voltages positive on the output. Select the input resistor (R_I) and the feedback resistor (R_F) to add amplification.



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Figure 62. Application Schematic

Macromodel information provided is derived using MicroSim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel (see G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974)) and subcircuit in [Figure 63](#) are generated using the TLV970x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

Typical Application (continued)

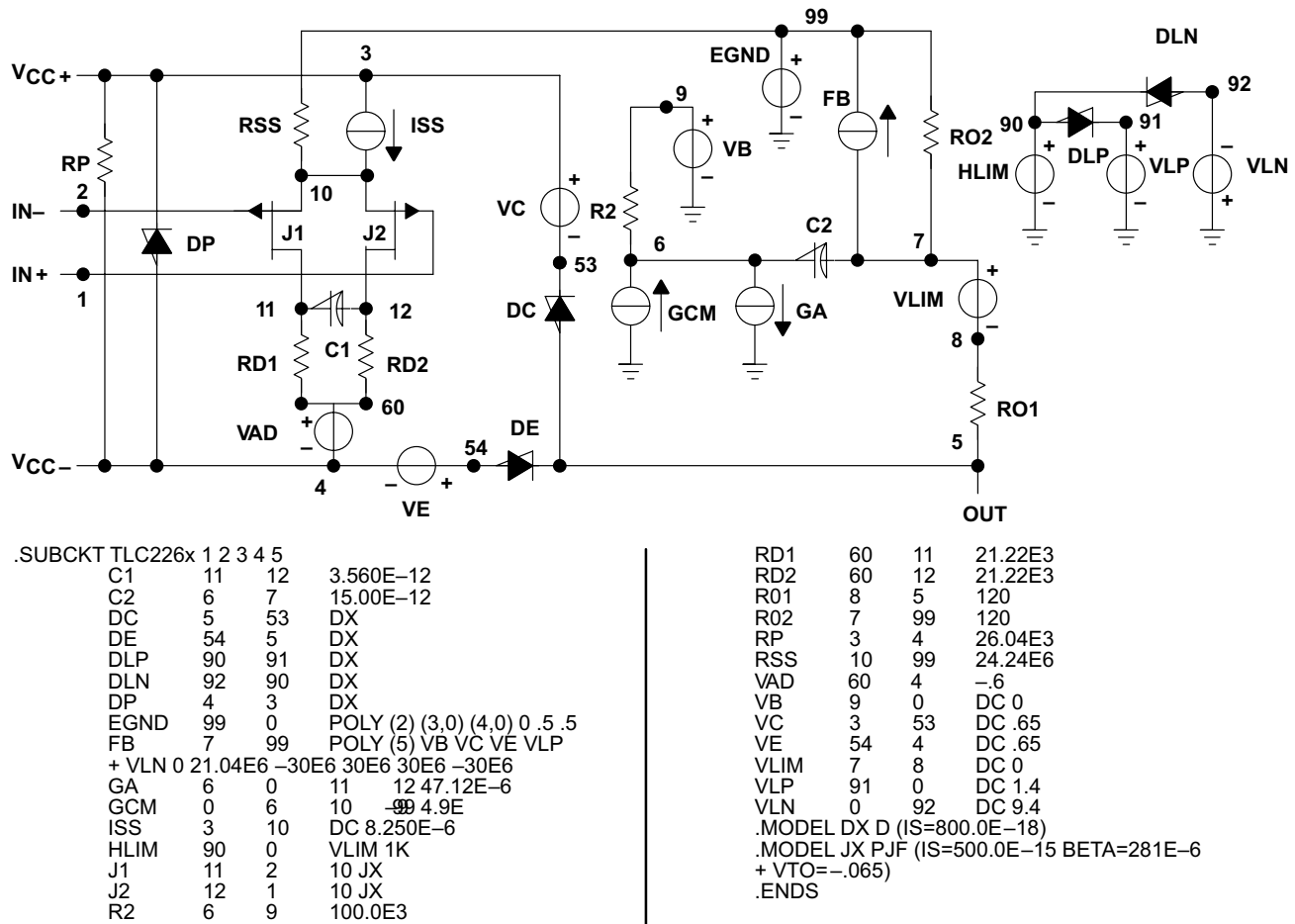


Figure 63. Boyle Macromodel and Subcircuit

8.2.1 Design Requirements

The selected supply voltage must be larger than the input voltage range and the desired output range. Consider the limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O). For example, this application scales a signal of ± 0.5 V (1 V) to ± 1.8 V (3.6 V). Setting the supply at ± 2.5 V is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 4](#) and [Equation 5](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (4)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (5)$$

When the desired gain is determined, choose a value for R_I or R_F . Choosing a value in the k Ω range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (100s of k Ω) draw the smallest current but generate the highest noise. Very small resistors (100s of Ω) generate low noise but draw high current. This example uses 10 k Ω for R_I , meaning 36 k Ω is used for R_F . These values are determined by [Equation 6](#):

Typical Application (continued)

$$A_V = -\frac{R_F}{R_I} \quad (6)$$

8.2.3 Application Curve

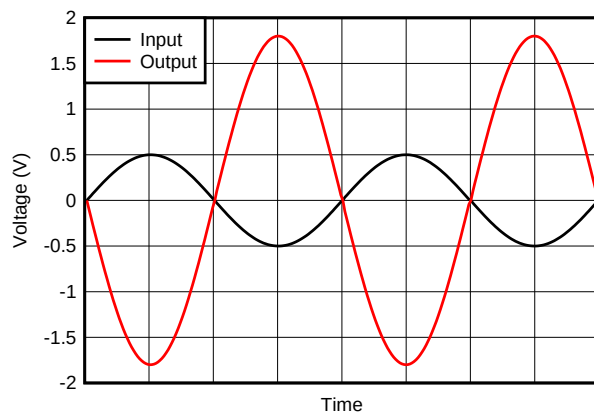


Figure 64. Inverting Amplifier Input and Output

9 Power Supply Recommendations

The TLV970x family is specified for operation from 2.7 V to 16 V (± 1.35 V to ± 8 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. The [Typical Characteristics](#) shows parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 16 V can permanently damage the device (see the table).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout](#).

10 Layout

10.1 Layout Guidelines

To achieve the levels of high performance of the TLV970x family, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes: TI highly recommends using a ground plane on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, remove the ground plane to minimize the stray capacitance.
- Proper power supply decoupling: Use a 6.8- μF tantalum capacitor in parallel with a 0.1- μF ceramic capacitor on each supply pin. It may be possible to share the tantalum among several amplifiers depending on the application, but always use a 0.1- μF ceramic capacitor on the supply pin of every amplifier. In addition, the 0.1- μF capacitor must be placed as close as possible to the supply pin. As this distance increases, the inductance in the connecting trace decreases the effectiveness of the capacitor. The designer must strive for distances of less than 0.1 inches between the device power pins and the ceramic capacitors.
- Sockets: Sockets can be used but are not recommended. The additional lead inductance in the socket pins can lead to stability problems. For the best implementation, solder surface mount packages directly to the printed circuit board.
- Short trace runs and compact part placements: To achieve optimum high performance, minimize stray series inductance. To achieve this, make the circuit layout as compact as possible, minimizing the length of all trace runs. Pay particular attention to the inverting input of the amplifier. The length of the inverting input must be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components: Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, which minimizes stray inductance and capacitance. If leaded components are used, TI recommends that the lead lengths be kept as short as possible.

10.2 Layout Example

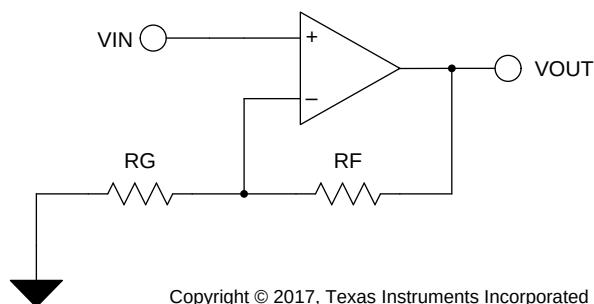


Figure 65. Schematic Representation

Layout Example (continued)

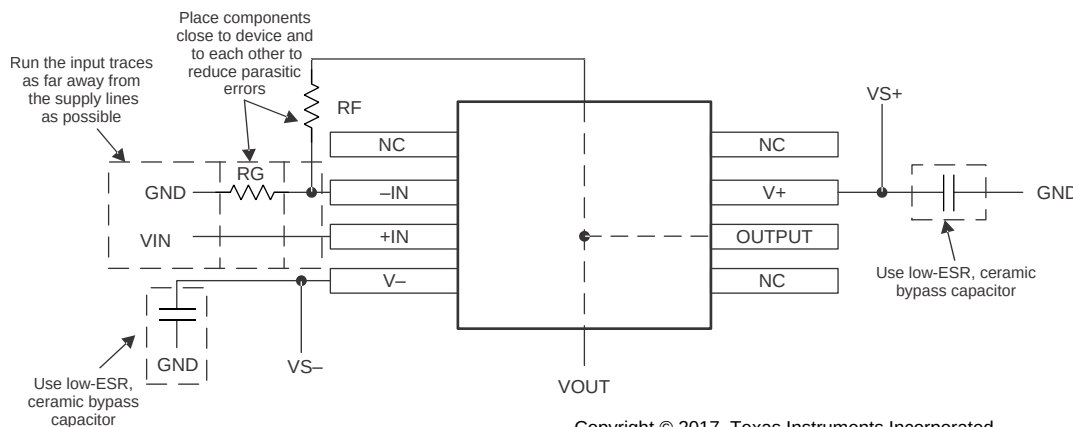


Figure 66. Operational Amplifier Board Layout for Noninverting Configuration

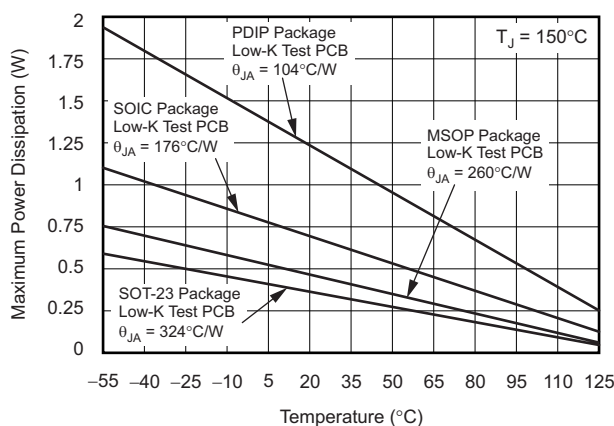
10.3 Power Dissipation Considerations

For a given θ_{JA} value, the maximum power dissipation is shown in Figure 67 and is calculated by Equation 7:

$$P_D = \left[\frac{T_{MAX} - T_A}{\theta_{JA}} \right]$$

where

- P_D = Maximum power dissipation of TLV970x (watts)
 - T_{MAX} = Absolute maximum junction temperature (150°C)
 - T_A = Free-ambient air temperature (°C)
 - $\theta_{JA} = \theta_{JC}$ (Thermal coefficient from junction to case) + θ_{CA} (Thermal coefficient from case to ambient air (°C/W))
- (7)



Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 67. Maximum Power Dissipation vs Free-Air Temperature

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV9702	Click here	Click here	Click here	Click here	Click here
TLV9704	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9702IDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9702	
TLV9704IDR	PREVIEW	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9704	
TLV9704IPWR	PREVIEW	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9704	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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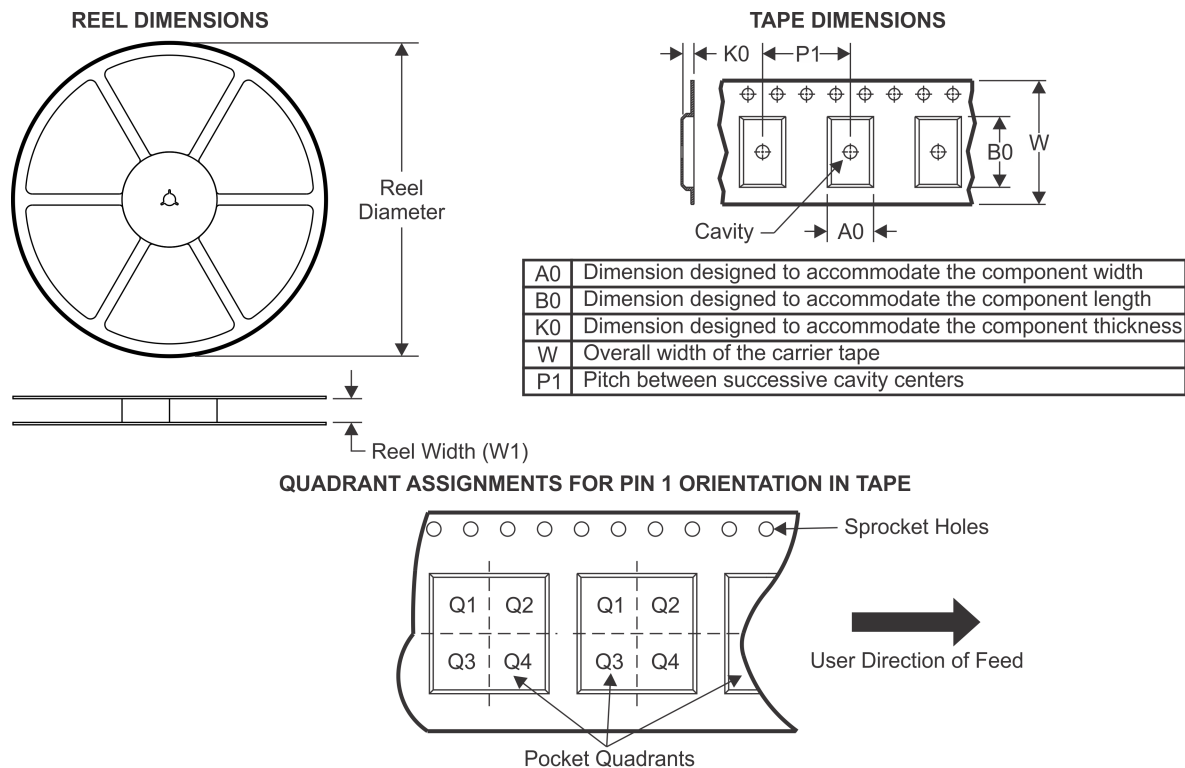


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PACKAGE OPTION ADDENDUM

31-Jan-2018

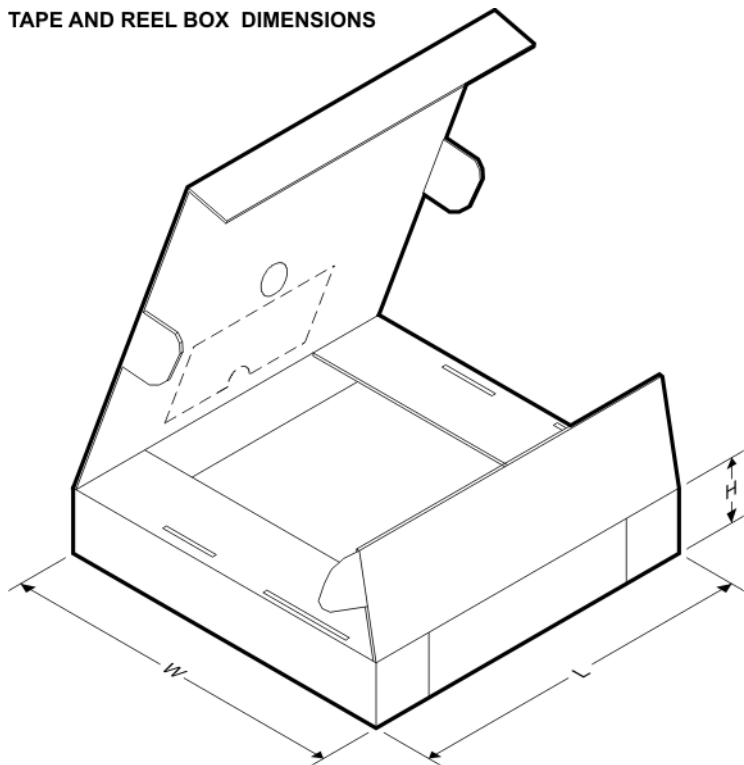
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9702IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9704IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9704IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

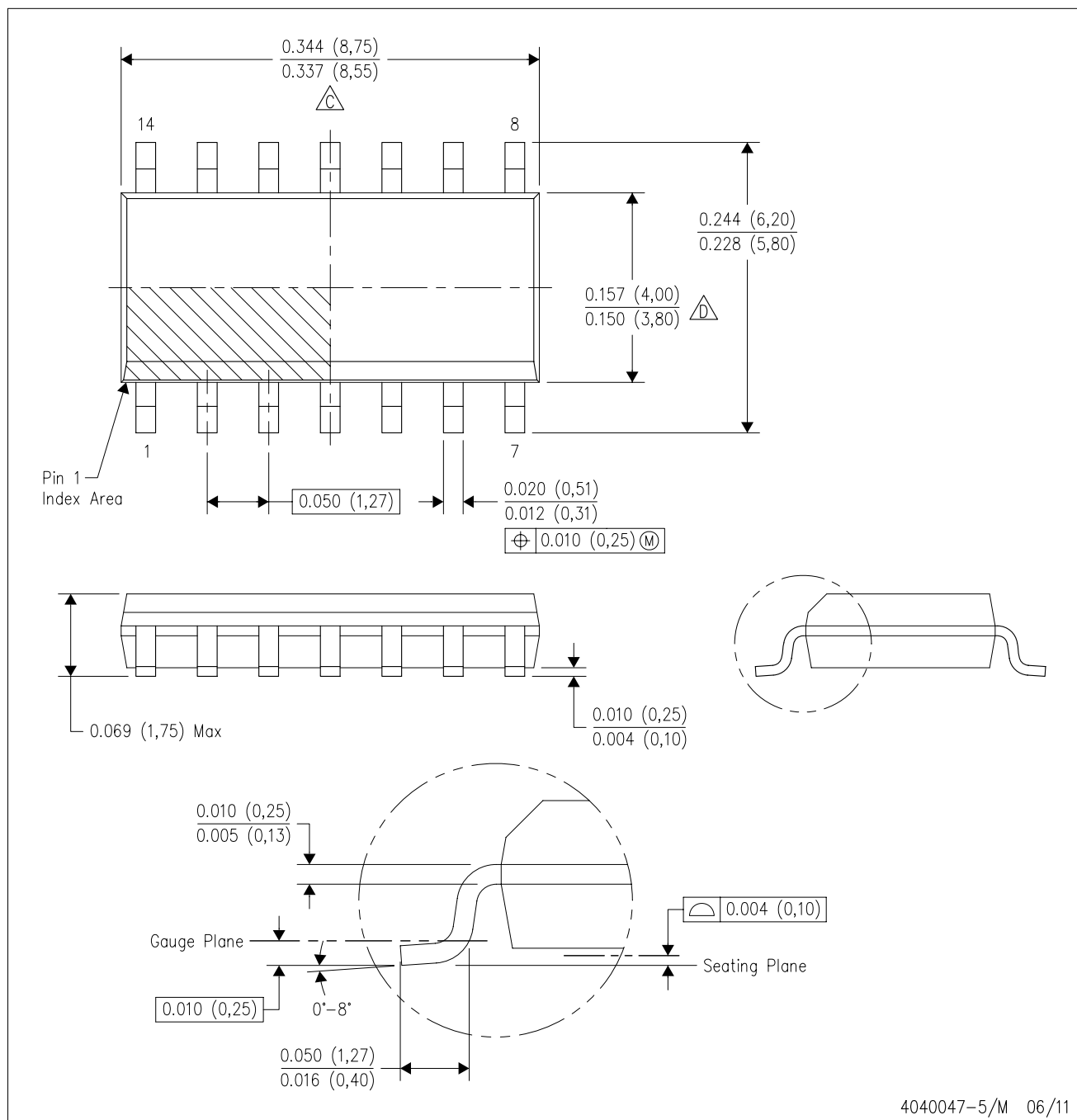


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9702IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV9704IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV9704IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

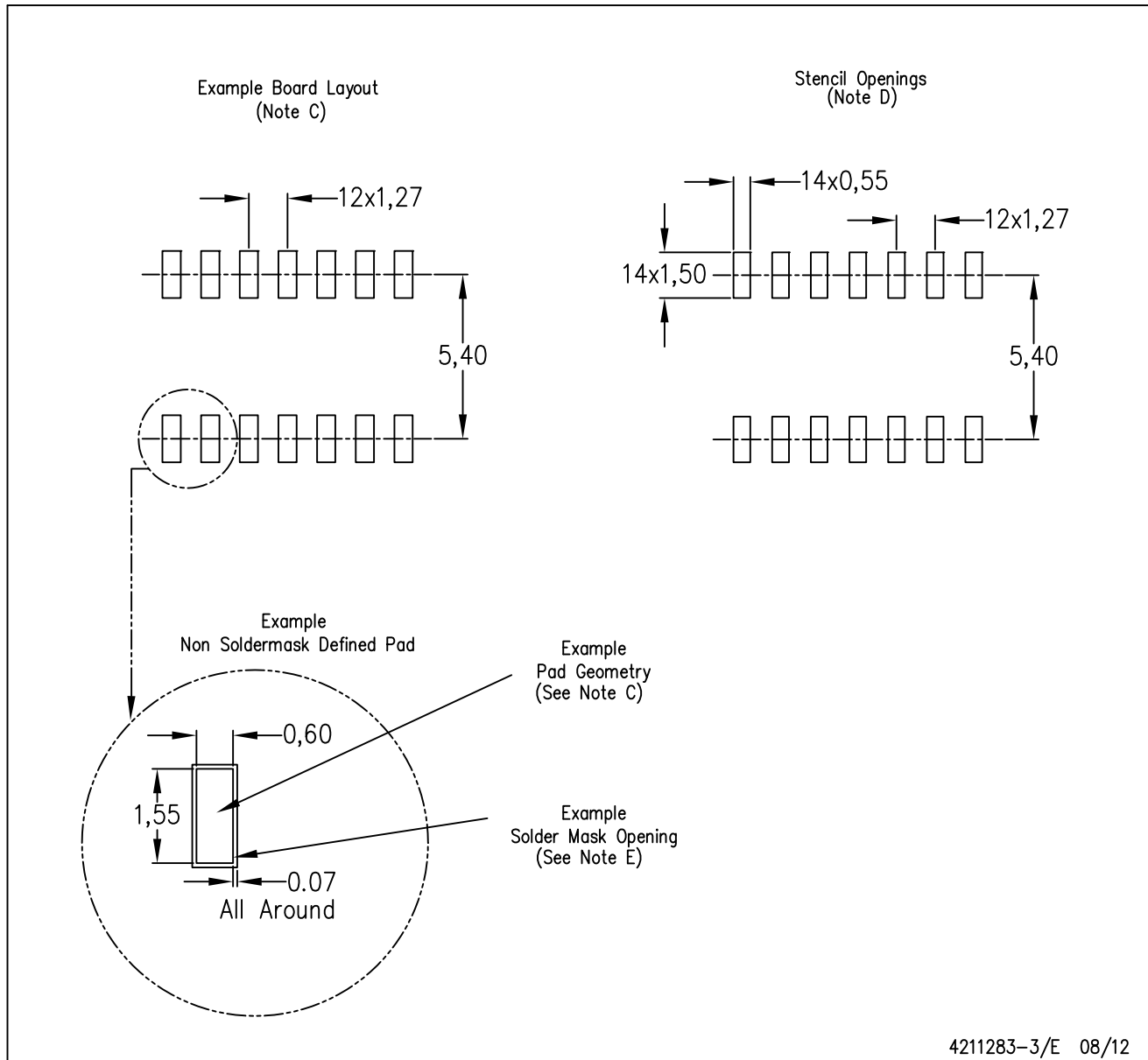


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

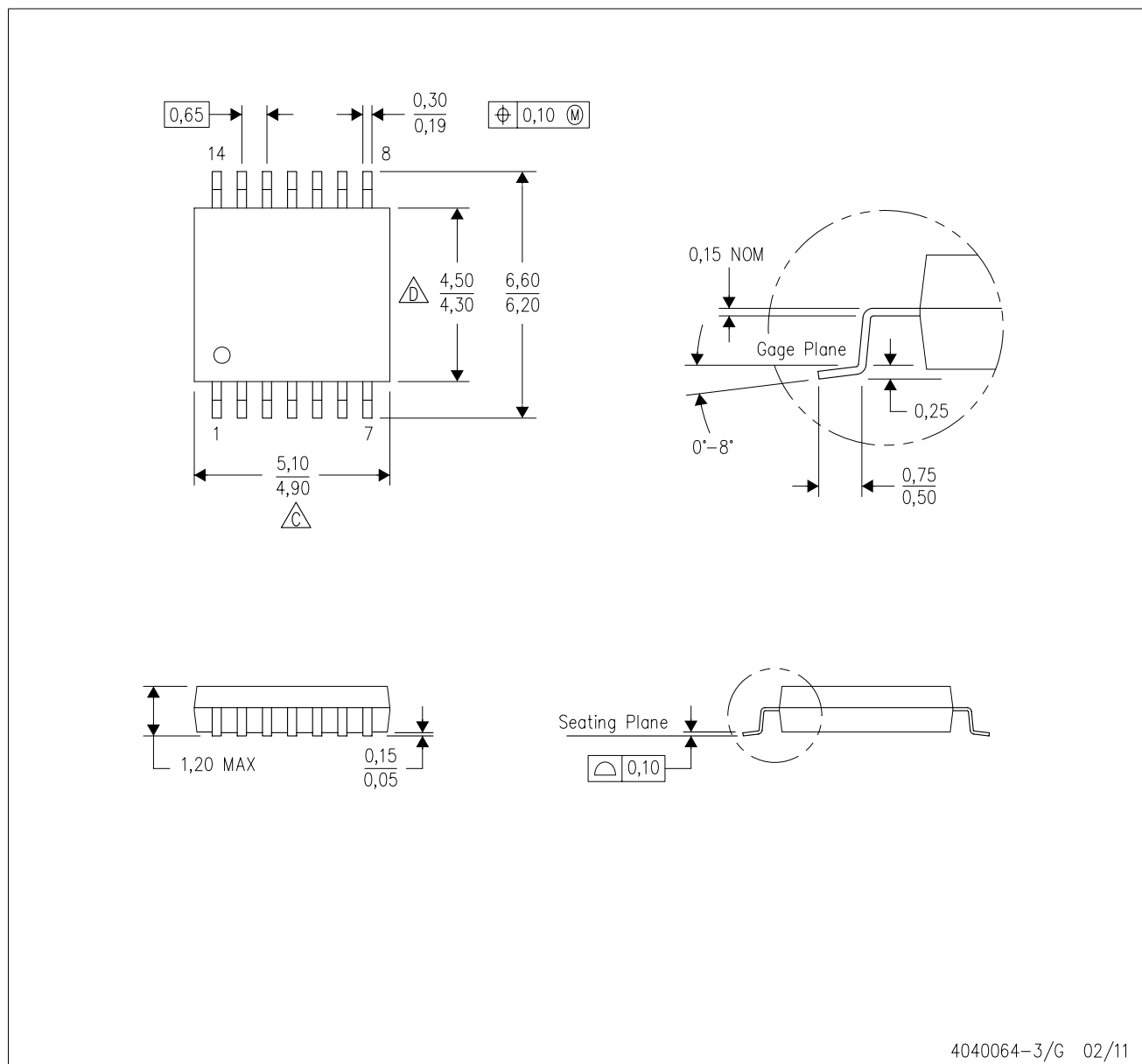
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

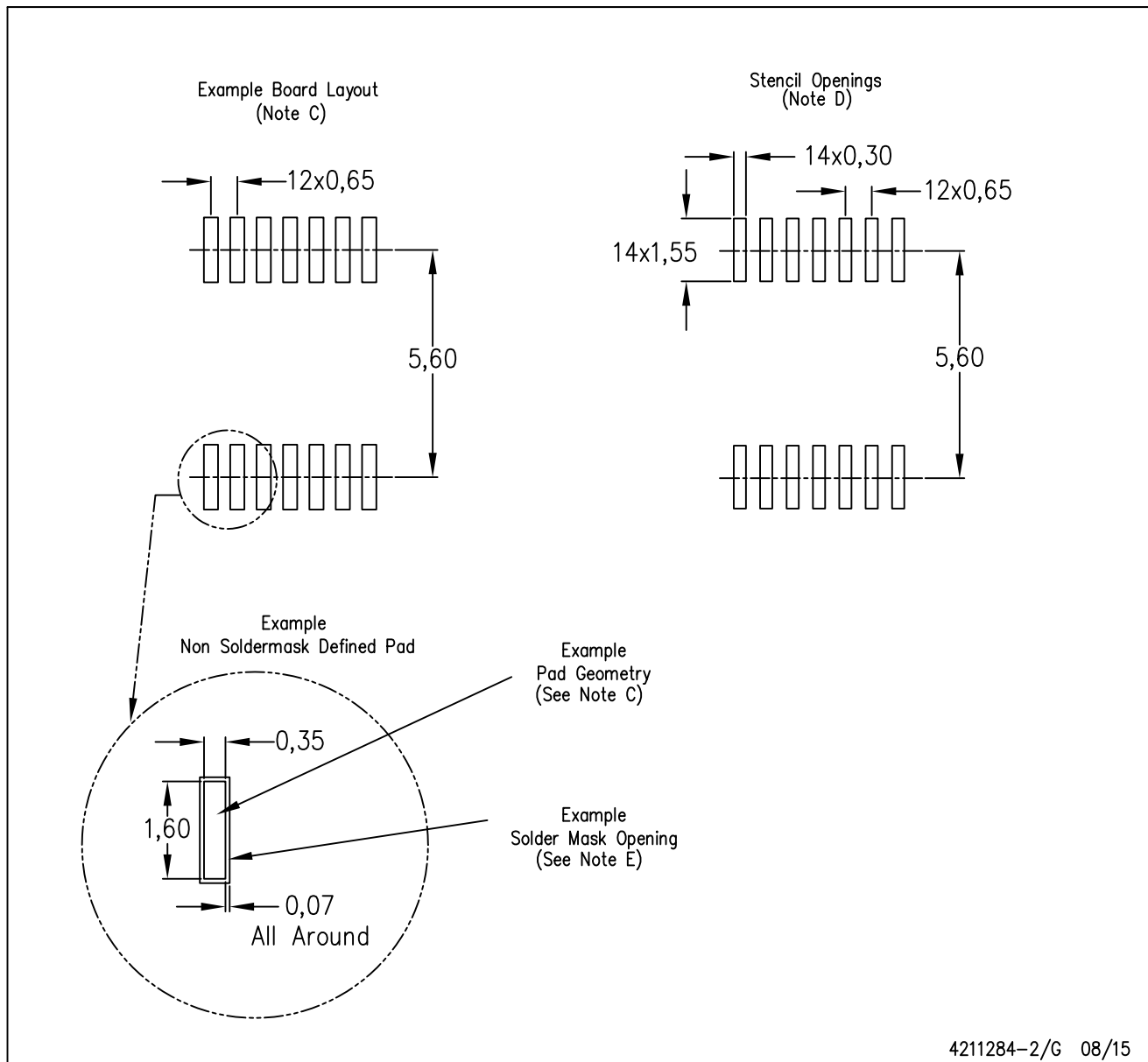


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

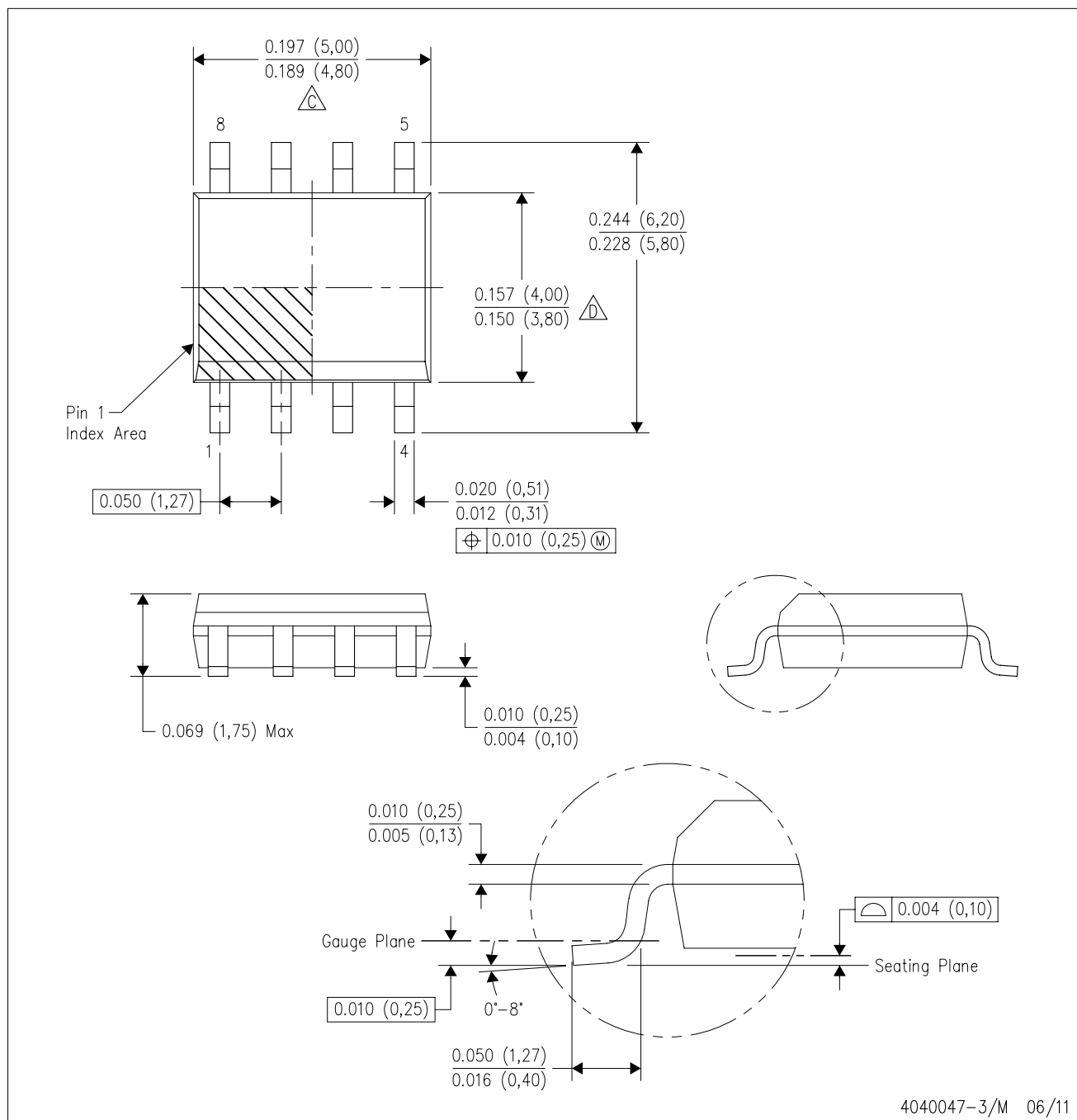
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

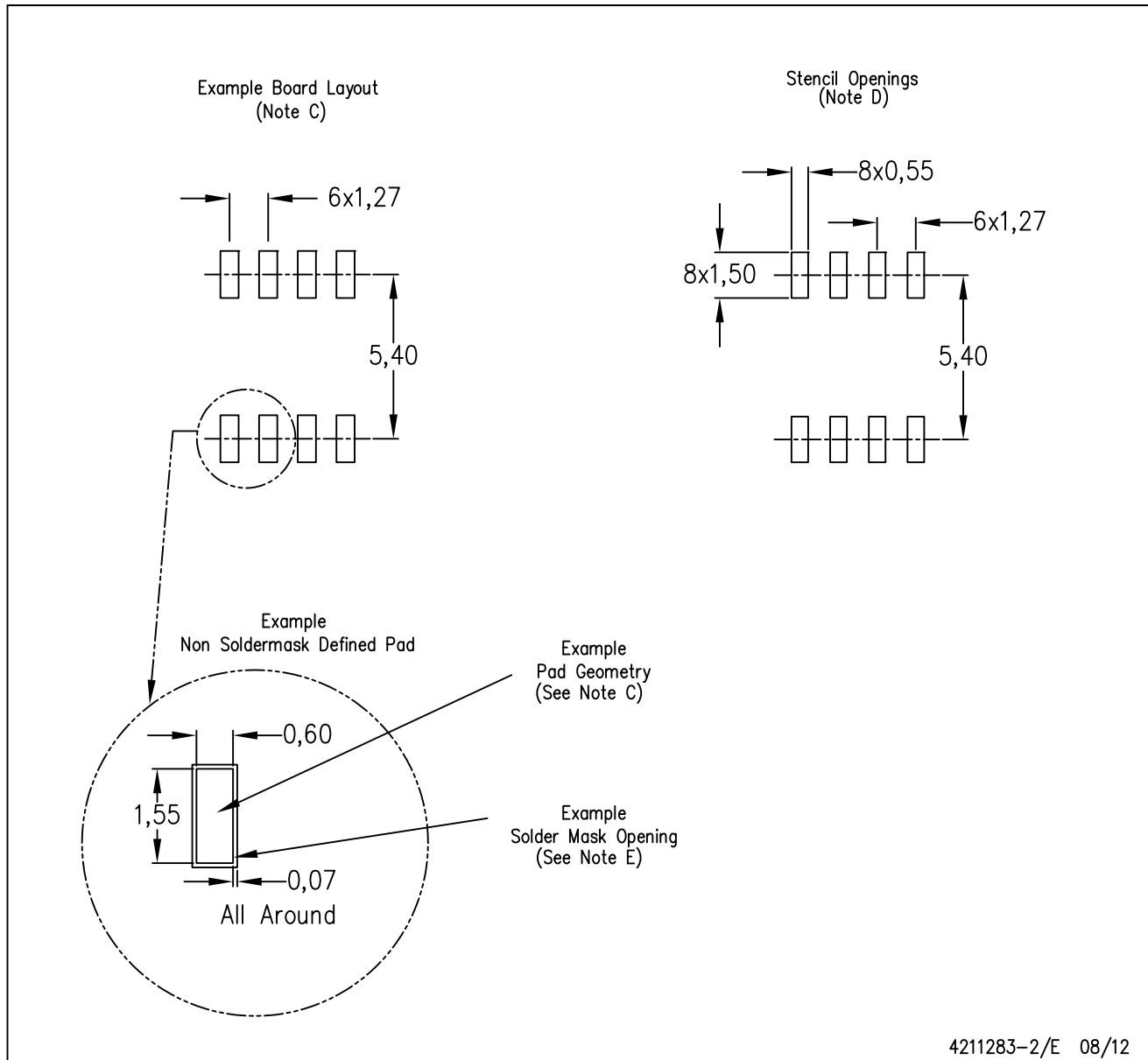


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

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