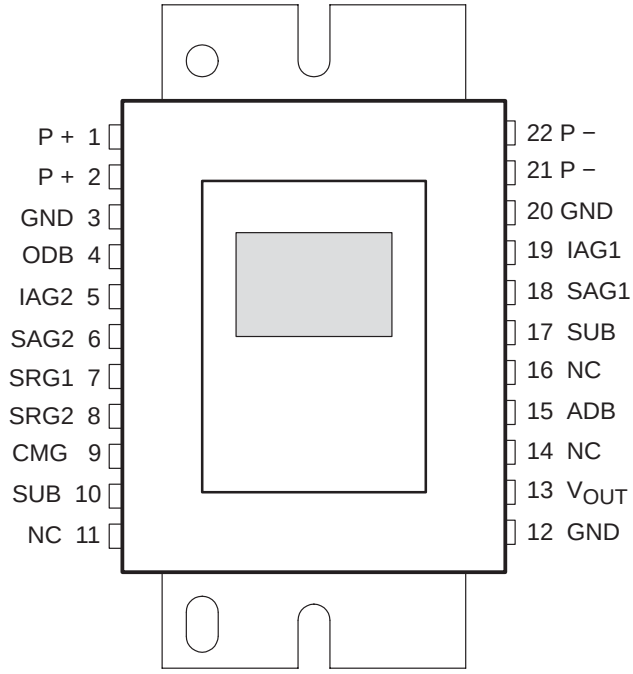
TC253SPD-B0
680 × 500 PIXEL IMPACTRON™ CCD IMAGE SENSOR

JULY 2003 − SOCS084

- **Very Low Noise, High Sensitivity Electronically Variable**
- **High Resolution, 1/3-in Format, Solid State Charge-Coupled Device (CCD) Frame Transfer Image Sensor for Black and White, NTSC, and Computer Applications**
- **340,000 Pixels per Field**
- **Frame Memory**
- **656 (H) × 496 (V) Active Pixels in Image Sensing Area Compatible With Electronic Centering**
- **Multimode Readout Capability**
  - **Progressive Scan**
  - **Interlace Scan**
  - **Line Summing**
- **Fast Single-Pulse Clear Capability**
- **Continuous Electronic Exposure Control From 1/30 s to 1/5,000 s**
- **7.4-μm Square Pixels**
- **Advanced Lateral Overflow Drain**
- **Low Dark Current**
- **High Photoresponse Uniformity Over a Wide Spectral Range**
- **Solid-State Reliability With No Image Burn-In, Resideual Imaging, Image Distortion, Image Lag, or Microphonics**
- **Package With Peltier Cooler**

DUAL−IN−LINE PACKAGE
(TOP VIEW)



description

The TC253SPD-B0 is a frame-transfer, CCD image sensor designed for use in black and white, NTSC TV, computer, and special-purpose applications requiring high sensitivity, low noise, and small size.

The TC253SPD-B0 is a new device of the IMPACTRON™ family of very-low noise, high sensitivity image sensors that multiply charge directly in charge domain before conversion to voltage. The charge carrier multiplication (CCM) is achieved by using a low-noise single-carrier, impact ionization process that occurs during repeated carrier transfers through high-field regions. Applying multiplication pulses to specially designed gates activates the CCM. The amount of multiplication is adjustable depending on the amplitude of the multiplication pulses. The device function resembles the function of image intensifiers implemented in solid state.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic-voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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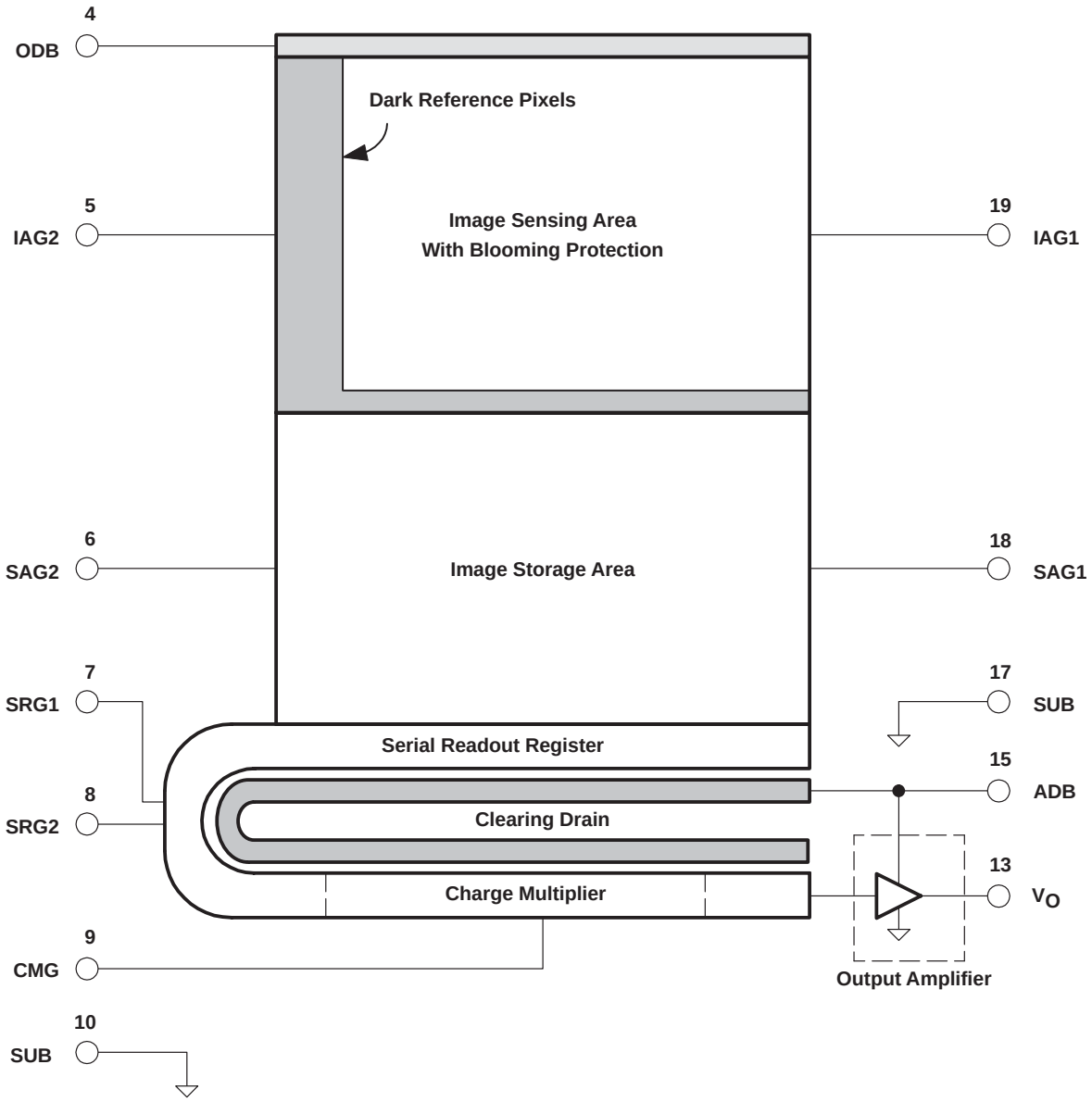
description (continued)

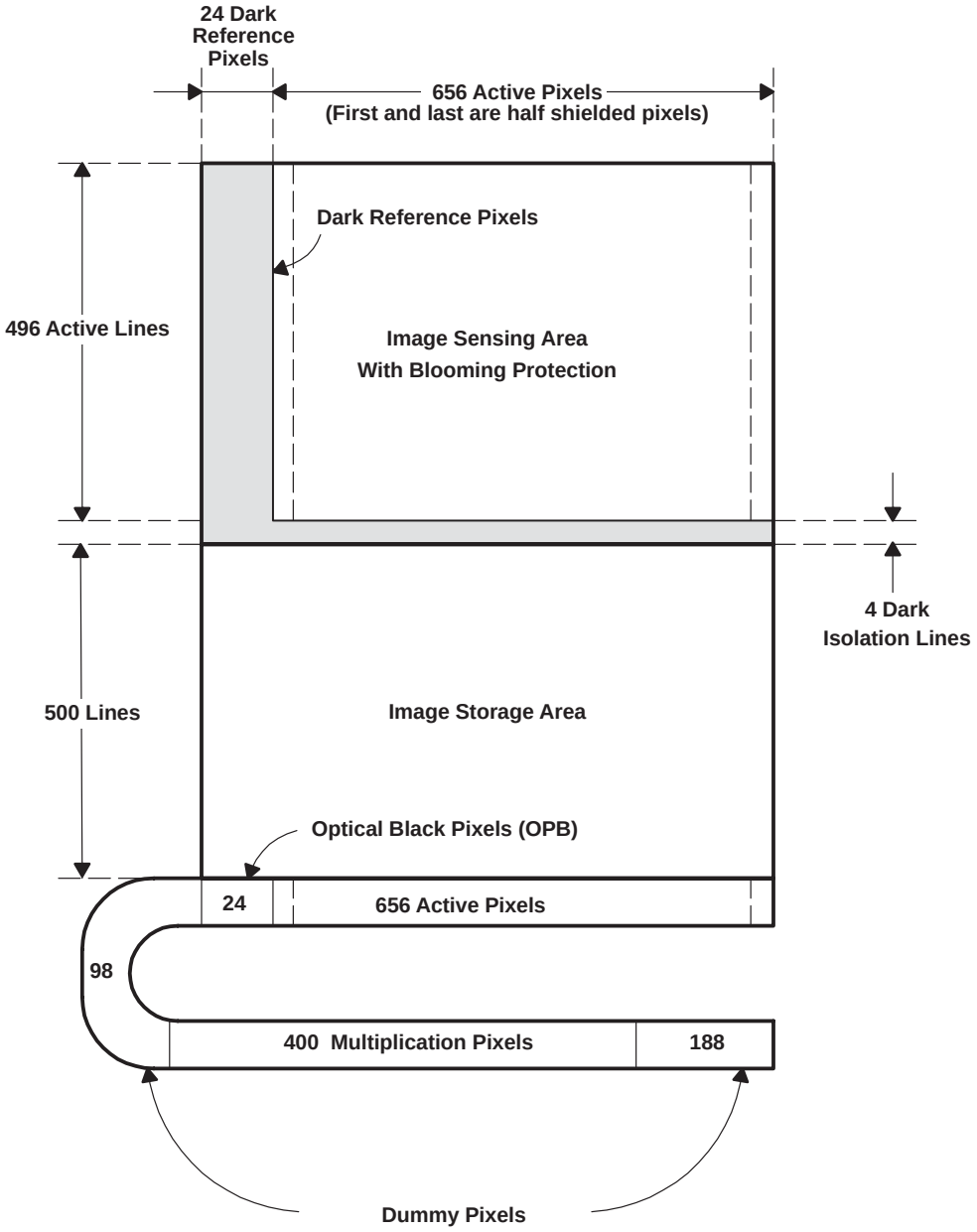
The image-sensing area of the TC253SPD-B0 is configured into 500 lines with 680 pixels in each line. Twenty-four pixels are reserved in each line for dark reference. The blooming protection is based on an advanced lateral overflow drain concept that does not reduce NIR response. The sensor can be operated in the interlaced or progressive scan modes and can capture a full 340,000 pixels in one image field. The frame transfer from the image sensing area to the memory area is accomplished at a very high rate that minimizes image smear. The electronic exposure control is achieved by clearing unwanted charge from the image area using a short positive pulse applied to the antiblooming drain. This marks the beginning of the integration time, which can be arbitrarily shortened from its nominal length. After the charge is integrated and stored in memory, it becomes available for readout in the next cycle. This is accomplished using a unique serial register design that includes special charge multiplication pixels.

The TC253SPD-B0 sensor is built using TI-proprietary advanced split-gate virtual-phase CCD (SGVPCCD) technology, which provides devices with wide spectral response, high quantum efficiency (QE), low dark current, and high response uniformity. The TC253SPD-B0 sensors are characterized for operation from –10°C to 45°C.

functional block diagram



sensor topology diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADB	15	I	Supply voltage for amplifiers and clearing drain
CMG	9	I	Charge multiplication gate
GND	3, 12, 20		Ground
IAG1	19	I	Image area gate 1
IAG2	5	I	Image area gate 2
NC	11, 14, 16	−	No connection
ODB	4	I	Supply voltage for antiblooming drain
P+	1, 2	I	Peltier cooler power supply—positive
P−	21, 22	I	Peltier cooler power supply—negative
SAG1	18	I	Storage area gate 1
SAG2	6	I	Storage area gate 2
SRG1	7	I	Serial register gate 1
SRG2	8	I	Serial register gate 2
SUB	10, 17	−	Chip substrate
VOUT	13	O	Output signal, multiplier channel

detailed description

The TC253SPD-B0 consists of four basic functional blocks: The image-sensing area, the image-storage area, the serial register, and the charge multiplier. The location of each of these blocks is identified in the functional block diagram.

image-sensing and storage areas

Figure 1 shows cross sections with potential-well diagrams. As light enters the silicon in the image-sensing area, electrons are generated and collected in the potential wells of the pixels. Applying a suitable dc bias to the antiblooming drain provides blooming protection. The electrons that exceed a specified level, determined by the ODB bias, are drained away from the pixels. If it is necessary to remove all previously accumulated charge from the wells, a short positive pulse must be applied to the drain. This marks the beginning of the new integration period. After the integration cycle is completed, charge is quickly transferred into the memory where it waits for readout. The lines can be read out from the memory in a sequential order to implement progressive scan, or two lines can be summed together to implement the pseudo-interlace scan.

Twenty-four columns at the left edge of the image-sensing area are shielded from the incident light. These pixels provide the dark reference used in subsequent video-processing circuits to restore the video-black level. Four additional dark lines, located between the image sensing area and the image-storage area, are added for isolation.

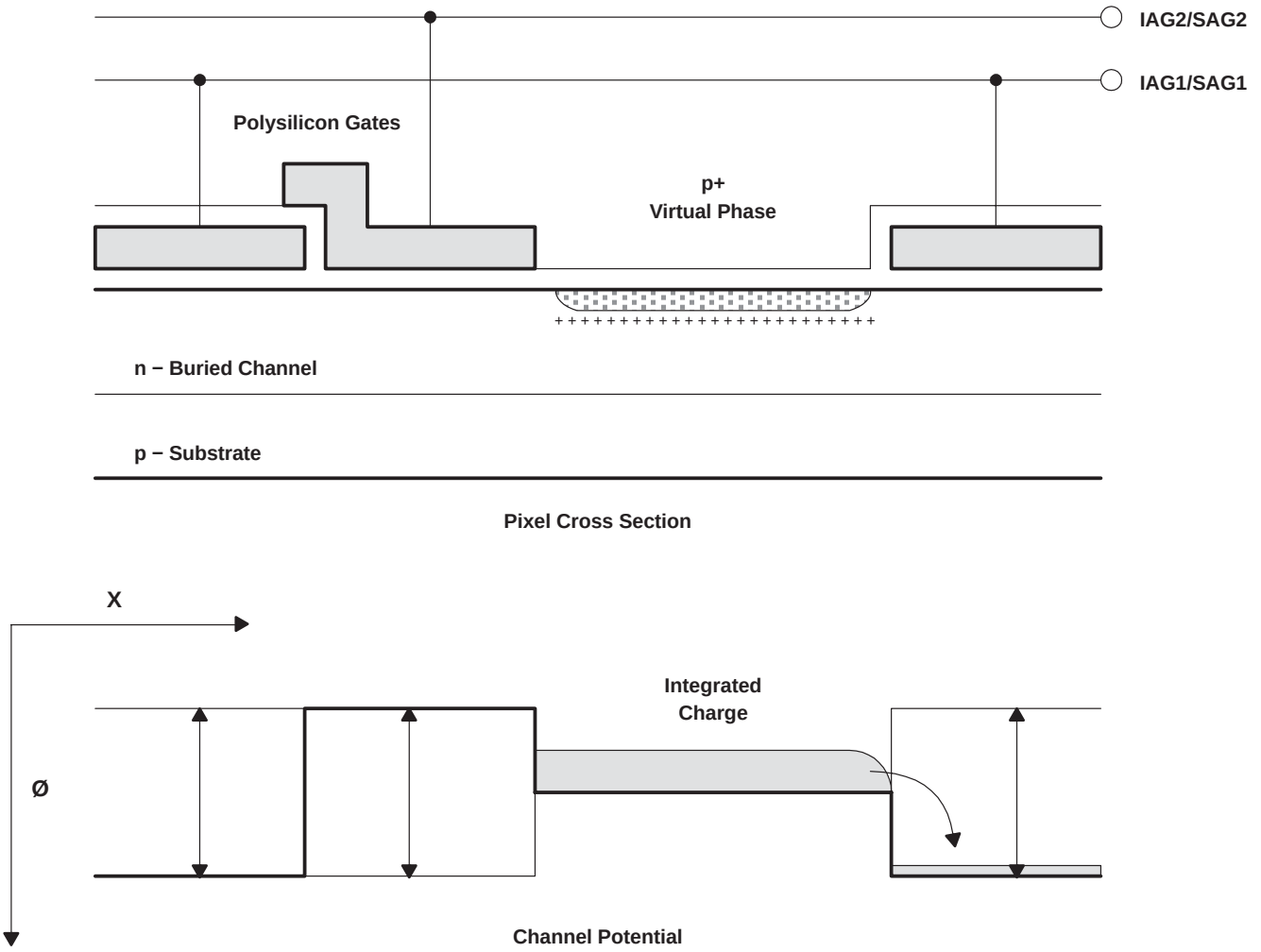


Figure 1. Image Area and Storage Area Pixel Cross Section With Potential Diagram

advanced lateral overflow drain

The advanced lateral overflow drain structure is shared by two neighboring pixels in each line. Varying the dc bias of the antiblooming drain controls the blooming protection level and trades it for well capacity. Applying a pulse to the drain, approximately 7 V above the nominal level for a minimum of 1 µs, removes all charge from the pixels. This feature permits precise control of the integration time on a frame-by-frame basis. The single-pulse clearing capability also reduces smear by eliminating accumulated charge in pixels before the start of the integration period (single-sided smear). The application of a negative 0.5-V pulse to the antiblooming drain during the parallel transfer is recommended. This pulse prevents the creation of undesirable artifacts caused by the on-chip cross talk between the image area gate clock lines and the antiblooming drain bias lines.

serial register and charge multiplier

The serial register is used for transporting charge stored in the memory pixels to the output amplifier. However, the TC253SPD-B0 device has a serial register with twice the standard length. The first half has a conventional design that interfaces with the memory and the clearing drain as it would in any other CCD sensor (for example the TC237 sensor). The second half, however, is unique and includes 400 charge-multiplication stages with a number of dummy pixels that are needed to transport charge between the active register blocks and the output

amplifier. Charge is multiplied as it progresses from stage to stage in the multiplier toward the charge detection node. The charge multiplication level depends on the amplitude of the multiplication pulses (approximately 11 V~15 V) applied to the multiplication gates. Due to the double length of the register, the first line in the field or frame scan does not contain valid data and should be discarded.

readout and video processing

The last element of the charge readout and detection chain is the charge detection node. The charge detection node uses standard floating diffusion (FD) concepts followed by dual stage source followers as buffer amplifiers. The reset gate is internally connected to SRG1. This results in simultaneous FD resets when the SRG1 gate is clocked high. To achieve the ultimate sensor performance, it is necessary to eliminate kTC noise using CDS processing techniques. The IMPACTRON™ devices can detect single photons when cooled or when sufficiently short integration times are used.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, Vss: ADB (see Note 1) . . . . . SUB to SUB + 15 V
Supply voltage range, Vss: ODB . . . . . SUB to SUB + 20 V
Input voltage range, V_I: IAG, SAG, SRG2 . . . . . −8 V to + 8 V
Input voltage range, V_I: SRG1 . . . . . −5 V to + 8 V
Input voltage range, V_I: CMG . . . . . −5 V to + 15 V
Supply voltage range, Vcool: P+ (see Note2) . . . . . 0 V + 3 V
Supply current range, Icool: P+ (see Note2) . . . . . 0 mA to 700 mA
Operating free-air temperature range, T_A . . . . . −10°C to 45°C
Storage temperature range, T_{STG} . . . . . −30°C to 85°C
Operating case temperature range . . . . . −10°C to 55°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to substrate terminal.
2. Peltier cooler generates heat during cooling process. To keep case temperature range, the heat must be removed through external heat sink.

recommended operating conditions

				MIN	NOM	MAX	UNIT
Substrate bias, V_{SS}					0		V
Supply voltage, V_{DD}	ADB			11.5	12	12.5	V
	ODB	For blooming control (see Note 3)		4.3	5.3	6.3	
		For clearing		12	12.5	13	
		For transfer (see Note 4)		3.8	4.8	5.8	
Input voltage, V_I		IAG1	High	4.9	5.2	5.5	V
		IAG2, SAG1, SAG2	High	2.8	3.1	3.4	
		IAG1, SAG1	Low	−6.3	−6	−5.7	
		IAG2, SAG2	Low	−7	−6.7	−6.4	
		SRG1, SRG2	High	4.6	4.9	5.2	
		SRG1	Low	−4.6	−4.3	−4	
		SRG2	Low	−5.8	−5.5	−5.2	
		CMG (see Note 5)	High (Gain)	7 (1)	14.5 (30)	15 (100)	
			Low	−3.1	−2.8	−2.5	

Clock frequency, f_{clk}	SAG1, SAG2		3.125	MHz
	IAG1, IAG2		3.125	
	SRG1, SRG2		12.5	
	CMG		12.5	
Load capacitance	OUT		6	pF
Operating free-air temperature, T_A		−10	45	°C

NOTES: 3. Adjustment within the specified MIN − MAX range may be required to optimize performance.
4. Application of a negative 0.5-V pulse (with respect to blooming control level) during parallel transfer is recommended for better antiblooming performance.
5. Over time, slight increase in CMG high level may be required to achieve corresponding gain.

electrical characteristics over recommended operating ranges of supply voltage at operating free-air temperature (unless otherwise noted)

	PARAMETER		MIN	TYP‡	MAX	UNIT
	Charge multiplication gain		1	30	(100)§	
	Excess noise factor for typical CCM gain (see Note 6)		1	1.4		
	Dynamic range without CCM gain			64		dB
	Dynamic range with typical CCM gain (see Note 7)			66		dB
	Charge conversion gain without CCM gain (see Note 8)			9		μV/e⁻
τ	Signal-response delay time (see Note 9)			9		ns
	Output resistance			320		Ω
	Amplifier noise-equivalent signal without CCM gain†			29		e⁻ rms
	Response linearity without CCM gain			1		
	Response linearity with typical CCM gain			1		
	Charge-transfer efficiency (see Note 10)		0.9998	0.9999		
	Supply current		2	3	4	mA
Ci	Input capacitance	IAG1		3		nF
		IAG2		3.2		
		IAG1-IAG2		2		
		SAG1		3		
		SAG2		3.6		
		SAG1-SAG2		2.2		
		SRG1		40		pF
		SRG2		40		
		SRG1−SRG2		50		
		CMG		30		
		CMG−SRG1		10		
		ODB		1,000		
	Pulse amplitude rejection ratio	ADB high (see Note 11)		20		dB
		SRG−1,2 high (Note 11)		45		
		SRG−1,2 low (Note 11)		45		
		CMG high (see Note 11)		45		
		CMD low (see Note 11)		45		
		OBD low (see Note 11)		45		

† The values in the table are quoted using CDS = correlated double sampling. CDS is a signal-processing technique that improves performance by minimizing undesirable effects of reset noise.

‡ All typical values are at T_A = 25°C.

§ Maximum CCM gain is not ensured.

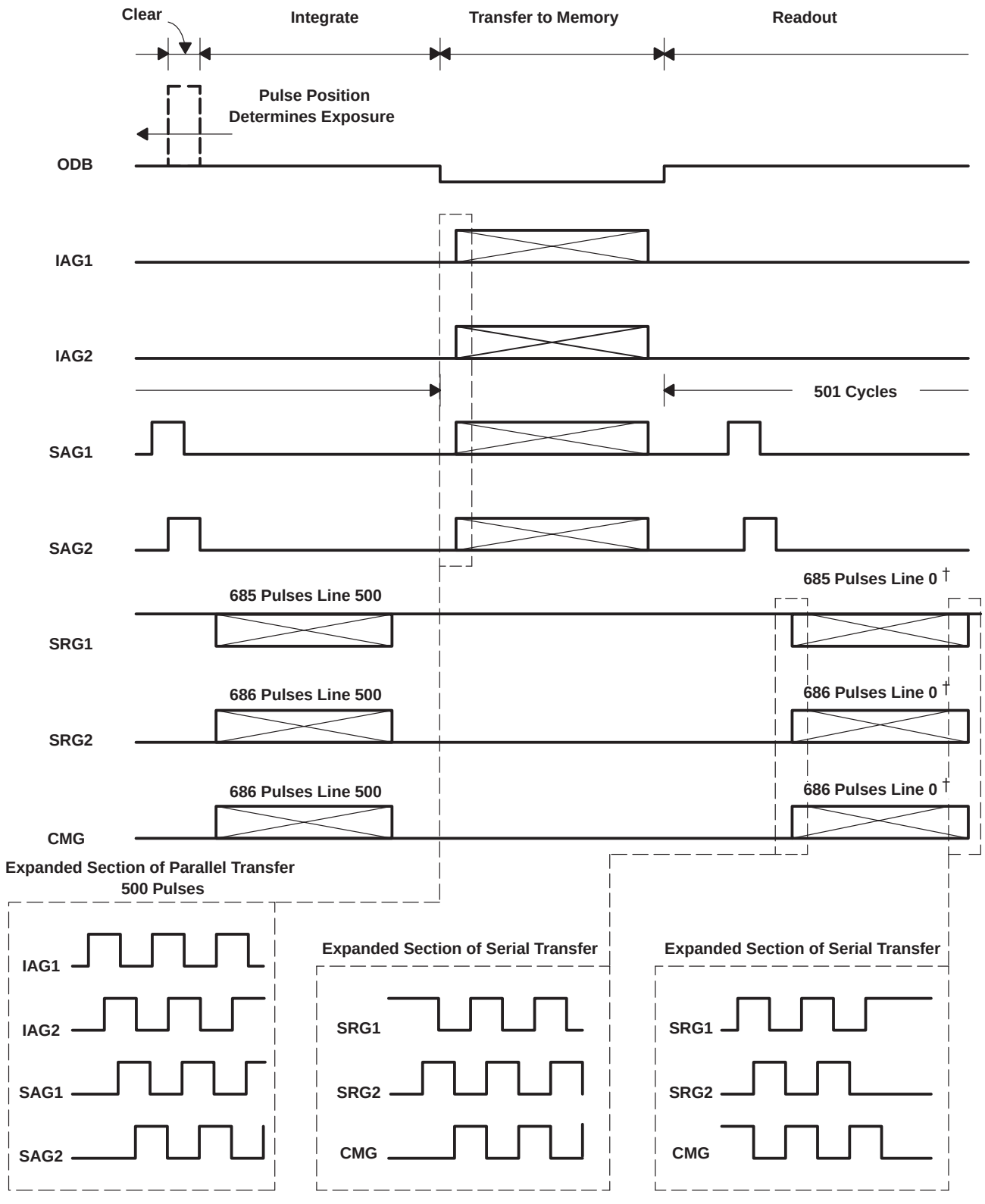
NOTES: 6. Excess noise factor F is defined as the ratio of noise sigma after multiplication divided by M times the noise sigma before multiplication, where M is the charge multiplication gain.

7. Dynamic range is −20 times the logarithm of the noise sigma divided by the saturation-output signal amplitude.
8. Charge-conversion factor is defined as the ratio of output signal to input number of electrons.
9. Signal-response delay time is the time between the falling edge of the SRG2 pulse and the output-signal valid state.
10. Charge transfer efficiency is one minus the charge loss per transfer in the CCD register.
11. Rejection ratio is −20 times the logarithm of the output referenced to the reset level divided by the 1 V of amplitude change of the corresponding gate or terminal signal.

optical characteristics, T_A = 25°C (unless otherwise noted)

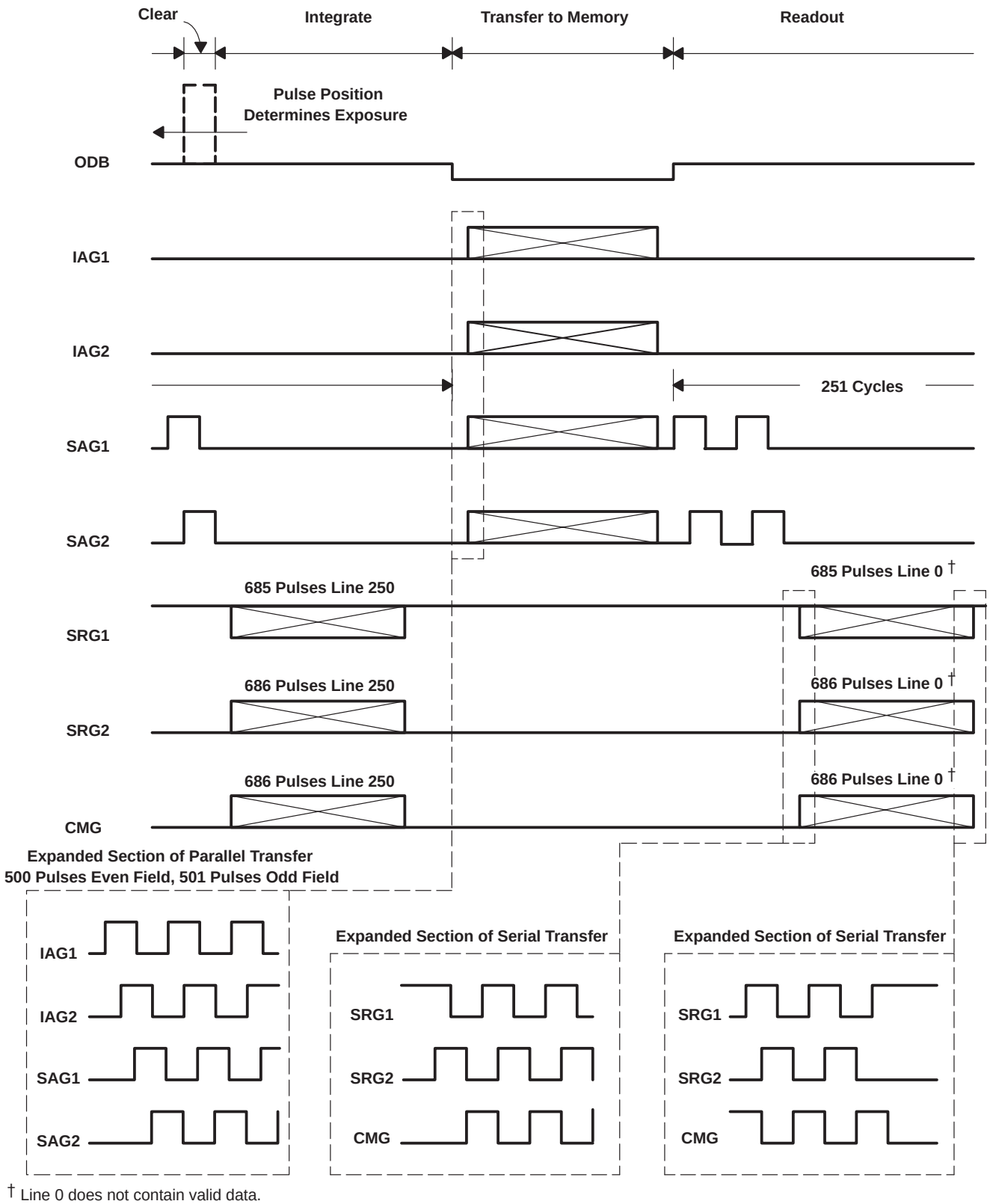
PARAMETER			MIN	TYP	MAX	UNIT
	Sensitivity with typical CCM gain (see Note 12)	No IR filter		290		V/Lx*s
		With IR filter		36		
	Sensitivity without CCM gain (see Note 12)	No IR filter		9.6		V/Lx*s
		With IR filter		1.2		
V_{sat}	Saturation signal output without CCM gain (see Note 13)		300	400		mV
	Handling capacity of charge multiplier		400	500		
V_{off}	Zero-input offset output (see Note 14)			90	200	mV
	Blooming overload ratio (see Note 15)				1000:1	
	Image area well capacity		33k	44k		e^-/pixel
	Smear (see Note 16)			60		dB
	Dark current (see Note 17 and Note 22)			0.01	0.03	nA/cm^2
	Dark signal (see Note 18 and Note 22)			0.005	0.015	mV
	Dark-signal uniformity (see Note 19)				0.15	mV
	Dark-signal shading (see Note 20)				0.1	mV
	Spurious nonuniformity	Dark		0.8	1.5	mV
		Illuminated	−20		20	%
	Column uniformity (see Note 21)				4.5	mV
	Electronic-shutter capability		1/5000	1/30		s

NOTES: 12. Light source temperature is 2856 °K. The IR filter used is CM500, 1-mm thick.
13. Saturation is the condition in which further increase in exposure does not lead to further increases in output signal.
14. Zero-input offset is the residual output signal measured from the reset level with no input charge present. This level is not caused by the dark current and remains approximately constant, independent of temperature. It may vary with the amplitude of SRG.
15. Blooming is the condition in which charge induced by light in one element spills over to the neighboring elements.
16. Smear is the measure of error signal introduced into the pixels by transferring them through the illuminated region into the memory. The illuminated region is 1/10 of the image area height. The value in the table is obtained for an integration time of 16.66 ms and a 3.125-MHz vertical-clock transfer frequency.
17. Dark current depends on temperature and approximately doubles every 8 °C. Dark current is also multiplied by CCM operation. The value given in the table is with the multiplier turned off and it is a calculated value.
18. Dark signal is actual device output measured in darkness.
19. Dark signal uniformity is the sigma of the difference between two neighboring pixels taking from all the image area pixels.
20. Dark signal shading is the difference between maximum and minimum of a 5-pixel median taken anywhere in the array.
21. Column uniformity is obtained by summing all the lines in the array, finding the maximum of the difference between two neighboring columns anywhere in the array, and dividing the result by the number of lines.
22. There will be an estimated 20% degradation in dark current performance when exposed to 320 nm UV light at 1 uWatt/cm^2 for 2700 hours.



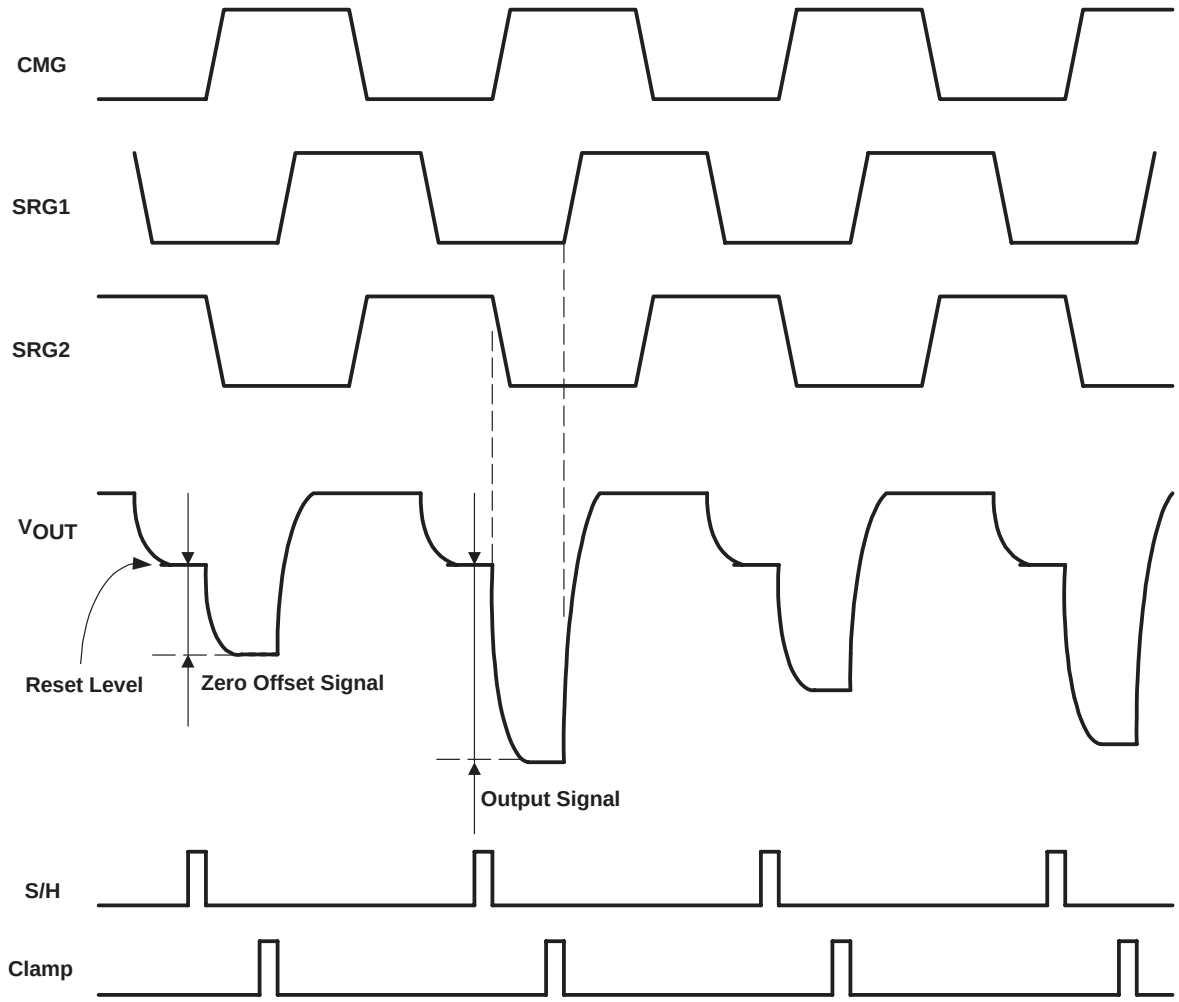
† Line 0 does not contain valid data.

Figure 2. Progressive Scan Timing



† Line 0 does not contain valid data.

Figure 3. Interlace Timing for Line Summing Mode



* Output signal may not be zero for zero input charge.

Figure 4. Serial Resistor Clock Timing for CDS Implementation

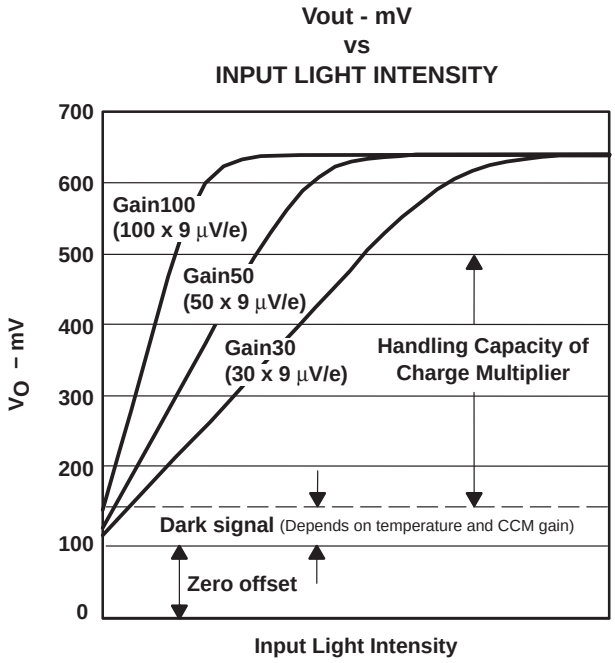


Figure 5. Photon Transfer Characteristic of CCD Output

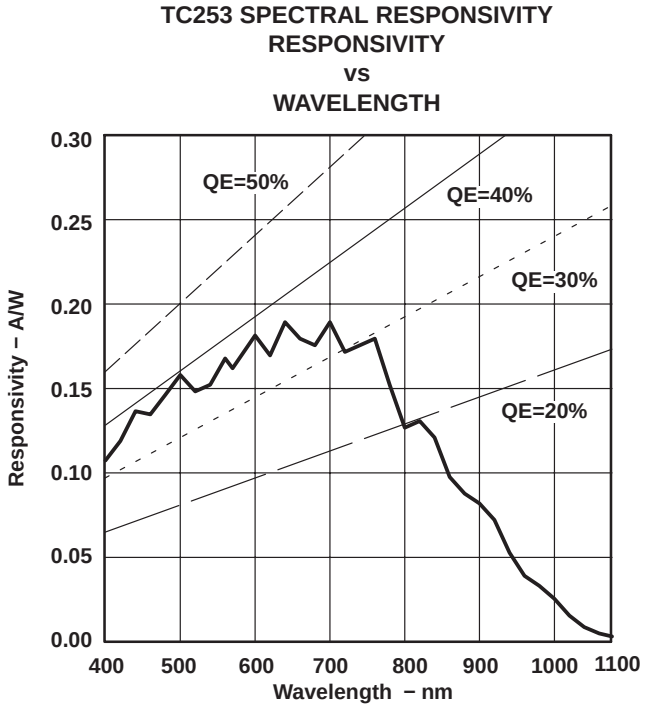


Figure 6. Typical Spectral Responsivity

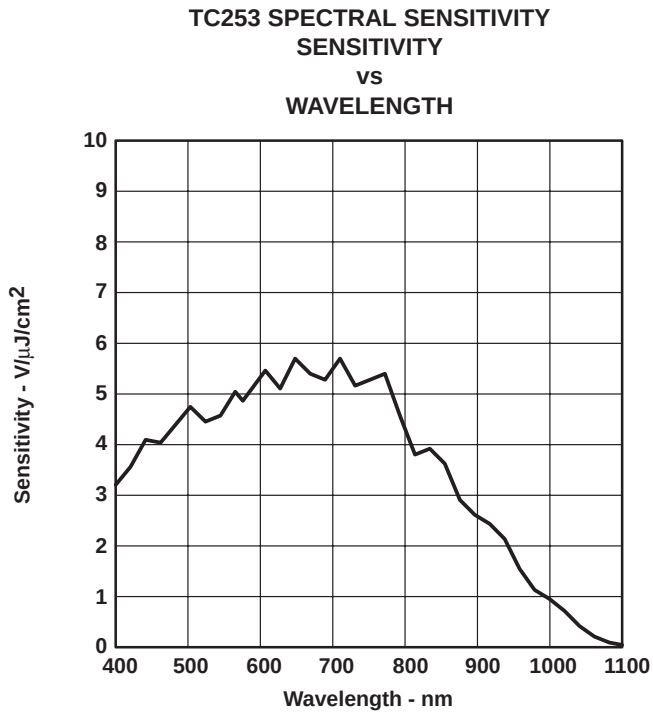


Figure 7. Typical Spectral Sensitivity

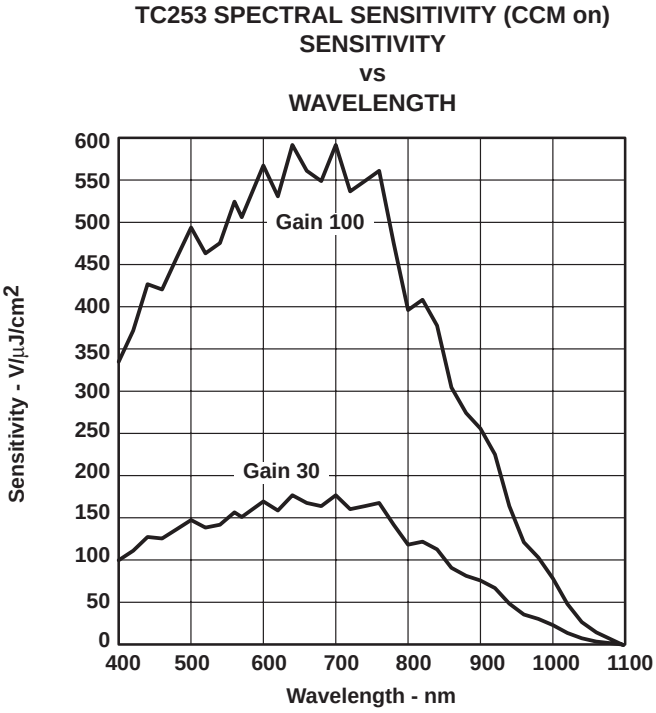


Figure 8. Typical Spectral Sensitivity (CCM on)

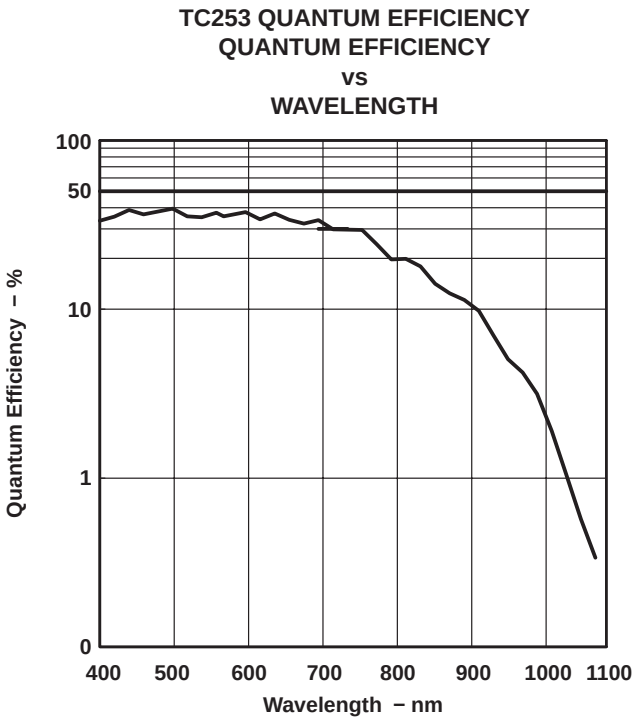


Figure 9. Typical Spectral Quantum Efficiency

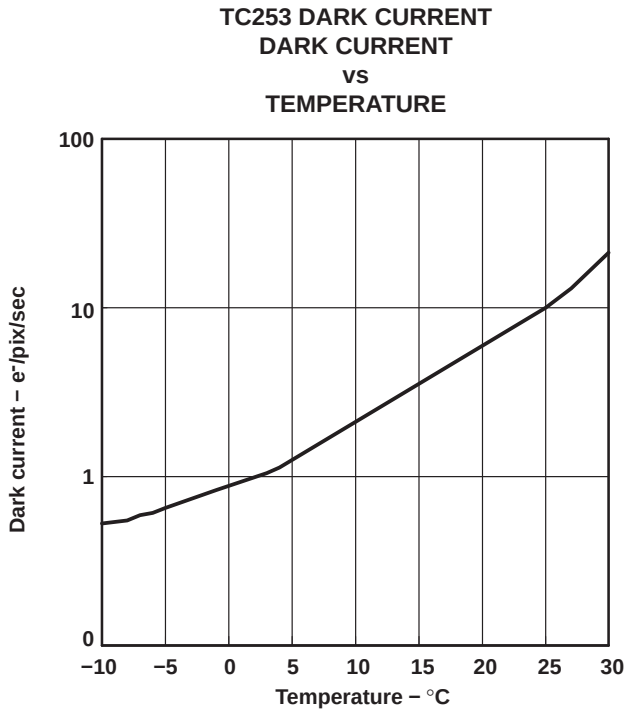


Figure 10. Typical Variation of Dark Current with Temperature

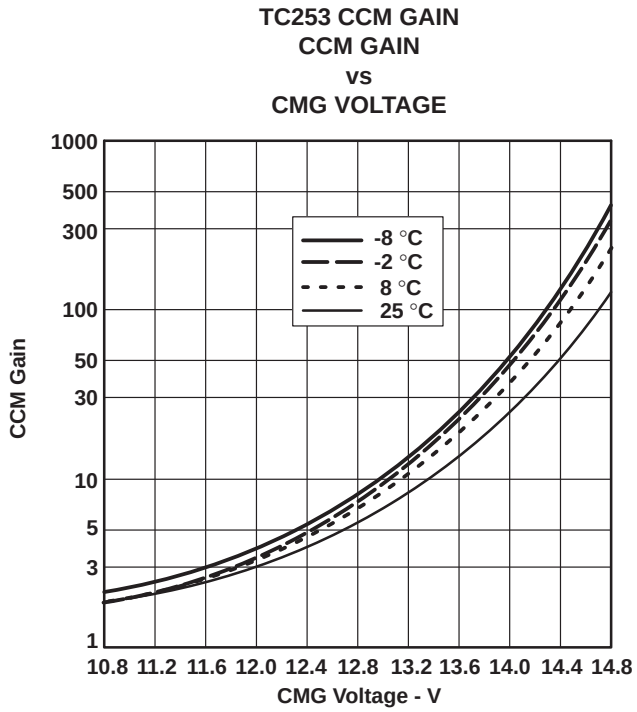
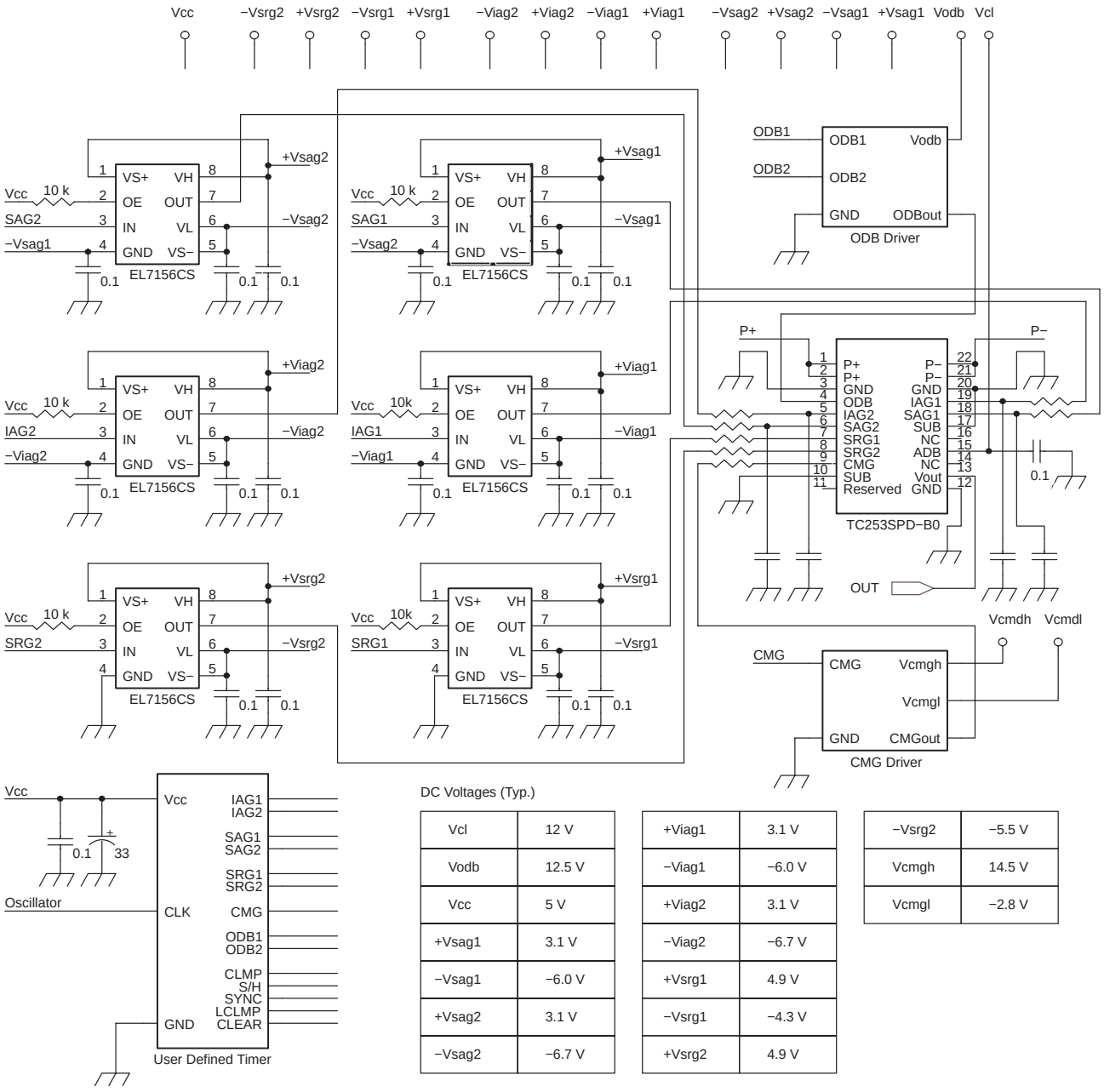


Figure 11. Typical Variation of CCM Gain with CMG Voltage



DC Voltages (Typ.)

Vcl	12 V
Vodb	12.5 V
Vcc	5 V
+Vsag1	3.1 V
−Vsag1	−6.0 V
+Vsag2	3.1 V
−Vsag2	−6.7 V

+Viag1	3.1 V
−Viag1	−6.0 V
+Viag2	3.1 V
−Viag2	−6.7 V
+Vsrg1	4.9 V
−Vsrg1	−4.3 V
+Vsrg2	4.9 V

−Vsrg2	−5.5 V
Vcmgh	14.5 V
Vcmgl	−2.8 V

Notes: A. All values are in Ohms and Microfarads unless otherwise noted.

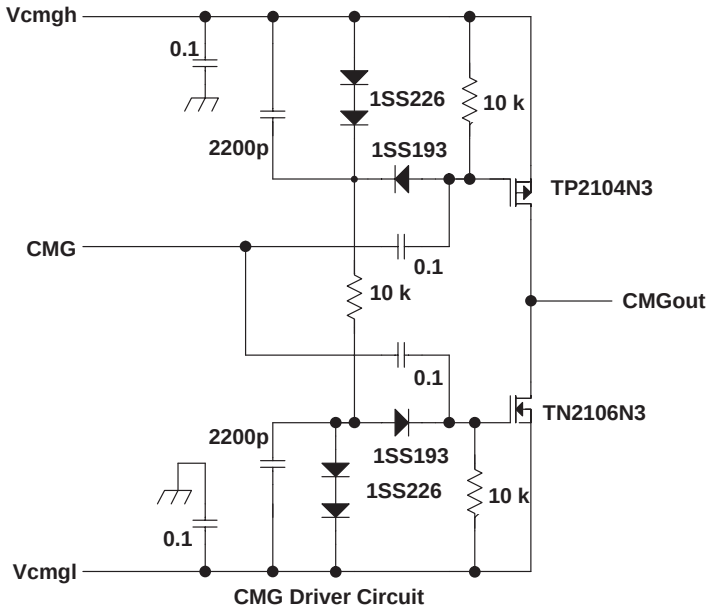
B. TI recommends AC coupled system for coupling to the next video processing circuits.

C. IAG and SAG signal from "User Defined Timer" should be shifted its GND level to −V before the driver IC (EL7156CS) input.

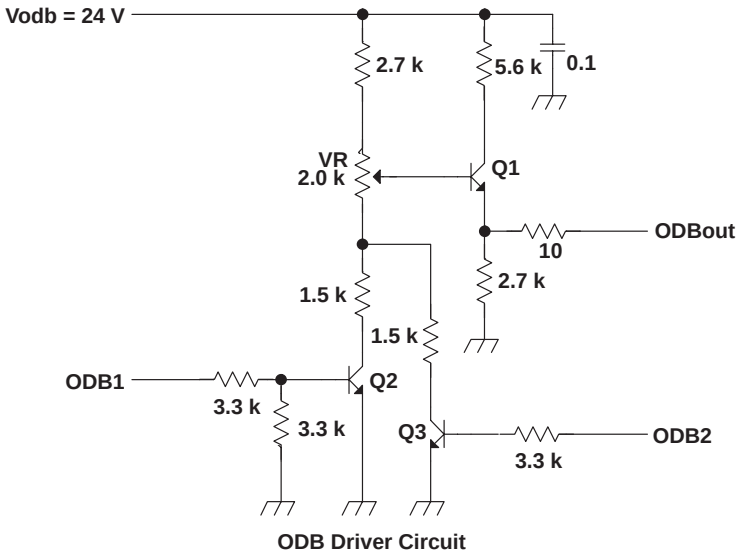
D. The value of the CCD external capaciters (on IAG and SAG) were recommended with 1000pF.

E. P+ and P− should be connected to the cooling controller (current source for the peltier cooler).

Figure 12. Typical Application Circuit Diagram



CMG Driver Circuit



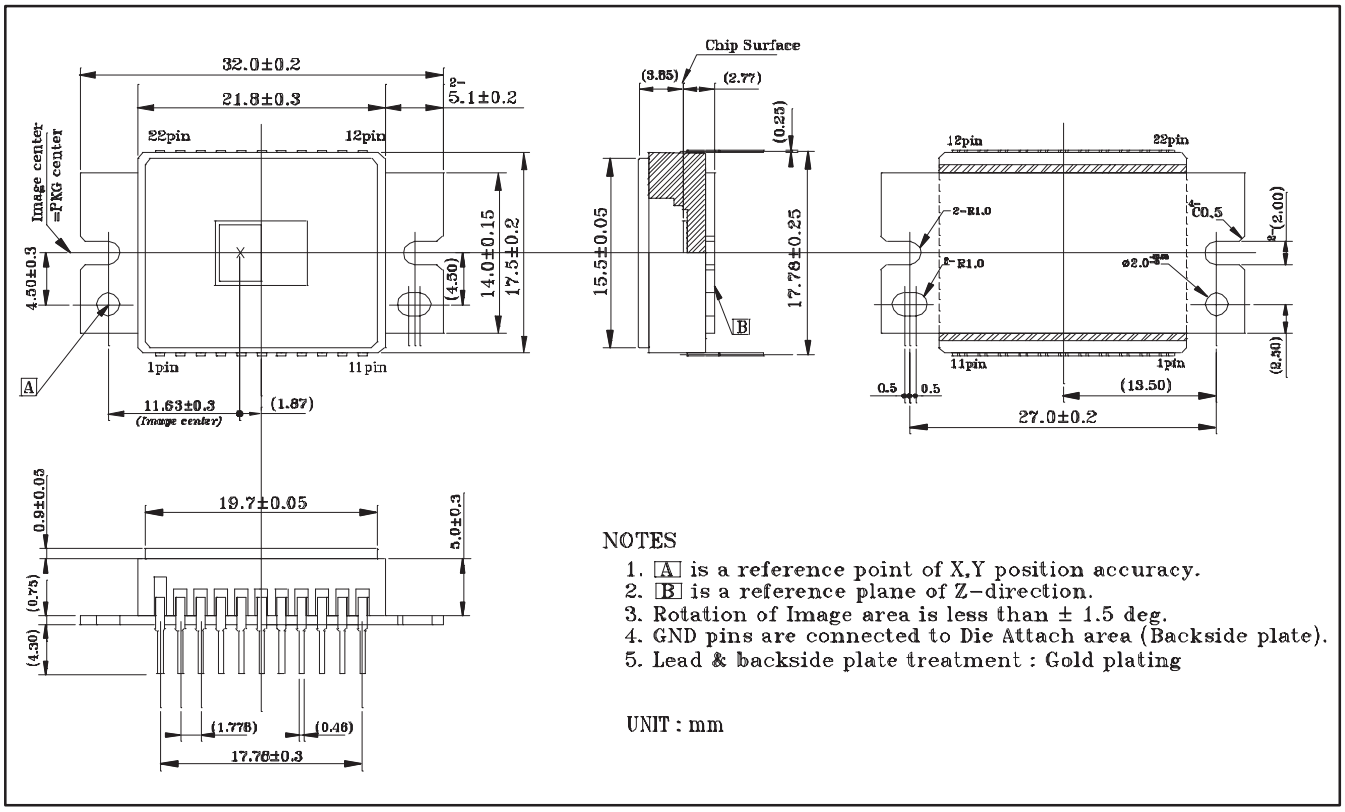
ODB Driver Circuit

Notes: A. All values are in Ohms and Microfarads unless otherwise noted.

Figure 13. Example of CMG Driver Circuit

MECHANICAL DATA

The package for the TC253SPD-B0 consists of a ceramic base, a glass window, and a 22-lead frame. The glass window is sealed to the package by an epoxy adhesive. The package leads are configured in a dual-in-line arrangement and fit into mounting holes with 1,78-mm center-to-center spacing.



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