DATA SHEET

# GPF16001A

## Advanced 16-bit SoC with $\mu$'nSP®

## 2.0

***Preliminary***

May 02, 2011

Version 0.1

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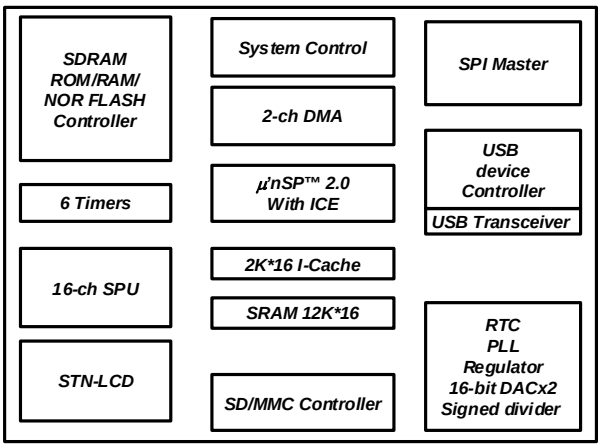
# Advanced 16-bit SoC with μ'nSP® 2.0

## 1. GENERAL DESCRIPTION

The Generalplus GPF16001A is a highly integrated system-on-a chip and it targets a cost-effective, high performance micro-controller solution for education and learning applications. It is embedded a μ'nSP® 2.0 (16-bit CPU developed by Sunplus Technology) with 4KB I-cache, 16 channels sound process unit (SPU), SDRAM controller, ROM/SRAM/NOR FLASH, two-channel DMA controller, six-channel 16-bit timers, SD/MMC memory interface, USB device, mono STN-LCD interface, interrupt controller, SPI master controller, programmable I/O ports, 16-bit DAC for audio playback, PLL, divider and 12K*16-bit SRAM.

By providing a complete set of common system peripherals, GPF16001A chip minimizes overall system costs and eliminates the needs of additional components. Not only does the GPF16001A provide the high-speed performance and low cost for a system, but also it integrates several powerful tools into the development system, such as development system with C language, assembly compiler, linker, source debugger functions and project management tools.

## 2. BLOCK DIAGRAM




## 3. FEATURES

- μ'nSP® 2.0 16-bit CPU with frequency up to 96MHz.
- 4K bytes I-cache.
- 12k*16-bit SRAM for programming or LCD frame buffers.
- Sound Process Unit (SPU)
  - 16 hardware PCM/ADPCM channels
  - Built-in sound compressor
- 96 MHz SDRAM with maximum size 64M bytes for single chip selection.
- Static memory controller. (ROM/SRAM/NOR FLASH/Page Memory)
- Two-channel DMA controller.
- Mono and 16-gray STN-LCD controller.
- 29 sources Interrupt Controller.
- Universal Serial Bus (USB) 2.0 full speed compliant device with built-in transceiver.
- Watchdog timer.
- 32-bit by 32-bit signed divider.
- Real-time clock.
- Six 16-bit timers.
- SD/MMC memory interface.
- SPI master interface.
- 51 Programmable general I/O ports with pull-high/low control.
- Power manager.
- Built-in 3.0V to 1.8V Regulator.
- Low voltage reset.
- 96MHz, 27MHz and 12MHz PLL.
- 16-bit stereo DAC (2ch) for audio playback.

## 4. SIGNAL DESCRIPTIONS

Left Side

| No | Package No | Name | Group | Type | Normal Function Description | GPIO Group |
|---|---|---|---|---|---|---|
| 1 | 2 | DVSS | Digital GND | P | Digital ground | |
| 2 | 3 | BKCSB0 | Memory I/F | I/O | External memory chip select 0 | IOD0 |
| 3 | 4 | XA3 | Memory I/F | I/O | External memory address pin 3 | |
| 4 | 5 | XA2 | Memory I/F | I/O | External memory address pin 2 | |
| 5 | 6 | XA1 | Memory I/F | I/O | External memory address pin 1 | |
| 6 | 7 | BKCSB1 | Memory I/F | I/O | External memory chip select 1 | IOD1 |
| 7 | 8 | XA0 | Memory I/F | I/O | External memory address pin 0 | |
| 8 | 9 | XA10 | Memory I/F | I/O | External memory address pin 10 | |
| 9 | 10 | XA11 | Memory I/F | I/O | External memory address pin 11 | |
| 10 | 11 | BKCSB2 | Memory I/F | I/O | External memory chip select 2 | IOD2 |
| 11 | 12 | XA12 | Memory I/F | I/O | External memory address pin 12 | |
| 12 | 13 | XA13 | Memory I/F | I/O | External memory address pin 13 | |
| 13 | 14 | XA14 | Memory I/F | I/O | External memory address pin 14 | |
| 14 | 15 | DVCC33 | Digital PWR | P | 3.3V digital power | |
| 15 | 16 | DVSS | Digital GND | P | Digital ground | |
| 16 | 17 | DVCC18 | Digital PWR | P | 1.8V digital power | |
| 17 | 18 | BKWEB | Memory I/F | I/O | External memory write enable pin | |
| 18 | 19 | BKOEB | Memory I/F | I/O | External memory output enable pin | |
| 19 | 20 | XA15 | Memory I/F | I/O | External memory address pin 15 | IOD7 |
| 20 | 21 | XA16 | Memory I/F | I/O | External memory address pin 16 | IOD8 |
| 21 | 22 | XA17 | Memory I/F | I/O | External memory address pin 17 | IOD9 |
| 22 | 23 | XA18 | Memory I/F | I/O | External memory address pin 18 | IOD10 |
| 23 | 24 | XA19 | Memory I/F | I/O | External memory address pin 19 | IOD11 |
| 24 | 25 | XA20 | Memory I/F | I/O | External memory address pin 20 | IOD12 |
| 25 | 26 | XA21 | Memory I/F | I/O | External memory address pin 21 | IOD13 |
| 26 | 27 | XA22 | Memory I/F | I/O | External memory address pin 22 | IOD14 |
| 27 | 28 | XA23 | Memory I/F | I/O | External memory address pin 23 | IOD15 |
| 28 | 29 | DVSS | Digital GND | P | Digital ground | |
| 29 | 30 | TEST | MODE | I | Test mode control signal. Input floating; it must be tied with ground under normal operation. | |

Bottom Side

| No | Package No | Name | Group | Type | Normal Function Description | GPIO Group |
|---|---|---|---|---|---|---|
| 30 | 31 | RESETB | SYSTEM | I/O | Reset input pin. (Low active) | |
| 31 | 32 | IOB2 | MODE | I/O | BM2: Boot mode selection pin 2.<br>(0: use 6MHz crystal ,1: use internal PLL) | IOB2 |
| 32 | 33 | IOB1 | MODE | I/O | BM1: Boot mode selection pin 1.<br>1 : Internal Boot (SPI boot)<br>0 : Chip Select 0 Memory Boot | IOB1 |
| 33 | 34 | IOB0 | MODE | I/O | BM0: Boot mode selection pin 0.<br>(This pin must be pull low with a resistor) | IOB0 |
| 34 | 35 | ICEDA | ICE | I/O | Embedded ICE data pin | |
| 35 | 36 | ICECK | ICE | O | Embedded ICE clock pin | |
| 36 | 37 | IOA7 | LCD | I/O | LCD's D7 | IOA7 |
| 37 | 38 | IOA6 | LCD | I/O | LCD's D6 | IOA6 |
| 38 | 39 | IOA5 | LCD | I/O | LCD's D5 | IOA5 |
| 39 | 40 | IOA4 | LCD | I/O | LCD's D4 | IOA4 |
| 40 | 41 | IOA3 | LCD | I/O | LCD's D3 | IOA3 |
| 41 | 42 | IOA2 | LCD | I/O | LCD's D2 | IOA2 |
| 42 | 43 | IOA1 | LCD | I/O | LCD's D1 | IOA1 |
| 43 | 44 | IOA0 | LCD | I/O | LCD's D0 | IOA0 |
| 44 | 45 | IOA8 | - | I/O | | IOA8 |
| 45 | 46 | DVCC33 | Digital PWR | PWR | 3.3V digital power | |
| 46 | 47 | DVSS | Digital GND | PWR | Digital ground | |
| 47 | 48 | DVCC18 | Digital PWR | PWR | 1.8V digital power | |
| 48 | 49 | IOA9 | - | I/O | - | IOA9 |
| 49 | 50 | IOA10 | - | I/O | - | IOA10 |
| 50 | 51 | IOA11 | - | I/O | - | IOA11 |
| 51 | 52 | IOA12 | - | I/O | - | IOA12 |
| 52 | 53 | IOA13 | - | I/O | - | IOA13 |
| 53 | 54 | IOA14 | - | I/O | - | IOA14 |
| 54 | 55 | IOA15 | - | I/O | - | IOA15 |
| 55 | 56 | IOC8 | SD2 | I/O | SD2 data0 | IOC8 |
| 56 | 57 | IOC7 | SD2 | I/O | SD2 clock | IOC7 |
| 57 | 58 | IOC6 | SD2 | I/O | SD2 command | IOC6 |
| 58 | 59 | IOC10 | SD2 | I/O | SD2 data2 | IOC10 |
| 59 | 60 | IOC9 | SD2 | I/O | SD2 data1 | IOC9 |
| 60 | 61 | IOC5 | SD2 | I/O | SD2 data3 | IOC5 |
| 61 | 62 | IOC11 | Key change A | I/O | Key change A input | IOC11 |
| 62 | 63 | IOC12 | Key change B | I/O | Key change B input | IOC12 |
| 63 | 64 | PLLV33 | PLL | PWR | 3.3V PLL power | |
| 64 | 65 | X32KO | PLL | O | 32768Hz crystal output pin | |
| 65 | 66 | X32KI | PLL | I | 32768Hz crystal input pin | |

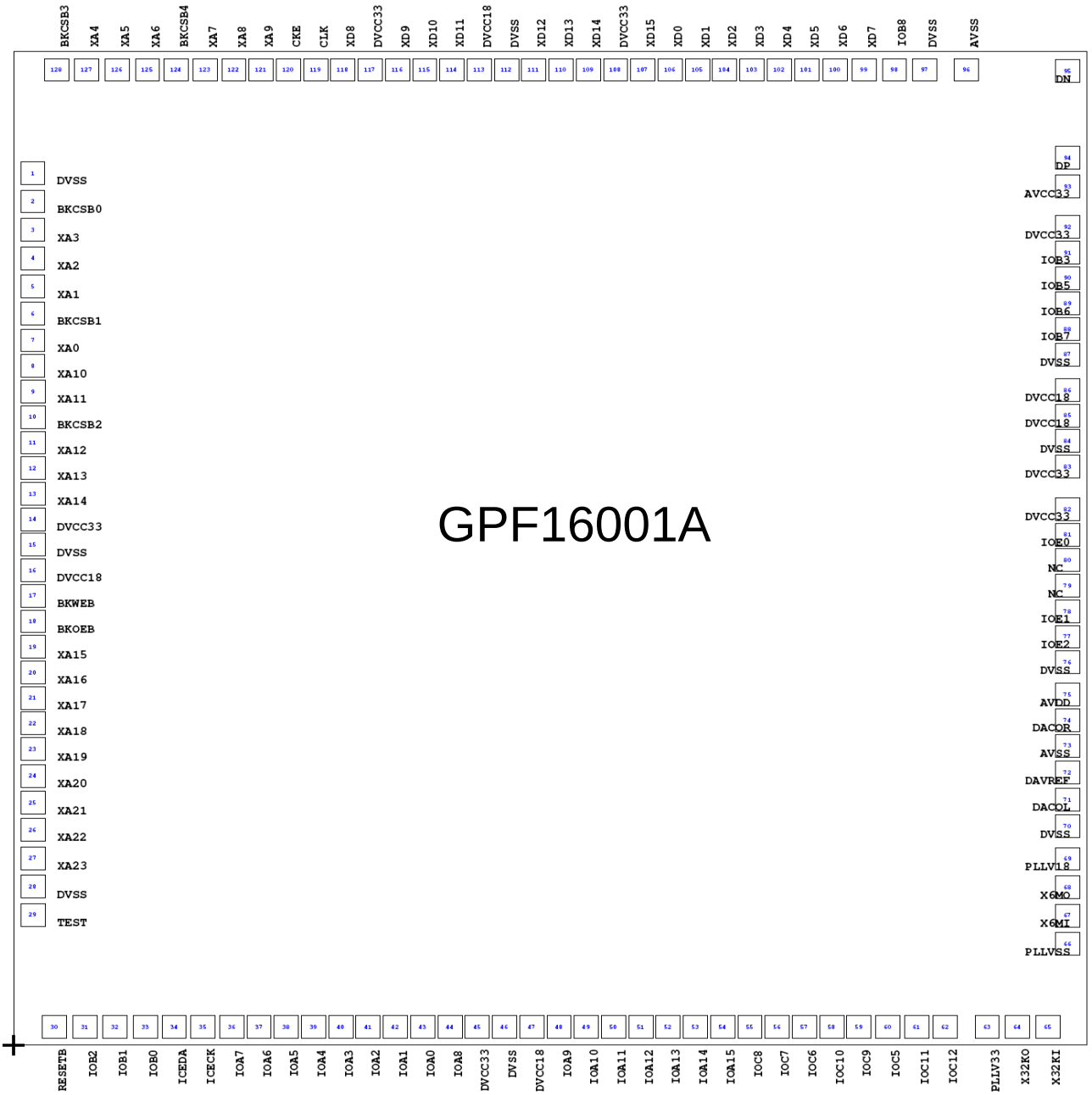
Right Side

| No | Package No | Name | Group | Type | Normal Function Description | GPIO Group |
|---|---|---|---|---|---|---|
| 66 | 67 | PLLVSS | PLL | PWR | PLL ground | |
| 67 | 68 | X6MI | PLL | A/I | 6MHz crystal input pin or 12M PLL filter pin | |
| 68 | 69 | X6MO | PLL | O | 6MHz crystal output pin | |
| 69 | 70 | PLLV18 | PLL | P | 1.8V power for PLL | |
| 70 | 71 | DVSS | Digital GND | PWR | Digital ground | |
| 71 | 72 | DACOL | DAC | A/O | Left channel audio output | |
| 72 | 73 | DAVREF | DAC | A/O | DAC reference voltage pin | |
| 73 | 74 | AVSS | DAC | PWR | DAC ground | |
| 74 | 75 | DACOR | DAC | A/O | Right channel audio output | |
| 75 | 76 | AVDD | DAC | PWR | 3.3V DAC power | |
| 76 | 77 | DVSS | Digital GND | PWR | Digital ground | |
| 77 | 78 | IOE2 | GPIO | I/O | General-purposed I/O E2 | IOE2 |
| 78 | 79 | IOE1 | GPIO | I/O | General-purposed I/O E1 | IOE1 |
| 79 | 80 | NC | | | | |
| 80 | 81 | NC | | | | |
| 81 | 82 | IOE0 | GPIO | I/O | General-purposed I/O E0 | IOE0 |
| 82 | 83 | DVCC33 | Digital PWR | PWR | 3.3V digital power | |
| 83 | 84 | DVCC33 | Regulator | PWR | 3.3V Regulator power | |
| 84 | 85 | DVSS | Regulator | PWR | Regulator ground | |
| 85 | 86 | DVCC18 | Regulator | A/O | Regulator 1.8V output | |
| 86 | 87 | DVCC18 | Digital PWR | PWR | 1.8V digital power | |
| 87 | 88 | DVSS | Digital GND | PWR | Digital ground | |
| 88 | 89 | IOB7 | SPI | I/O | SPIRX: SPI data input | IOB7 |
| 89 | 90 | IOB6 | SPI | I/O | SPITXD: SPI data output | IOB6 |
| 90 | 91 | IOB5 | SPI | I/O | SPICLK: SPI clock | IOB5 |
| 91 | 92 | IOB3 | - | I/O | - | IOB3 |
| 92 | 93 | DVCC33 | Digital PWR | PWR | 3.3V digital power | |
| 93 | 94 | AVCC33 | USB | PWR | 3.3V USB power | |
| 94 | 95 | DP | USB | I/O | DP pin of USB PHY | |
| 95 | 96 | DN | USB | I/O | DN pin of USB PHY | |

Top Side

| No | Package No | Name | Group | Type | Normal Function Description | GPIO Group |
|---|---|---|---|---|---|---|
| 96 | 97 | AVSS | USB | PWR | USB ground | |
| 97 | 98 | DVSS | Digital GND | PWR | Digital ground | |
| 98 | 99 | IOB8 | EINT | I/O | External INT0 | IOB8 |
| 99 | 100 | XD7 | Memory I/F | I/O | External memory data pin 7 | |
| 100 | 101 | XD6 | Memory I/F | I/O | External memory data pin 6 | |
| 101 | 102 | XD5 | Memory I/F | I/O | External memory data pin 5 | |
| 102 | 103 | XD4 | Memory I/F | I/O | External memory data pin 4 | |
| 103 | 104 | XD3 | Memory I/F | I/O | External memory data pin 3 | |
| 104 | 105 | XD2 | Memory I/F | I/O | External memory data pin 2 | |
| 105 | 106 | XD1 | Memory I/F | I/O | External memory data pin 1 | |
| 106 | 107 | XD0 | Memory I/F | I/O | External memory data pin 0 | |
| 107 | 108 | XD15 | Memory I/F | I/O | External memory data pin 15 | |
| 108 | 109 | DVCC33 | Digital PWR | PWR | 3.3V digital power | |
| 109 | 110 | XD14 | Memory I/F | I/O | External memory data pin 14 | |
| 110 | 111 | XD13 | Memory I/F | I/O | External memory data pin 13 | |
| 111 | 112 | XD12 | Memory I/F | I/O | External memory data pin 12 | |
| 112 | 113 | DVSS | Digital GND | PWR | Digital ground | |
| 113 | 114 | DVCC18 | Digital PWR | PWR | 1.8V digital power | |
| 114 | 115 | XD11 | Memory I/F | I/O | External memory data pin 11 | |
| 115 | 116 | XD10 | Memory I/F | I/O | External memory data pin 10 | |
| 116 | 117 | XD9 | Memory I/F | I/O | External memory data pin 9 | |
| 117 | 118 | DVCC33 | Digital PWR | PWR | 3.3V digital power | |
| 118 | 119 | XD8 | Memory I/F | I/O | External memory data pin 8 | |
| 119 | 120 | CLK | SDRAM | I/O | SDRAM clock | IOC0 |
| 120 | 121 | CKE | SDRAM | I/O | SDRAM clock enable | IOC1 |
| 121 | 122 | XA9 | Memory I/F | I/O | External memory address pin 9 | |
| 122 | 123 | XA8 | Memory I/F | I/O | External memory address pin 8 | |
| 123 | 124 | XA7 | Memory I/F | I/O | External memory address pin 7 | |
| 124 | 125 | BKCSB4 | Memory I/F | I/O | External memory chip select 4 | IOD4 |
| 125 | 126 | XA6 | Memory I/F | I/O | External memory address pin 6 | |
| 126 | 127 | XA5 | Memory I/F | I/O | External memory address pin 5 | |
| 127 | 128 | XA4 | Memory I/F | I/O | External memory address pin 4 | |
| 128 | 1 | BKCSB3 | Memory I/F | I/O | External memory chip select 3 | IOD3 |

### 4.1. PAD Assignment

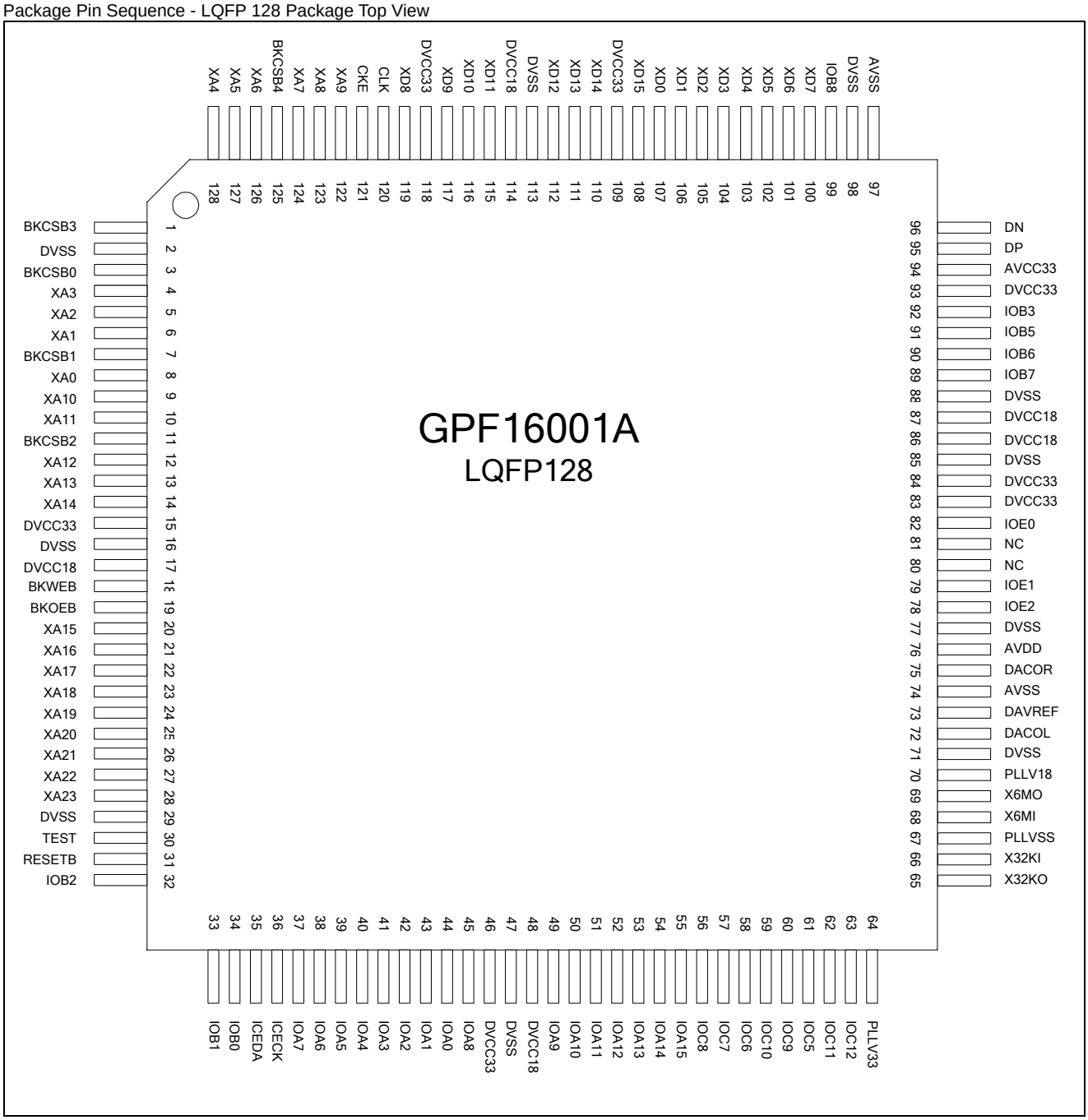



This IC substrate should be connected to VSS

**Note1:** To ensure that the IC functions properly, please bond all of VDD and VSS pins.
**Note2:** The 0.1μF-capacitor between VDD and VSS should be placed to IC as close as possible.

### 4.2. Pin Map

Package Pin Sequence - LQFP 128 Package Top View



## 5. FUNCTIONAL DESCRIPTIONS

### 5.1. CPU

The GPF16001A is equipped with a 16-bit *μ'nSP*™ 2.0, the newest 16-bit microprocessor by SUNPLUS and pronounced as *micro-n-SP*. Sixteen registers are involved in *μ'nSP*™ 2.0: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and R8 - R15 (General-purpose register). The interrupts include three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), and one software-interrupt, BREAK. GPF16001A is also built-in a 4K-byte I-cache which can increase the performance significantly.

### 5.2. Memory

#### 5.2.1. Internal SRAM

The amount of SRAM is 12K-word (including Stack), ranged from 0x0000 through 0x2FFF with access speed of one CPU clock. Since this SRAM is located in CPU's local bus, system bus will not be occupied when this SRAM is accessed by CPU. This SRAM can be accessed freely by CPU/DMA /LCD.

#### 5.2.2. External memory

The memory is separated into five banks; each bank can be up to 256 pages, and each page is 64K words. The controller supports up to 80M words NOR flash memories. Each bank can be programmed as SDRAM/ ROM/ SRAM/NOR Flash. GPF16001A can support up-to 64M bytes (512Mb) SDRAM with single chip-selection.

### 5.3. PLL, Clock, Power Mode

#### 5.3.1. PLL (Phase Lock Loop)

There are three PLLs embedded in GPF16001A. The 1st PLL can pump up to 96MHz, 2nd PLL to 27MHz, and 3rd PLL to 12MHz. The output frequency of fast PLL is programmable and ranged from 15MHz ~ 96MHz (3MHz per step).

#### 5.3.2. System clock

The system clock can be selected from 32768Hz, 12MHz or 6MHz (determined by fast PLL's output frequency) by register implementation. Furthermore, a clock divider which can divide clock up to 1/128 is featured to reduce power consumption.

### 5.4. Power Savings Mode

The GPF16001A offers four power modes: Normal, Wait, Halt and Sleep.

| Mode | CPU | System | RTC | POWEREN | After wakeup |
|---|---|---|---|---|---|
| Normal | ON | ON | ON | ON | - |
| Wait | OFF | ON | ON | ON | Next Instruction |
| Halt | OFF | OFF | ON | OFF | Reset CPU |
| Halt2 | OFF | OFF | ON | OFF | Next Instruction |
| Sleep | OFF | OFF | OFF | OFF | Reset System |

Enter the Wait/Halt/Halt2/Sleep mode, is done by write designated value to designated port. The wake-up source includes interrupt, timer or key-change state

### 5.5. Sound Process Unit

GPF16001A equips a 16-channel SPU. Each channel supports PCM8/PCM16/ADPCM36. A dynamic volume compressor is also embedded to enlarge the overall volume. For software application, GPF16001A is also capable of wide-band (sample rate >= 16kHz) low bit-rate algorithm.

### 5.6. STN-LCD Interface

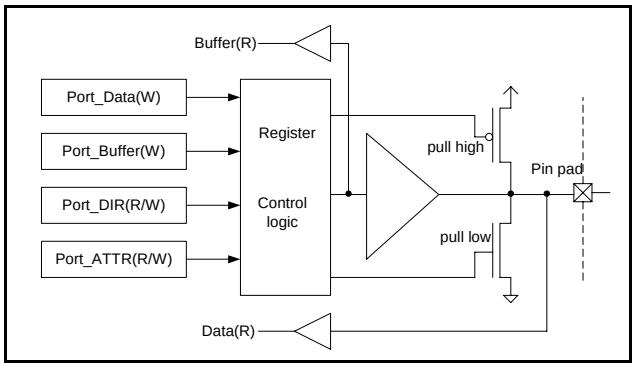
The STN-LCD driver interface built-in GPF16001A supports up to 320X240 LCD panel and it supports 1bit/4-bit data bus in monochrome/gray-scale STN.

### 5.6. Interrupt

The GPF16001A has 29 interrupt sources, grouped into two types: FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt while IRQ is the low-priority one. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources. Some of the interrupt sources can be programmed as FIQ or IRQ by register setting.

### 5.7. GPIO

Five I/O ports are built in GPF16001A: IOA, IOB, IOC, IOD and IOE. Each I/O pin has its normal function and is described in the signal description section. When the normal function of an I/O is disabled, it will switch to GPIO function automatically. The following diagram is a GPIO schematic.




### 5.8. Timer / Counter

The GPF16001A provides six 16-bit timers/counters, TimerA to TimerF. The clock source of each timer can be set individually. For Timer A to TimerD, an INT will be sent to CPU when timer overflows. Besides, Capture, Comparison and PWM functions are also provided by TimerA/TimerB/TimerC.

| Clock Source A | Clock Source B |
|---|---|
| Fosc/2 | 2048Hz |
| Fosc/256 | 1024Hz |
| 32768Hz | 256Hz |
| 8192Hz | Time Base B |
| 4096Hz | Time Base A |
| 1 | 0 |
| Another Timer | 1 |
| INT1 | INT2 |

The GPF16001A is embedded with a timebase controller which is used to generate the slow and precisely interrupt form 32768Hz crystal. The following table shows the available time-base.

| TimeBase A | TimeBase B | TimeBase C |
|---|---|---|
| -- | 8Hz | 128Hz |
| 1Hz | 16Hz | 256Hz |
| 2Hz | 32Hz | 512Hz |
| 4Hz | 64Hz | 1024Hz |

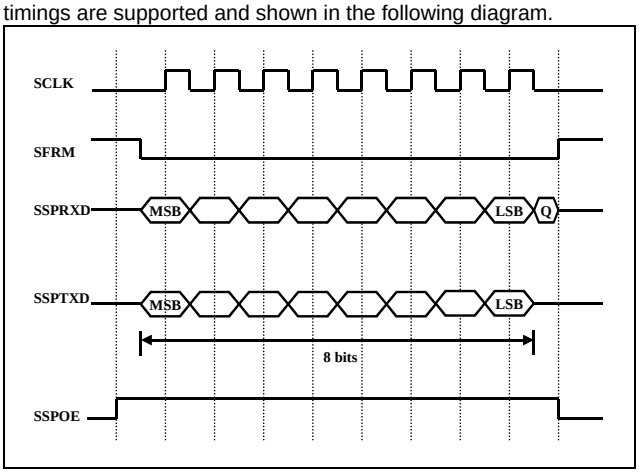
### 5.9. Watchdog

The purpose of watchdog is to monitor if the system operates normally. Within a certain period, watchdog must be cleared. If not, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GPF16001A, the clear period is software programmable. If watchdog is cleared before expiration, the system will not be reset.

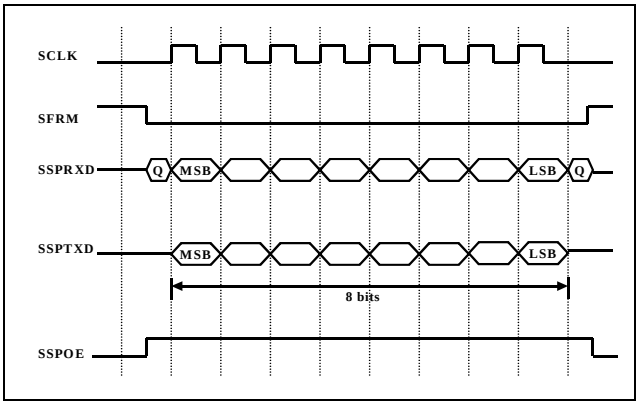
### 5.10. Serial Interface

#### 5.10.1. Serial Peripheral Interface (SPI)

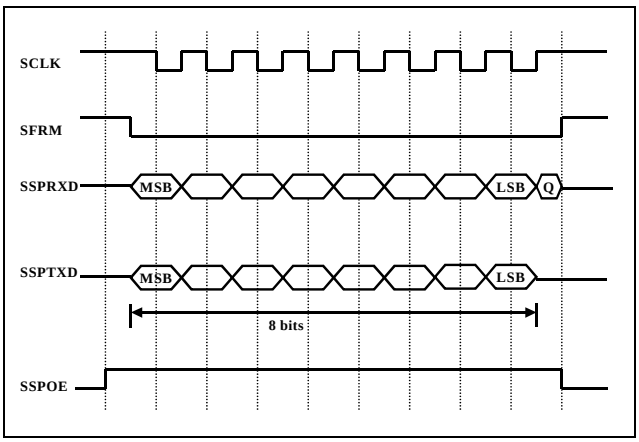
The SPI interface is a master interface that enables synchronous serial communication with slave/master peripherals. Two 8-byte FIFOs are used for transmitting and receiving data. Four types of timings are supported and shown in the following diagram.



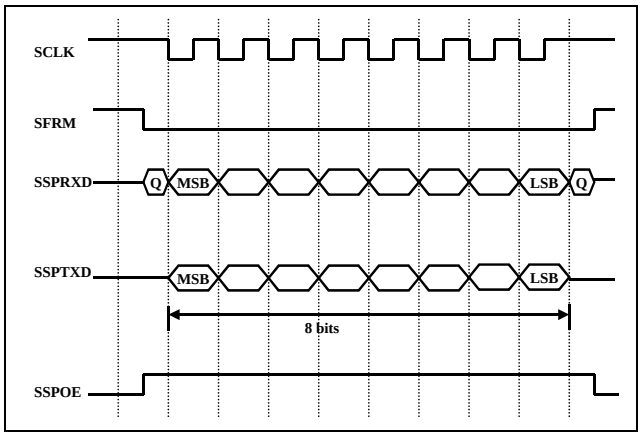

SPO = 0, SPH = 0




SPO = 0, SPH = 1




SPO = 1, SPH = 0




SPO = 1, SPH = 1

### 5.10.2. USB Device Function

GPF16001A provides USB device function which is compatible with USB 1.1 and USB 2.0 full speed standard. An USB transceiver is built-in for device function. A FIFO with size of 128x8 is used for bulk-in and bulk-out transfer and an 8-byte FIFO is used for pipe transferring control. Interrupt IN/OUT pipes are also supported. The DMA transfer is enabled for bulk-in/out to optimize the transferring performance.

### 5.11. IDE Tools Function

The functions of IDE include the following:
1). C compiler, Assembly and Linker
2). Single step trace
3). Break point (break point for debugging)
4). Run (execute)

### 5.12. SD/MMC Controller

GPF16001A provides SD/MMC controllers which is compatible with MMC system specification version 2.3 and SD Memory Card specification 1.1. The controller supports automatic CRC generation and check, 1-bit and 4-bit transfer, interrupt generation when buffer empty/full, DMA transfer for page read/write.

### 5.13. Real Time Clock (RTC)

The RTC block provides the alarm function, schedule function, and hour/minute/second/half-second interrupt function.

### 5.14. Analog Control

#### 5.14.1. DAC control

A 16-bit stereo DAC (2ch) is embedded in GPF16001A. For both left and right channel, a 16x16 FIFO is used to prevent the sound glitch when CPU is busy. The left and right channels are not necessarily having the same sample rate. A single DMA channel can utilize the stereo playback.

## 6. ELECTRICAL SPECIFICATIONS

### 6.1. Absolute Maximum Rating

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage 1 | DVCC33<br>PLL_V33 | -0.3 to 4.0 | V |
| Supply Voltage 2 | AVDD | -0.3 to 4.0 | V |
| Supply Voltage 3 | DVCC18<br>PLL_V18 | -0.3 to 2.16 | V |
| Input Voltage | $V_{IN}$ | -0.3 to 4.0 | V |
| Operating Temperature | $T_A$ | 0 to 70 | ℃ |
| Storage Temperature | $T_{STG}$ | -40 to +150 | ℃ |

### 6.2. DC Characteristics

| Characteristic | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage 1 | DVCC33<br>PLL_V33 | 2.7<br>3.0[1] | 3.0 | 3.6 | V | - |
| Operating Voltage 2 | AVDD | 2.7 | 3.0 | 3.3 | V | - |
| Operating Voltage 3 | DVCC18<br>PLL_V18 | 1.62 | 1.8 | 1.98 | V | - |
| Operating Current | $I_{OP}$ | - | 60[2] | - | mA | @96MHz, 3.3V, all clocks on |
| Power Down Current | $I_{PD}$ | - | 25[3] | 30[3] | μA | Sleep Mode@1.5V |
| Halt Mode Current | $I_{HM}$ | - | 30[4] | 35[4] | μA | Halt Mode@1.5V |
| High Input Voltage | $V_{IH}$ | 0.7DVDD33 | - | DVDD33 | V | - |
| Low Input Voltage | $V_{IL}$ | VSS | - | 0.8 | V | - |
| Crystal Frequency 1 | - | - | 32768 | - | Hz | - |
| Crystal Frequency 2 | $F_{CRYSTAL}$ | - | 6.0[5] | - | MHz | - |
| System Clock | $F_{SYS}$ | 256Hz[6] | 48 | 96 | MHz | - |

**Note1:** When USB function is enabled, the minimum voltage of DVCC33 is 3.0V.

**Note2:** Operating current depends on software code. In this test case, the following macro is turned on: Audio DAC, 96MHz PLL and 27MHz PLL.

**Note3:** Regulator is in sleep mode.

**Note4:** Regulator is in sleep mode. Use only 32KHz crystal,;6MHz crystal is disabled.

**Note5:** 6MHz Crystal is required when USB function or TV function is enabled.

**Note6:** By setting clock divider and changing system clock to 32768Hz mode.

### 6.3. Audio DAC Characteristics

| Characteristic | Limits | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Resolution | - | 16 | - | Bit | - |
| Full Scale Output Voltage | - | 0.6*VDDDA | - | Vp-p | - |
| THD+N (f = 1kHz) | - | 0.1 | - | % | - |
| Noise at No Signal | -85 | 90 | - | dBv | - |
| Frequency Response | 20 | - | 19200 | Hz | - |

### 6.4. Regulator Characteristics

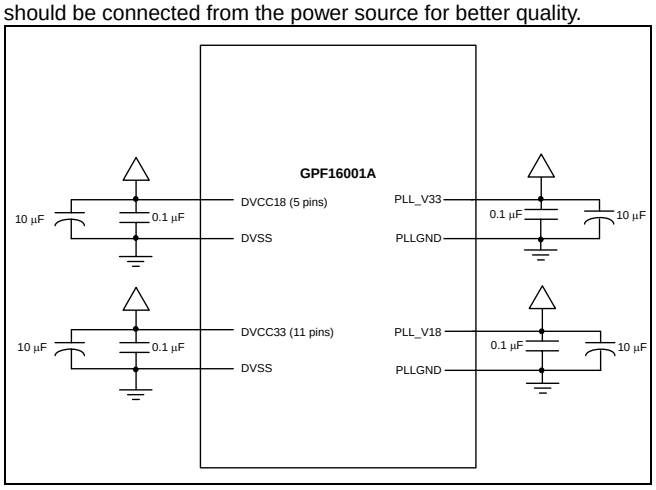
| Characteristics | Symbol | Unit | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Input Voltage | VREGI | 2.7 | 3.0 | 3.6 | V |
| Maximum Current Output | IREGO | - | 70 | 100 | mA |
| Output Voltage | VREGO | 1.5[1] | 1.8 | 1.89 | V |
| Standby Current | IREGS | - | 10 | - | - |

**Note1:** To save more power, it is recommended switching to 1.5V before entering the halt/sleep mode and switching to 1.8V in normal operation mode.

## 7. RECOMMENDED BOARD LAYOUT

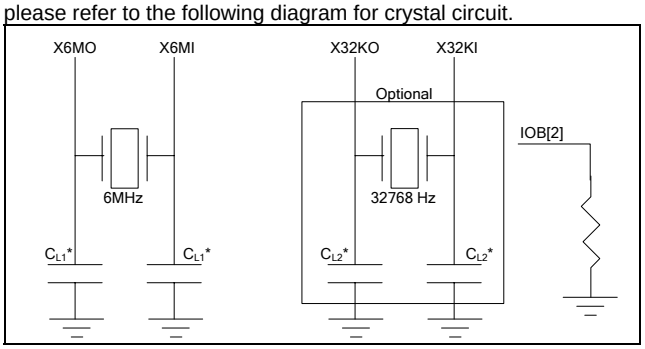
### 7.1. Power and Ground

All digital power and ground should be connected. The decoupling capacitor of 0.1μF and 10μF should be connected to each power pin of the IC as the following diagram. The power of analog parts should be connected from the power source for better quality.



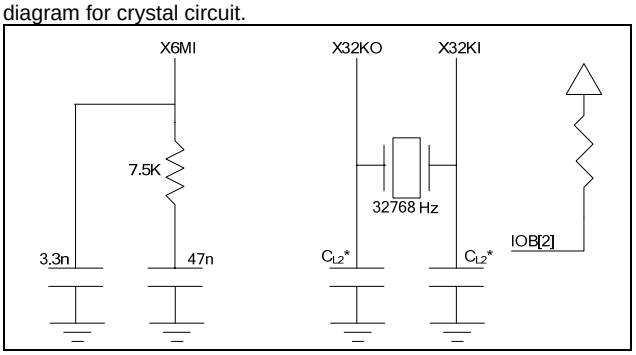

### 7.2. Crystal and PLL

When the 32768Hz crystal is disabled, usually for USB application, please refer to the following diagram for crystal circuit.




**Note*:** Please refer to the crystal's application circuit.

When the 6MHz crystal is disabled, please refer to the following diagram for crystal circuit.




### 7.3. Analog Section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. DAVREF should be connected to a 1μF capacitor.

## 8. ORDERING INFORMATION

### 8.1. Ordering Information

| Product Number | Package Type |
|---|---|
| GPF16001A - NnnV - C | Chip Form |
| GPF16001A - NnnV - QL09x | Halogen Free Package |

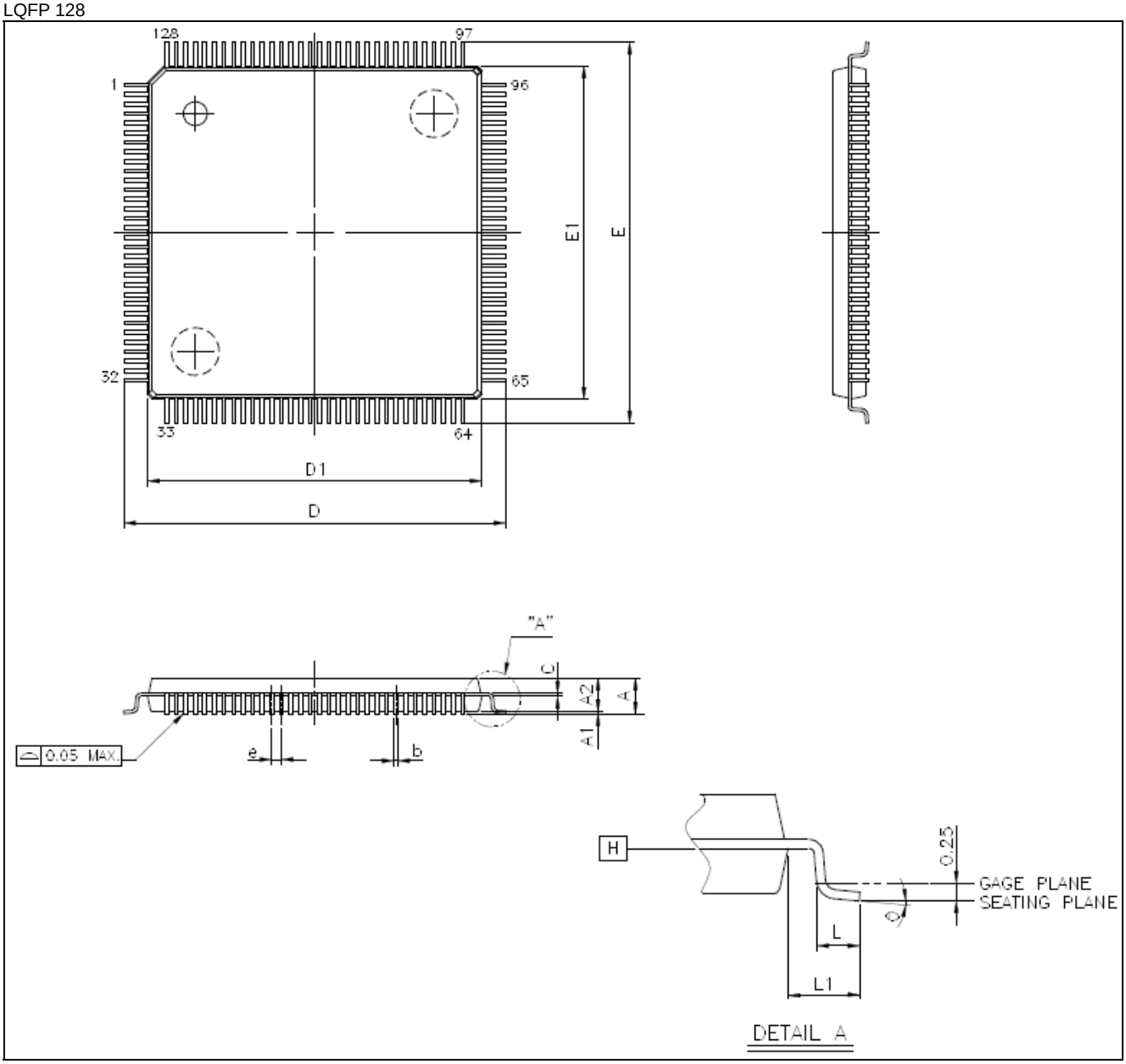
**Note1:** Code number is assigned for customer.

**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

**Note3:** Package form number (x = 1 - 9, serial number).

### 8.2. Package Information

LQFP 128




| Symbol | Millimeter | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | -- | -- | 1.60 |

| Symbol | Millimeter | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.13 | 0.16 | 0.23 |
| C | 0.09 | -- | 0.20 |
| D | 16.00 BSC | | |
| D1 | 14.00 BSC | | |
| E | 16.00 BSC | | |
| E1 | 14.00 BSC | | |
| e | 0.40 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| $\theta$ | 0° | 3.5° | 7° |

## 9. DISCLAIMER

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## 10. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| May 02, 2011 | 0.1 | Preliminary version. | 19 |