16-Bit CCD/CIS Analog Signal Processor

Features

- Operating voltage: 3.3V (typ.)
- Low Power CMOS: 300 mW (typ.)
- Power-Down Mode: 10μA (max.)
- 16-Bit 30 MSPS A/D converter
- Guaranteed won't miss codes
- 1~5.85x programmable gain
- Correlated double sampling
- ±250 mV programmable offset
- Input clamp circuitry
- Internal voltage reference
- Multiplexed byte-wide output (8+8 format)
- Programmable 3-wire serial interface
- 3 .3V digital I/O compatibility
- 3-Channel operation up to 30 MSPS
- 2-Channel (even-odd) operation up to 30 MSPS
- 1-Channel operation up to 20 MSPS
- 28-pin SSOP (209mil) package

Applications

- Flatbed document scanners
- Film scanners
- Digital color copiers
- Multifunction peripherals

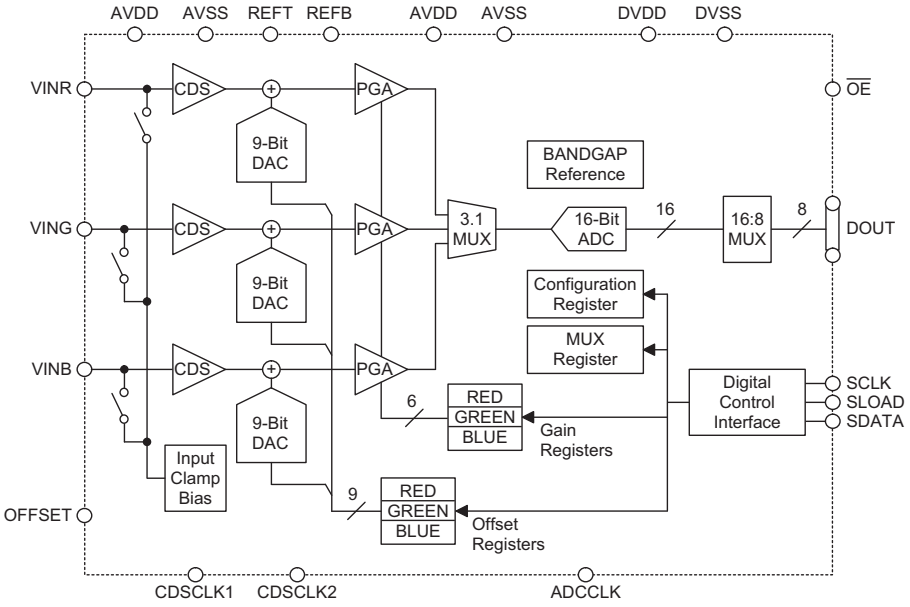
General Description

The HT82V38 is a complete analog signal processor for CCD imaging applications. It features a 3 channel architecture designed to sample and condition the outputs of trilinear color CCD arrays. Each channel consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), multiplexed to a high performance 16-bit A/D converter.

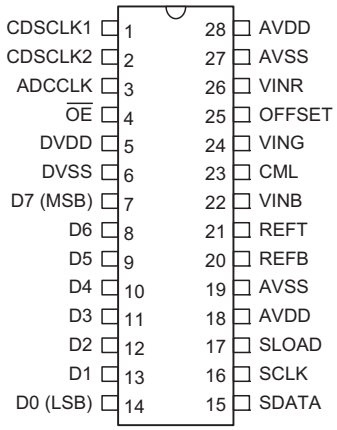
The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS.

The 16-bit digital output is multiplexed into an 8-bit output word that is accessed using two read cycles. The internal registers are programmed through a 3-wire serial interface, and provide adjustment of the gain, offset, and operating mode.

Block Diagram



Pin Assignment



HT82V38
28 SSOP-A

Pin Description

Pin No.	Pin Name	I/O	Description
1	CDSCLK1	DI	CDS Reference Clock Pulse Input
2	CDSCLK2	DI	CDS Data Clock Pulse Input
3	ADCCLK	DI	A/D Sample Clock Input for 3-channels Mode
4	$\overline{OE}$	DI	Output Enable, Active Low Internal pull-low 50kΩ
5	DVDD	P	Digital Power
6	DVSS	P	Digital Ground
7~14	D7~D0	DO	Digital Data Output
15	SDATA	DI/DO	Serial Data Input/Output
16	SCLK	DI	Clock Input for Serial Interface
17	SLOAD	DI	Serial Interface Load Pulse
18, 28	AVDD	P	Analog Supply
19, 27	AVSS	P	Analog Ground
20	REFB	AO	Reference Decoupling
21	REFT	AO	Reference Decoupling
22	VINB	AI	Analog Input, Blue
23	CML	AO	Internal Reference Output
24	VING	AI	Analog Input, Green
25	OFFSET	AO	Clamp Bias Level Decoupling
26	VINR	AI	Analog Input, Red

Note: AI=Analog Input, AO=Analog Output, DI=Digital Input, DO=Digital Output, P=Power

Absolute Maximum Ratings

Supply Voltage .....V_{SS}–0.3V to V_{SS}+4.3V

Input Voltage .....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature .....–50°C to 125°C

Operating Temperature .....0°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Logic Inputs							
V_{IH}	High Level Input Voltage	—	—	$0.8V_{DD}$	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	—	$0.2V_{DD}$	V
I_{IH}	High Level Input Current	—	—	—	—	1	μA
I_{IL}	Low Level Input Current	—	—	—	—	1	μA
C_{IN}	Input Capacitance	—	—	—	5	—	pF
Logic Outputs							
V_{OH}	High Level Output Voltage	—	I_{OH}=3mA	DV_{DD}-0.5	—	—	V
V_{OL}	Low Level Output Voltage	—	I_{OL}=3mA	—	—	0.5	V

A.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Power Supplies							
AV_{DD}	AVDD	—	—	3.15	3.3	3.45	V
DV_{DD}	DVDD	—	—	3.15	3.3	3.45	V
Maximum Conversion Rate							
t_{MAX}	3-channel Mode with CDS	—	—	30	—	—	MPS
	2-channel Mode with CDS	—	—	30	—	—	MPS
	1-channel Mode with CDS	—	—	20	—	—	MPS
Accuracy (Entire Signal Path)							
	ADC Resolution	—	—	—	16	—	Bits
	Integral Nonlinear (INL)	—	—	—	±32	—	LSB
	Differential Nonlinear (DNL)	—	—	–1	—	+1	mV
	Offset Error	—	—	–100	—	+100	mV
	Gain Error	—	—	—	5	—	%FSR

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Analog Inputs							
R_{FS}	Full-scale Input Range	—	—	—	1.6/2.0	—	V
V_i	Input Limits	—	—	AV_{SS}-0.3	—	AV_{DD}+0.3	V
C_i	Input Capacitance	—	—	—	10	—	pF
I_i	Input Current	—	—	—	10	—	μA
Amplifiers							
	PGA Gain at Minimum	—	—	—	1	—	V/V
	PGA Gain at Maximum	—	—	—	5.85	—	V/V
	PGA Gain Resolution	—	—	—	6	—	Bits
	Programmable Offset at Minimum	—	—	—	–250	—	mV
	Programmable Offset at Maximum	—	—	—	250	—	mV
	Offset Resolution	—	—	—	9	—	Bits
Clamp DAC Circuit							
t_A	Clamp DAC resolution	—	—	—	4	—	Bits
	Clamp DAC output voltage at code 0			—	0.45	—	V
	Clamp DAC output voltage at code F			—	2.7	—	V
	Clamp DAC Step size			—	0.15	—	V/Step
	Clamp DAC deviation (AV_{DD}=3.300V)			–50	—	50	mV
Temperature Range							
t_A	Operating	—	—	0	—	70	°C
Power Consumption							
P_{tot}	Total Power Consumption	—	—	—	300	—	mW

Timing Specification AV_{DD}=DRV_{DD}=3.3V, AV_{SS}=DRV_{SS}=0V, Ta=25°C, ADCCLK=30MHz unless otherwise stated

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock Parameters					
t_{PRA}	3-Channel Pixel Rate	100	—	—	ns
t_{PRB}	2-Channel Pixel Rate	66	—	—	ns
t_{PRC}	1-Channel Pixel Rate	50	—	—	ns
t_{ADCLK}	ADCCLK Pulse Width	16	—	—	ns
t_{C1}	CDSCLK1 Pulse Width	10	—	—	ns
t_{C2}	CDSCLK2 Pulse Width	10	—	—	ns
t_{C1C2}	CDSCLK1 Falling to CDSCLK2 Rising	0	—	—	ns
t_{ADC2}	ADCCLK Falling to CDSCLK2 Rising	2	—	—	ns
t_{C2ADR}	CDSCLK2 Rising to ADCCLK Rising	2	—	—	ns
t_{C2ADF}	CDSCLK2 Falling to ADCCLK Falling	20	—	—	ns
t_{C2FADR}	CDSCLK2 Falling to ADCLK Rising	4	—	—	ns
t_{ADC1}	ADCCLK Falling to CDSCLK1 Rising	0	—	—	ns
t_{AD}	Aperture Delay for CDS Clocks	—	3	—	ns

Symbol	Parameter	Min.	Typ.	Max.	Unit
Serial Interface					
f_{SCLK}	Maximum SCLK Frequency	—	—	10	MHz
t_{LS}	SLOAD to SCLK Setup Time	10	—	—	ns
t_{LH}	SCLK to SLOAD Hold Time	10	—	—	ns
t_{DS}	SDATA to SCLK Rising Setup Time	10	—	—	ns
t_{DH}	SCLK Rising to SDATA Hold Time	10	—	—	ns
t_{RDV}	SCLK Falling to SDATA Valid	10	—	—	ns
Data Output					
t_{OD}	Output Delay (output load 10pF)	—	10	—	ns
t_{HZ}	Output Enable High to 3-State	—	10	—	ns
t_{DV}	3-State to Data Valid	—	10	—	ns
	Latency (Pipeline Delay)	—	9	—	Cycles

Functional Description

Integral Nonlinear (INL)

Integral nonlinearity error refers to the deviation of each individual code from a line drawn from ″zero scale″ through ″positive full scale″. The point used as ″zero scale″ occurs 1/2 LSB before the first code transition. ″Positive full scale″ is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinear (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 16-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

Offset Error

The first ADC code transition should occur at a level 1/2 LSB above the nominal zero scale voltage. The offset error is the deviation of the actual first code transition level from the ideal level.

Gain Error

The last code transition should occur for an analog value 1/2 LSB below the full-scale voltage (2×(REFT−REFB)). Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

Aperture Delay

The aperture delay is the time delay that occurs from when a sampling edge is applied to the HT82V38 until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low, so the aperture delay is measured from each clock's falling edge to the instant the actual internal sample is taken.

Internal Register Descriptions

Register Name	Address			Data Bits								
	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	0	0	Clamp Int	3 CH	CDS on	0	Pwr Dn	Full scale input range	1byte out
MUX	0	0	1	0	RGB/ BGR	Red	Green	Blue	ClapC[3]	ClapC[2]	ClapC[1]	ClapC[0]
Red PGA	0	1	0	0	0	0	MSB					LSB
Green PGA	0	1	1	0	0	0	MSB					LSB
Blue PGA	1	0	0	0	0	0	MSB					LSB
Red Offset	1	0	1	MSB								LSB
Green Offset	1	1	0	MSB								LSB
Blue Offset	1	1	1	MSB								LSB

Internal Register Map

Configuration Register

The Configuration Register controls the HT82V38′s operating mode and bias levels. Bits D6 controls reference clamp voltage. Setting this bit low change OFFSET to high-Z, allowing OFFSET to be driven from external power source. Bit D5 will configure the HT82V38 for the 3-Channel (high) mode of operation. Setting Bit D4 high will enable the CDS mode of operation, and setting this bit low will enable the SHA mode of operation. Bit D3 should always be set low. Bit D2 controls the power-down mode. Setting Bit D2 high will place the HT82V38 into a very low power ″sleep″ mode. All register contents are retained while the HT82V38 is in the powered-down state. Bit D1 controls full-scale input range. D1=1, full scale input range will be 2V, D1=0 full scale input range will be 1.6V. Bit D0 controls the output mode of the HT82V38. Setting bit D0 high will enable a single byte output mode where only 8 MSBs of the 16-bit ADC will be output. If bit D0 is set low, then the 16-bit ADC output is multiplexed into two bytes.

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	ClampInt	3 Channels	CDS operation	—	Power-down	Full scale input range	1 byte out
		1=Internal*	1=On*	1=CDS mode*	—	1=On	1=2V	1=On
		0=External	0=Off	0=SHA mode	0*	0=Off (Normal)*	0=1.6V*	0=Off *

Note: * Power-on default value

Configuration Register Settings

MUX Register

The MUX Register controls the sampling channel order in the HT82V38. Bits D8 should always be set low. Bit D7 is used when operating in 3-Channel Mode. Setting Bit D7 high will sequence the MUX to sample the red channel first, then the green channel, and then the blue channel. When in this mode, the CDSCLK2 rising edge always resets the MUX to sample the red channel first (see Timing Figure). When Bit D7 is set low, the channel order is reversed to blue first, green second, and red third. The CDSCLK2 rising edge pulse will always reset the MUX to sample the blue channel first. Bits D6, D5, and D4 are used when operating in 1-Channel Mode. Bit D6 is set high to sample the red channel. Bit D5 is set high to sample the green channel. Bit D4 is set high to sample the blue channel. The MUX will remain stationary during 1-Channel Mode. Bit D3 to Bit D0 control 4 bits DAC clamp voltage from 0.45V to 2.7V.

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	3-Channel	1-Channel	1-Channel	1-Channel	Clap[3]	Clap[2]	Clap[1]	Clap[0]
	1=R-G-B* 0=B-G-R	1=RED* 0=Off	1=GREEN 0=Off*	1=BLUE 0=Off *	1111=2.7V* 1110=2.55V : : 0001=0.6V 0000=0.45V			

Note: * Power-on default value

MUX Register Settings

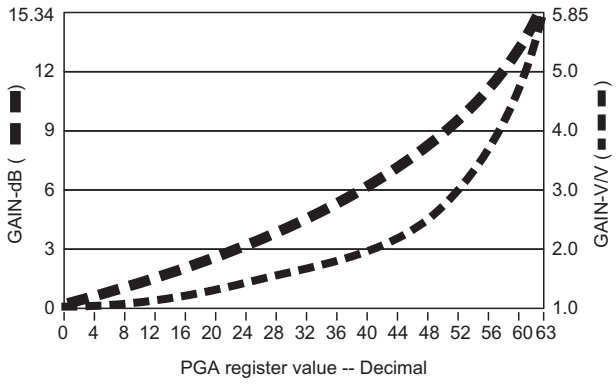
PGA Gain Register

There are three PGA registers for individually programming the gain in the red, green, and blue channels. Bits D8, D7, and D6 in each register must be set low, and bits D5 through D0 control the gain range in 64 increments. See Figure for a graph of the PGA Gain versus PGA register code. The coding for the PGA registers is straight binary, with an all ″zeros″ word corresponding to the minimum gain setting (1x) and an all ″ones″ word corresponding to the maximum gain setting (5.85x).

The PGA has a gain range from 1×(0dB) to 5.85×(15.3dB), adjustable in 64 steps. The Figure shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately linear in dB, the gain in V/V varies in non-linear proportion with the register code, according to the following the equation:

$$\text{Gain} = \frac{76}{76 - G}$$

Where ″G″ is the decimal value of the gain register contents, and varies from 0 to 63.



PGA Gain Transfer Function

D8	D7	D6	D5	D4	D3	D2	D1	D0	Gain (V/V)	Gain (dB)
Set to 0	Set to 0	Set to 0	MSB					LSB		
0	0	0	0	0	0	0	0	0*	1.0	0.0
0	0	0	0	0	0	0	0	1	1.013	0.11
					:				:	:
0	0	0	1	1	1	1	1	0	5.43	14.7
0	0	0	1	1	1	1	1	1	5.85	15.34

Note: * Power-on default value

PGA Gain Register Settings

Offset Register

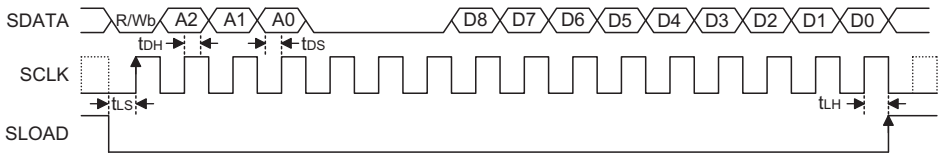
There are three PGA registers for individually programming the offset in the red, green, and blue channels. Bits D8 through D0 control the offset range from −250mV to +250mV in 512 increments. The coding for the offset registers is sign magnitude, with D8 as the sign bit. Table shows the offset range as a function of the Bits D8 through D0.

D8	D7	D6	D5	D4	D3	D2	D1	D0	Offset (mV)
MSB								LSB	
0	0	0	0	0	0	0	0	0*	0
0	0	0	0	0	0	0	0	1	+0.98
					:				:
0	1	1	1	1	1	1	1	1	+250
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	−0.98
					:				:
1	1	1	1	1	1	1	1	1	−250

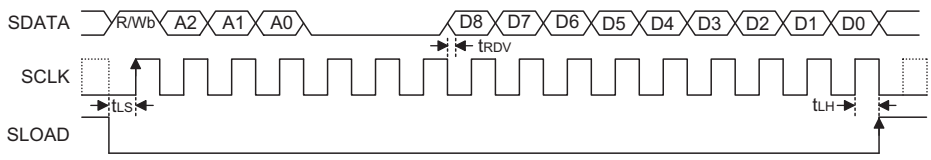
Note: * Power-on default value

Offset Register Settings

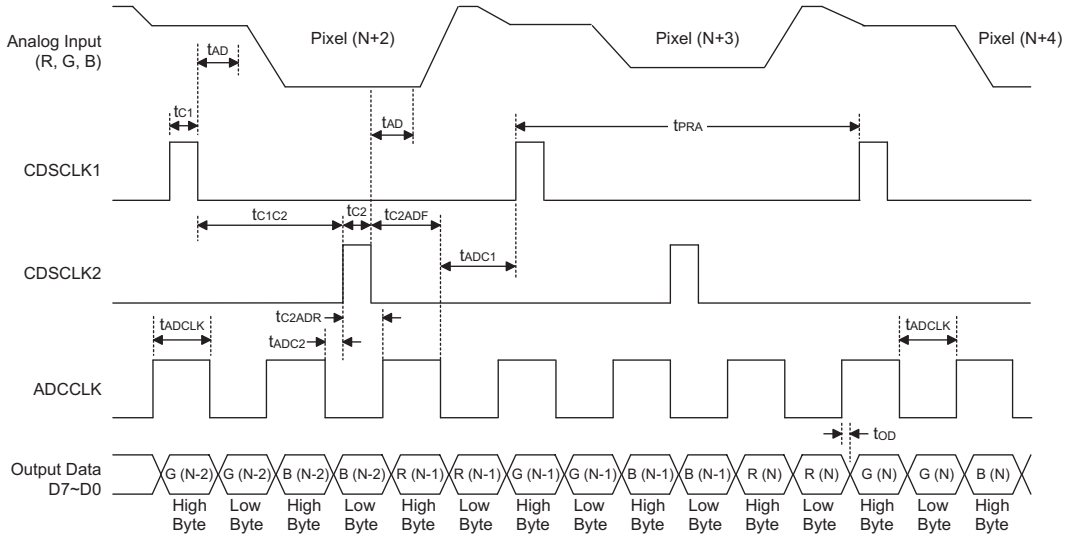
Timing Diagrams



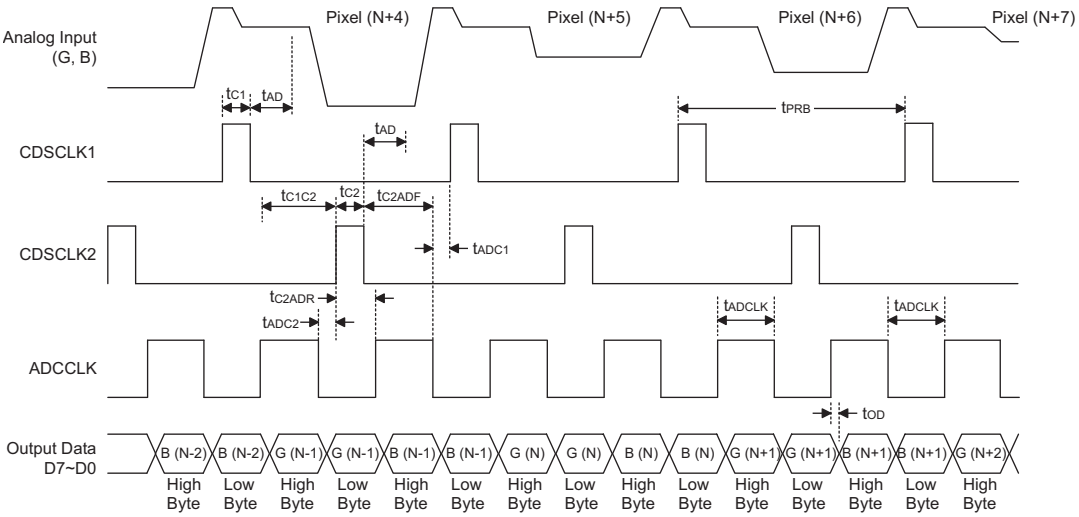
Serial Write Operation Timing



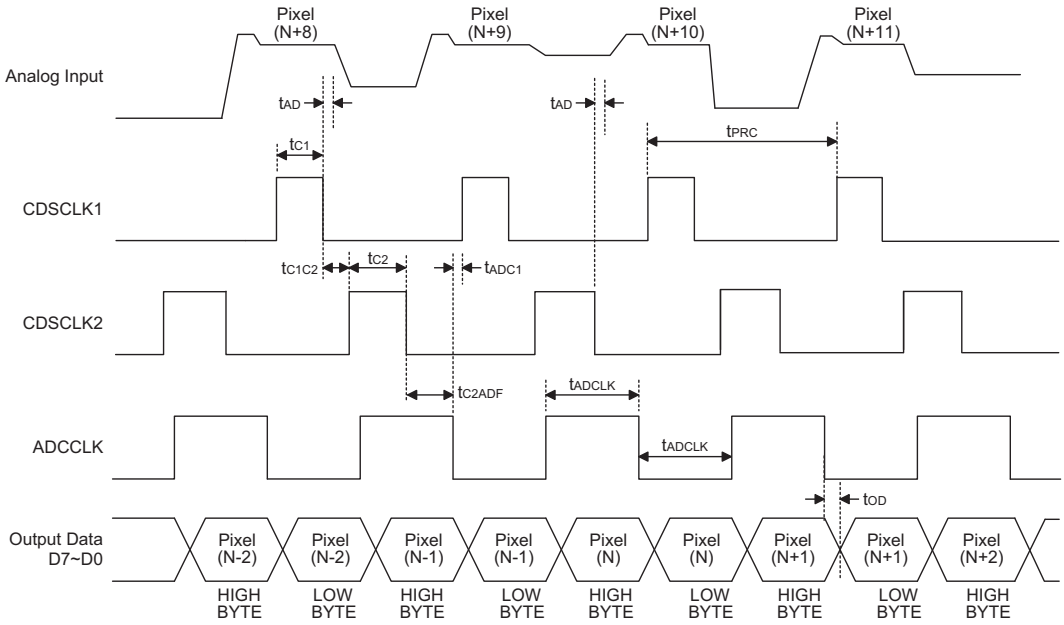
Serial Read Operation Timing



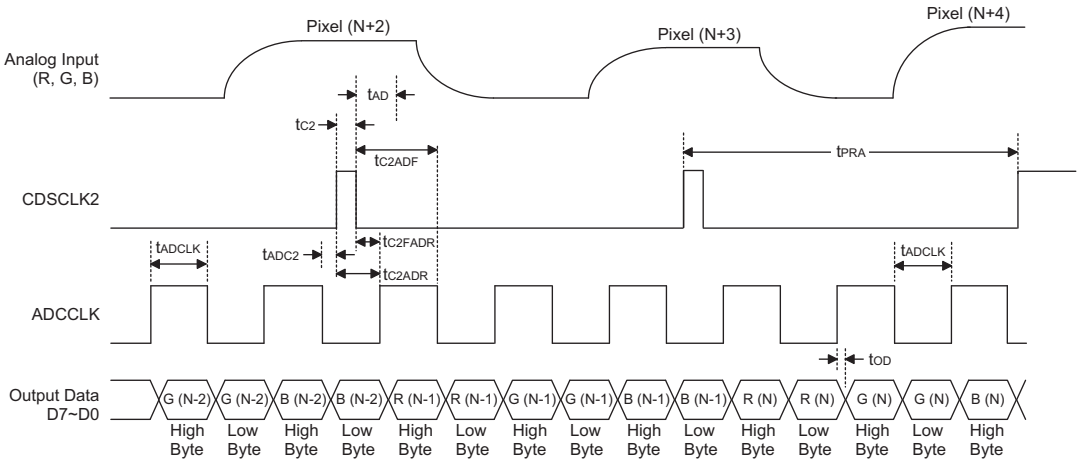
3-Channel CCD Mode Timing (select R-G-B mode)



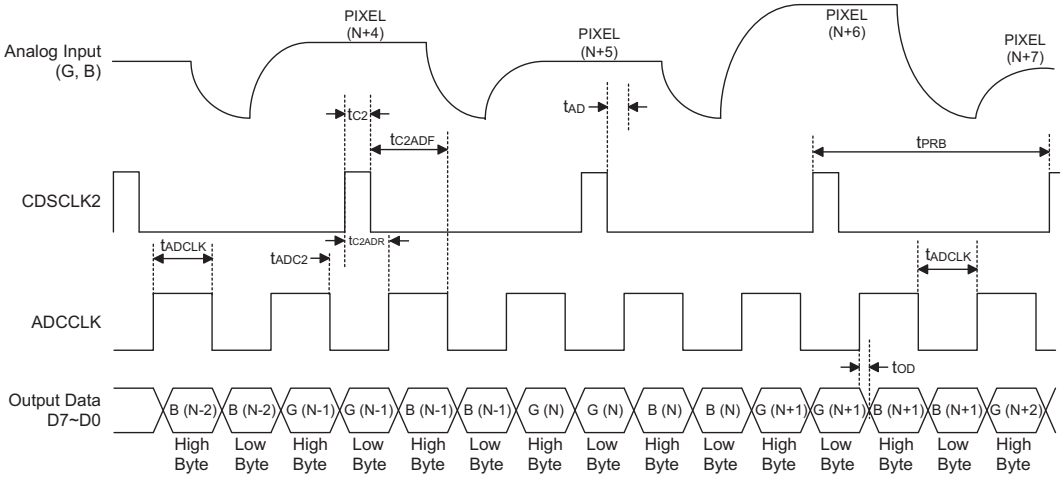
2-Channel CCD Mode Timing (select G-B mode)



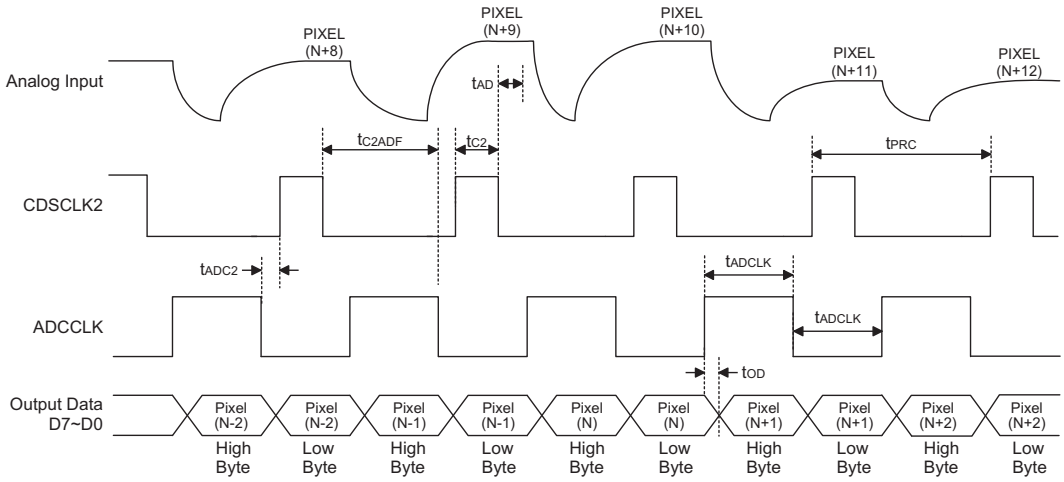
1-Channel CCD Mode Timing



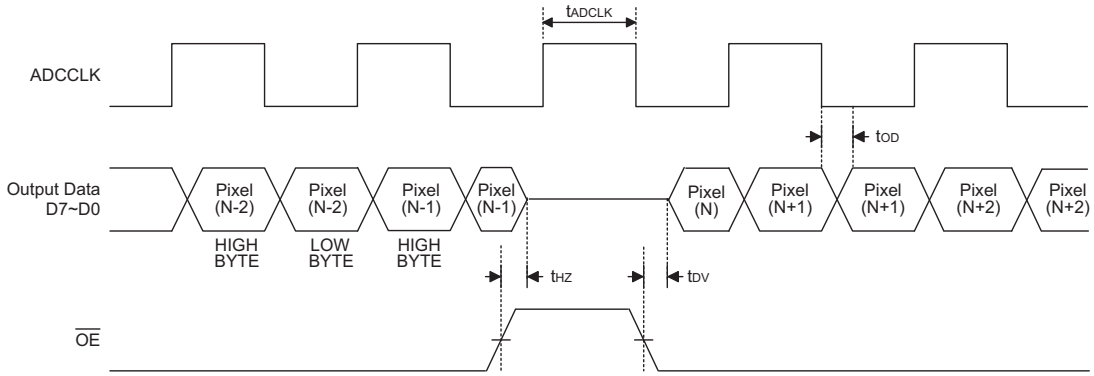
3-Channel SHA Mode Timing (select R-G-B mode)



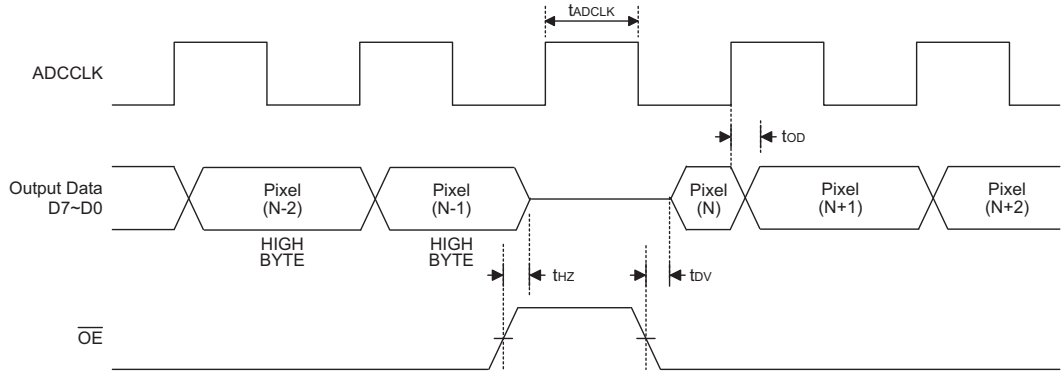
2-Channel SHA Mode Timing (select G-B mode)



1-Channel SHA Mode Timing



Digital Data Output Timing

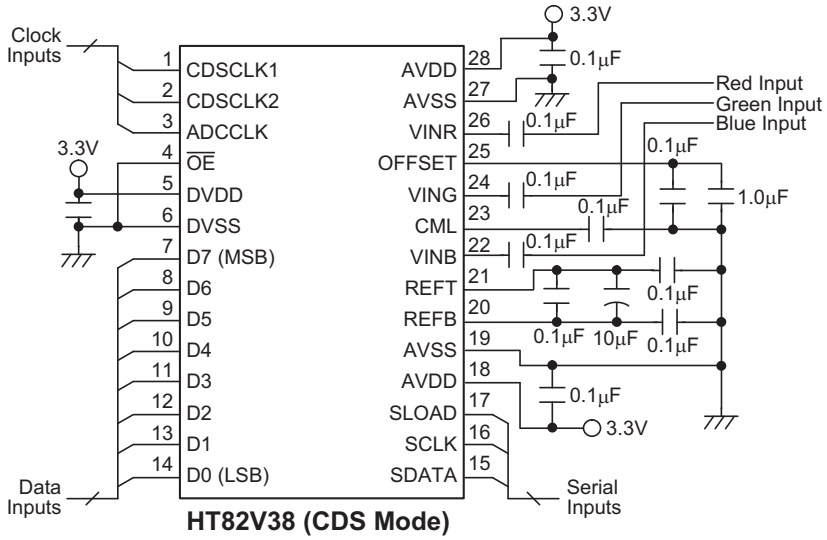


Single Byte Mode Digital Data Output Timing

Application Circuits

Circuit and Layout Recommendations

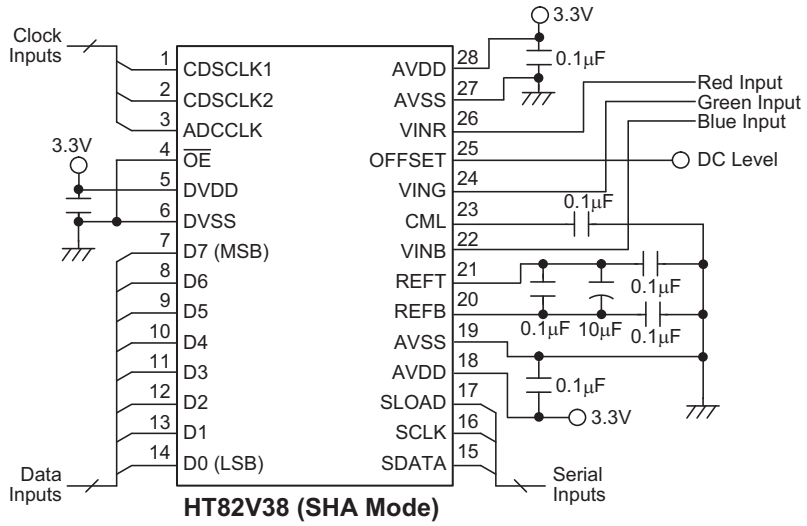
The recommended circuit configuration for 3-Channel CDS mode operation is shown in Figure. The recommended input coupling capacitor value is 0.1μF (see Circuit Operation section for more details). A single ground plane is recommended for the HT82V38. A separate power supply may be used for DRV_{DD}, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as the rest of the HT82V38. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC, or by using external digital buffers. To minimize the effect of digital transients during major output code transitions, the falling edge of CDSCLK2 should occur coincident with or before the transient edge of ADCCLK. All 0.1μF decoupling capacitors should be located as close as possible to the HT82V38 pins. When operating in single channel mode, the unused analog inputs should be grounded.



HT82V38 (CDS Mode)

CDS Application Circuit

Figure shows the recommended circuit configuration for 3-Channel SHA mode. All of the above considerations also apply for this configuration, except that the analog input signals are directly connected to the HT82V38 without the use of coupling capacitors. The analog input signals must already be dc-biased (relative to OFFSET pin) between 0V and 1.60V/2.0V.



HT82V38 (SHA Mode)

SHA Application Circuit

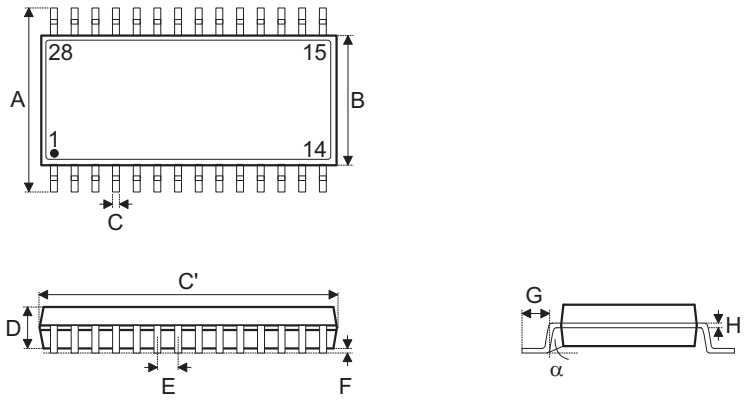
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

28-pin SSOP (209mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.291	0.307	0.323
B	0.197	0.209	0.220
C	0.009	—	0.015
C′	0.390	0.402	0.413
D	—	—	0.079
E	—	0.026 BSC	—
F	0.002	—	—
G	0.022	—	0.037
H	0.004	—	0.008
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	7.40	7.80	8.20
B	5.00	5.30	5.60
C	0.22	—	0.38
C′	9.90	10.20	10.50
D	—	—	2.00
E	—	0.65 BSC	—
F	0.05	—	—
G	0.55	0.75	0.95
H	0.09	—	0.21
α	0°	—	8°

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