DDR3 SDRAM VLP Registered DIMM Based on 1Gb A version

HMT112V7AFP8C
HMT125V7AFP8C
HMT125V7AFP4C
HMT351V7AMP4C

** Contents may be changed at any time without any notice.

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	2008-8	
0.2	Added IDD, corrected typos	2008-12	

Table of Contents

1. Description

This Hynix DDR3 VLP (Very Low Profile) registered Dual In-Line Memory Module (DIMM) series consists of 1Gb A generation. These are intended for use as main memory in server and workstation systems, providing a high performance 8 byte interface in 133.35mm width form factor of industry standard. It is suitable for easy interchange and addition.

1.1 Device Features & Ordering Information

1.1.1 Features

- VDD=VDDQ=1.5V
- VDDSPD=3.3V to 3.6V
- Fully differential clock inputs (CK, $\overline{CK}$) operation
- Differential Data Strobe (DQS, $\overline{DQS}$)
- On chip DLL align DQ, DQS and /DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, and (11) supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- DDR3 SDRAM Package: JEDEC standard 78ball FBGA(x4/x8), 96ball FBGA(x16) with support balls
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Auto Self Refresh supported
- 8 bit pre-fetch
- Heat Spreader installed for 4GB
- SPD with Integrated TS of Class B

1.1.2 Ordering Information

Part Name	Density	Organization	# of DRAMs	# of ranks	Materials	FDHS
HMT112V7AFP8C-G7/H9	1GB	128Mx72	9	1	Lead free	X
HMT125V7AFP8C-G7/H9	2GB	256Mx72	18	2	Lead free	X
HMT125V7AFP4C-G7/H9	2GB	256Mx72	18	1	Lead free	X
HMT351V7AMP4C-G7/H9	4GB	512Mx72	36	2	Lead free	O

*Please Contact local sales administrator for more details of part number

1.2 Speed Grade & Key Parameters

MT/S	DDR3-1066	DDR3-1333	Unit
Grade	-G7	-H9	
tCK (min)	1.875	1.5	ns
CAS Latency	7	9	tCK
tRCD (min)	13.125	13.5	ns
tRP (min)	13.125	13.5	ns
tRAS (min)	37.5	36	ns
tRC (min)	50.625	49.5	ns
CL-tRCD-tRP	7-7-7	9-9-9	tCK

1.3 Address Table

	1GB(1Rx8)	2GB(2Rx8)	2GB(1Rx4)	4GB(2Rx4)
Organization	128M x 72	256M x 72	256M x 72	512M x 72
Refresh Method	8K/64ms	8K/64ms	8K/64ms	8K/64ms
Row Address	A0-A13	A0-A13	A0-A13	A0-A13
Column Address	A0-A9	A0-A9	A0-A9,A11	A0-A9,A11
Bank Address	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2
Page Size	1KB	1KB	1KB	1KB
# of Rank	1	2	1	2
# of Device	9	18	18	36

2. Pin Architecture

2.1 Pin Definition

Pin Name	Description	Num-ber	Pin Name	Description	Num-ber
A0–A9,A11 A13-A15	Address Inputs	14	A10/AP	Address Input/Autoprecharge	1
BA0–BA2	SDRAM Bank Addresses	3	A12/$\overline{BC}$	Address Input/Autoprecharge	1
$\overline{RAS}$	Row Address Strobe	1	SCL	Serial Presence Detect (SPD) Clock Input	1
$\overline{CAS}$	Column Address Strobe	1	SDA	SPD Data Input/Output	1
$\overline{WE}$	Write Enable	1	SA0–SA2	SPD Address Inputs	3
$\overline{S}$0–$\overline{S}$3	Chip Selects	4	Par_in	Parity Bit For The Address and Control Bus	1
CKE0–CKE1	Clock Enables	2	$\overline{ERR\_OUT}$	Parity Error Found on the Address and Control Bus	1
ODT0–ODT1	On-die termination Inputs	2	$\overline{EVENT}$	Reserved for Optional Hardware temperature Sensing	1
DQ0–DQ63	Data Input/Output	64	TEST	Memory Bus Test Tool (Not Connected and Not Usable on DIMMs)	1
CB0–CB7	Data Check Bits Input/Output	8	$\overline{RESET}$	Register and SDRAM control pin	1
DQS0–DQS8	Data Strobes	9	V_{DD}	Power Supply	22
$\overline{DQS0}$–$\overline{DQS8}$	Data Strobes, Negative Line	9	V_{SS}	Ground	59
DM0–DM8 DQS9-DQS17 TDQS9-TDQS17	Data Masks Data Strobes Termination Data Strobes	9	V_{REF}DQ	Reference Voltage for DQ	1
			V_{REF}CA	Reference Voltage for CA	1
			V_{TT}	Termination Voltage	4
$\overline{DQS9}$–$\overline{DQS17}$ TDQS9–TDQS17	Data Strobes, Negative Line Termination Data Strobes	9	V_{DDSPD}	SPD Power	1
			CK1	Clock Input, positive line	1
CK0	Clock Input, positive line	1	$\overline{CK1}$	Clock Input, negative line	1
$\overline{CK0}$	Clock Input, positive Line	1			

2.2 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	IN	Positive Line	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver.
$\overline{CK0}$	IN	Negative Line	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver.
CK1	IN	Positive Line	Terminated but not used on RDIMMs
$\overline{CK1}$	IN	Negative Line	Terminated but not used on RDIMMs
CKE0–CKE1	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank)
$\overline{S0}$–$\overline{S3}$	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders.When decoders are disabled, new commands are ignored and previous operations continue.Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s).For modules with two registers,S[3:2] operate similarly to S[1:0] for the second set of register outputs or register control words.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
ODT0–ODT1	IN	Active High	On-Die Termination control signals
V_{REF}DQ	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7
V_{REF}CA	Supply		Reference voltage for A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$, $\overline{S1}$, CKE0, CKE1, Par_In, ODT0 and ODT1.
V_{DD}Q	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, V_{DD}Q shares the same power plane as V_{DD} pins.
BA0–BA2	IN	—	Selects which SDRAM bank of eight is activated. BA0-BA2 define to which bank an Active, Read, Write or Precharge command is being applied.Bank address also determines mode register is to be accessed during an MRS cycle.
A0-A9 A10/AP A11 A12/BC A13-A15	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank.A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH).If only one bank is to be precharged, the bank is selected by BA.A12 is also utilized for BL 4/8 identification for “BL on the fly” during CAS command. The address inputs also provide the op-code during Mode Register Set commands.
DQ0–DQ63, CB0–CB7	I/O	—	Data and Check Bit Input/Output pins.

Symbol	Type	Polarity	Function
DM0–DM8	IN	Active High	Masks write data when high, issued concurrently with input data.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR3 SDRAM input buffers, and core logic.
V_{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS0-DQS17	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
$\overline{DQS0}$–$\overline{DQS17}$	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
TDQS9-TDQS17 $\overline{TDQS9-TDQS17}$	OUT		TDQS/TDQS is applicable for x8 DRAMs only. WHen enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/TDQS that is applied to DQS/DQS. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and TDQS is not used.x4/x16 DRAMs must disable the TDQS function via mode register A11=0 in MR1.
SA0–SA2		—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pullup on the system board.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to V_{DDSPD} to act as a pull up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
$\overline{EVENT}$	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the $\overline{EVENT}$ pin on TS/SPD part.
$\overline{RESET}$	IN		The $\overline{RESET}$ pin is connected to the $\overline{RESET}$ pin on the register and to the $\overline{RESET}$ pin on the DRAM. When low, all register outputs will be driven low and the Clock Driver clocks to the DRAMs and register(s) will be set to low level (the Clock Driver will remain synchronized with the input clock)
Par_In	IN		Parity bit for the Address and Control bus.(“1”:Odd, “0”:Even)
$\overline{Err\_Out}$	OUT (open drain)		Parity error detected on the Address and Control bus.A resistor may be connected from $\overline{Err\_Out}$ bus line to VDD on the system planar to act as a pull up.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

2.3 Pin Assignment

Pin #	Front Side (left 1–60)	Pin #	Back Side (right 121–180)	Pin #	Front Side (left 61–120)	Pin #	Back Side (right 181–240)
1	VREFDQ	121	VSS	61	A2	181	A1
2	VSS	122	DQ4	62	VDD	182	VDD
3	DQ0	123	DQ5	63	NC, CK1	183	VDD
4	DQ1	124	VSS	64	NC, $\overline{CK1}$	184	CK0
5	VSS	125	DM0,DQS9,TDQS9	65	VDD	185	$\overline{CK0}$
6	$\overline{DQS0}$	126	NC, $\overline{DQS9}$,$\overline{TDQS9}$	66	VDD	186	VDD
7	DQS0	127	VSS	67	VREFCA	187	$\overline{EVENT}$, NC
8	VSS	128	DQ6	68	Par_in, NC	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10 / AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDD
12	DQ8	132	DQ13	72	VDD	192	$\overline{RAS}$
13	DQ9	133	VSS	73	$\overline{WE}$	193	$\overline{S0}$
14	VSS	134	DM1,DQS10,TDQS10	74	$\overline{CAS}$	194	VDD
15	$\overline{DQS1}$	135	NC,$\overline{DQS10}$,$\overline{TDQS10}$	75	VDD	195	ODT0
16	DQS1	136	VSS	76	$\overline{S1}$, NC	196	A13
17	VSS	137	DQ14	77	ODT1, NC	197	VDD
18	DQ10	138	DQ15	78	VDD	198	$\overline{S3}$, NC
19	DQ11	139	VSS	79	$\overline{S2}$, NC	199	VSS
20	VSS	140	DQ20	80	VSS	200	DQ36
21	DQ16	141	DQ21	81	DQ32	201	DQ37
22	DQ17	142	VSS	82	DQ33	202	VSS
23	VSS	143	DM2,DQS11,TDQS11	83	VSS	203	DM4,DQS13,TDQS13
24	$\overline{DQS2}$	144	NC,$\overline{DQS11}$,$\overline{TDQS11}$	84	$\overline{DQS4}$	204	NC, $\overline{DQS13}$,$\overline{TDQS13}$
25	DQS2	145	VSS	85	DQS4	205	VSS
26	VSS	146	DQ22	86	VSS	206	DQ38
27	DQ18	147	DQ23	87	DQ34	207	DQ39
28	DQ19	148	VSS	88	DQ35	208	VSS
29	VSS	149	DQ28	89	VSS	209	DQ44
30	DQ24	150	DQ29	90	DQ40	210	DQ45
31	DQ25	151	VSS	91	DQ41	211	VSS
32	VSS	152	DM3,DQS12,TDQS12	92	VSS	212	DM5,DQS14,TDQS14
33	$\overline{DQS3}$	153	NC, $\overline{DQS12}$,$\overline{TDQS12}$	93	$\overline{DQS5}$	213	NC, $\overline{DQS14}$,$\overline{TDQS14}$

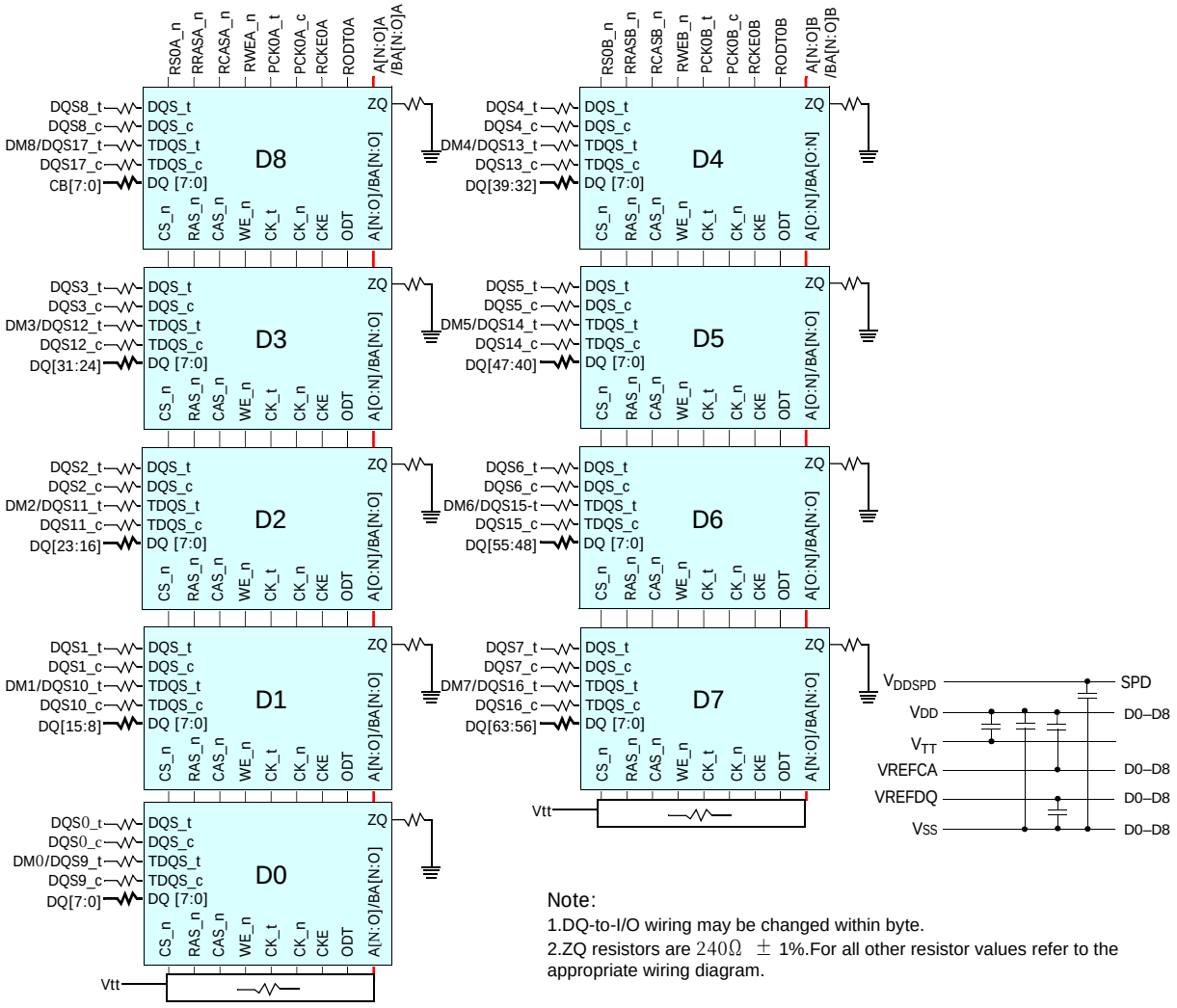
NC = No Connect; RFU = Reserved Future Use

Pin #	Front Side (left 1–60)	Pin #	Back Side (right 121–180)	Pin #	Front Side (left 61–120)	Pin #	Back Side (right 181–240)
34	DQS3	154	VSS	94	DQS5	214	VSS
35	VSS	155	DQ30	95	VSS	215	DQ46
36	DQ26	156	DQ31	96	DQ42	216	DQ47
37	DQ27	157	VSS	97	DQ43	217	VSS
38	VSS	158	CB4, NC	98	VSS	218	DQ52
39	CB0, NC	159	CB5, NC	99	DQ48	219	DQ53
40	CB1, NC	160	VSS	100	DQ49	220	VSS
41	VSS	161	DM8,DQS17,TDQS17 NC	101	VSS	221	DM6,DQS15,TDQS15
42	$\overline{DQS8}$	162	NC,$\overline{DQS17}$,$\overline{TDQS17}$	102	$\overline{DQS6}$	222	NC, $\overline{DQS15}$,$\overline{TDQS15}$
43	DQS8	163	VSS	103	DQS6	223	VSS
44	VSS	164	CB6, NC	104	VSS	224	DQ54
45	CB2, NC	165	CB7, NC	105	DQ50	225	DQ55
46	CB3, NC	166	VSS	106	DQ51	226	VSS
47	VSS	167	NC(TEST)	107	VSS	227	DQ60
48	VTT, NC	168	$\overline{RESET}$	108	DQ56	228	DQ61
KEY		KEY		109	DQ57	229	VSS
49	VTT, NC	169	CKE1, NC	110	VSS	230	DM7,DQS16,TDQS16
50	CKE0	170	VDD	111	$\overline{DQS7}$	231	NC, $\overline{DQS16}$,$\overline{TDQS16}$
51	VDD	171	A15	112	DQS7	232	VSS
52	BA2	172	A14	113	VSS	233	DQ62
53	$\overline{Err\_Out}$, NC	173	VDD	114	DQ58	234	DQ63
54	VDD	174	A12 / $\overline{BC}$	115	DQ59	235	VSS
55	A11	175	A9	116	VSS	236	VDDSPD
56	A7	176	VDD	117	SA0	237	SA1
57	VDD	177	A8	118	SCL	238	SDA
58	A5	178	A6	119	SA2	239	VSS
59	A4	179	VDD	120	VTT	240	VTT
60	VDD	180	A3				

NC = No Connect; RFU = Reserved Future Use

3. Functional Block Diagram

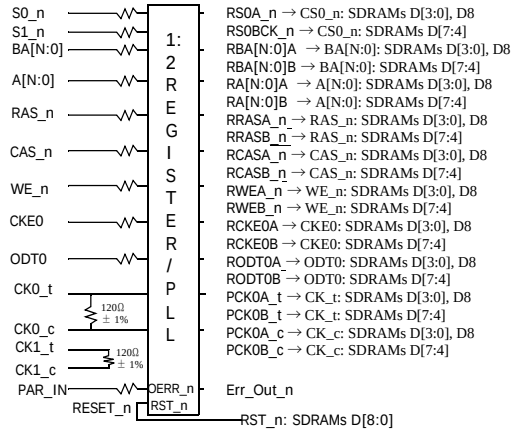
3.1 1GB, 128Mx72 Module(1Rank of x8)



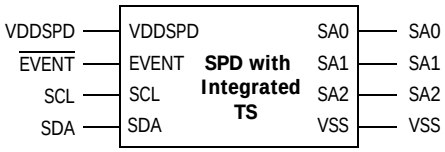
Note:

1.DQ-to-I/O wiring may be changed within byte.

2.ZQ resistors are 240Ω ± 1%.For all other resistor values refer to the appropriate wiring diagram.

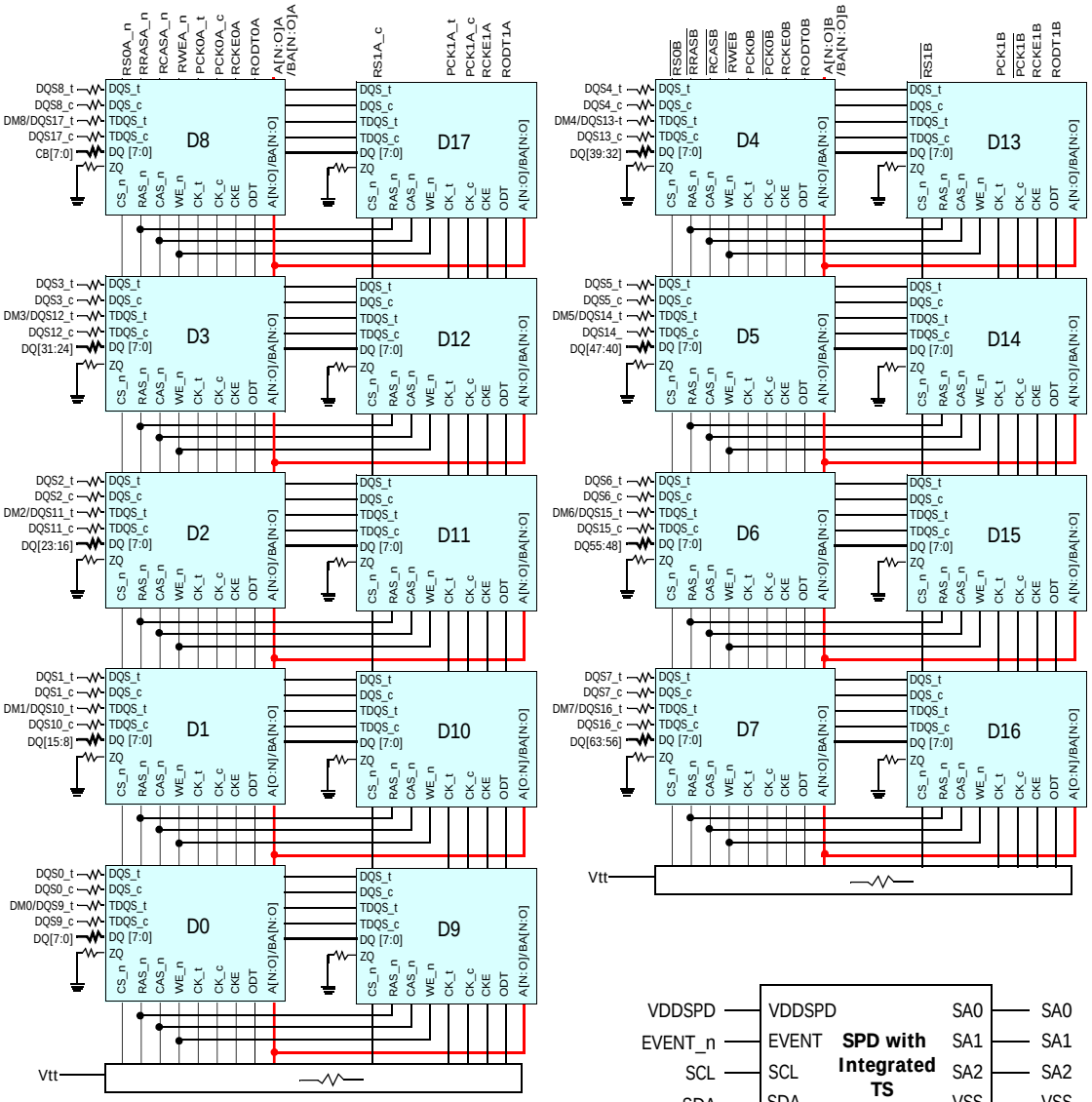


S[3:2], CKE1, ODT1, are NC (Unused register inputs ODT1 and CKE1 have a 120...330Ω resistor to ground



Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative

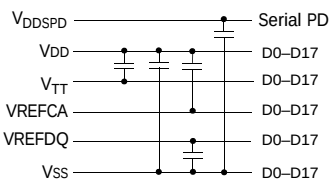
3.2 2GB, 256Mx72 Module(2Rank of x8)

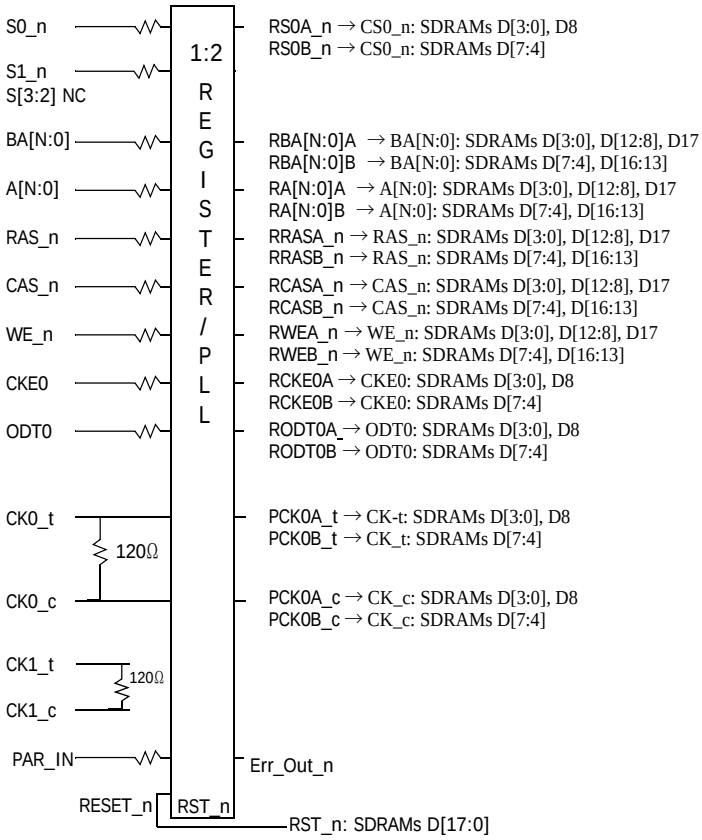


Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative

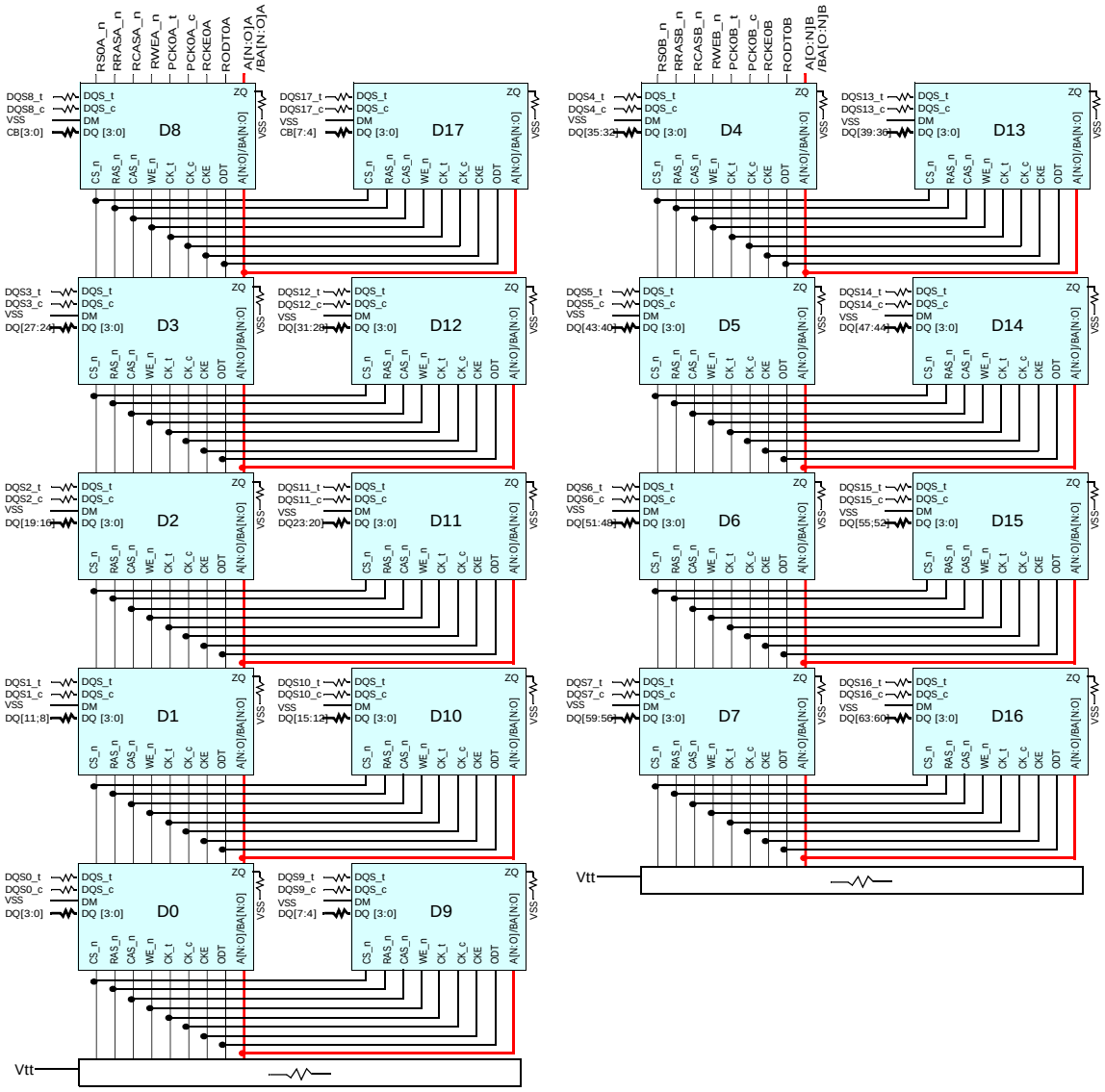
Note:

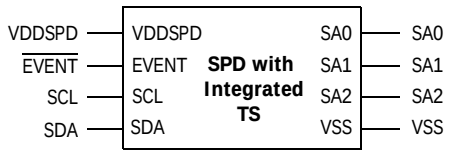
1. DQ-to-I/O wiring may be changed within a byte.
2. Unless otherwise noted, resistor values are 15Ω ± 5%.
3. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
4. See the wiring diagrams for all resistors associated with the command, address and control bus.




S0_n
S1_n
S[3:2] NC
BA[N:0]
A[N:0]
RAS_n
CAS_n
WE_n
CKE0
ODT0
CK0_t
120Ω
CK0_c
CK1_t
120Ω
CK1_c
PAR_IN
RESET_n
1:2
REGISTER/PLL
RST_n
RS0A_n → CS0_n: SDRAMs D[3:0], D8
RS0B_n → CS0_n: SDRAMs D[7:4]
RBA[N:0]A → BA[N:0]: SDRAMs D[3:0], D[12:8], D17
RBA[N:0]B → BA[N:0]: SDRAMs D[7:4], D[16:13]
RA[N:0]A → A[N:0]: SDRAMs D[3:0], D[12:8], D17
RA[N:0]B → A[N:0]: SDRAMs D[7:4], D[16:13]
RRASA_n → RAS_n: SDRAMs D[3:0], D[12:8], D17
RRASB_n → RAS_n: SDRAMs D[7:4], D[16:13]
RCASA_n → CAS_n: SDRAMs D[3:0], D[12:8], D17
RCASB_n → CAS_n: SDRAMs D[7:4], D[16:13]
RWEA_n → WE_n: SDRAMs D[3:0], D[12:8], D17
RWEB_n → WE_n: SDRAMs D[7:4], D[16:13]
RCKE0A → CKE0: SDRAMs D[3:0], D8
RCKE0B → CKE0: SDRAMs D[7:4]
RODT0A → ODT0: SDRAMs D[3:0], D8
RODT0B → ODT0: SDRAMs D[7:4]
PCK0A_t → CK-t: SDRAMs D[3:0], D8
PCK0B_t → CK_t: SDRAMs D[7:4]
PCK0A_c → CK_c: SDRAMs D[3:0], D8
PCK0B_c → CK_c: SDRAMs D[7:4]
Err_Out_n
RST_n: SDRAMs D[17:0]

3.3 2GB, 256Mx72 Module(1Rank of x4)

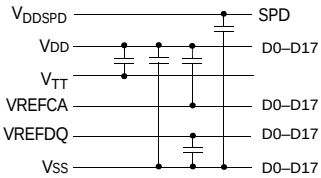


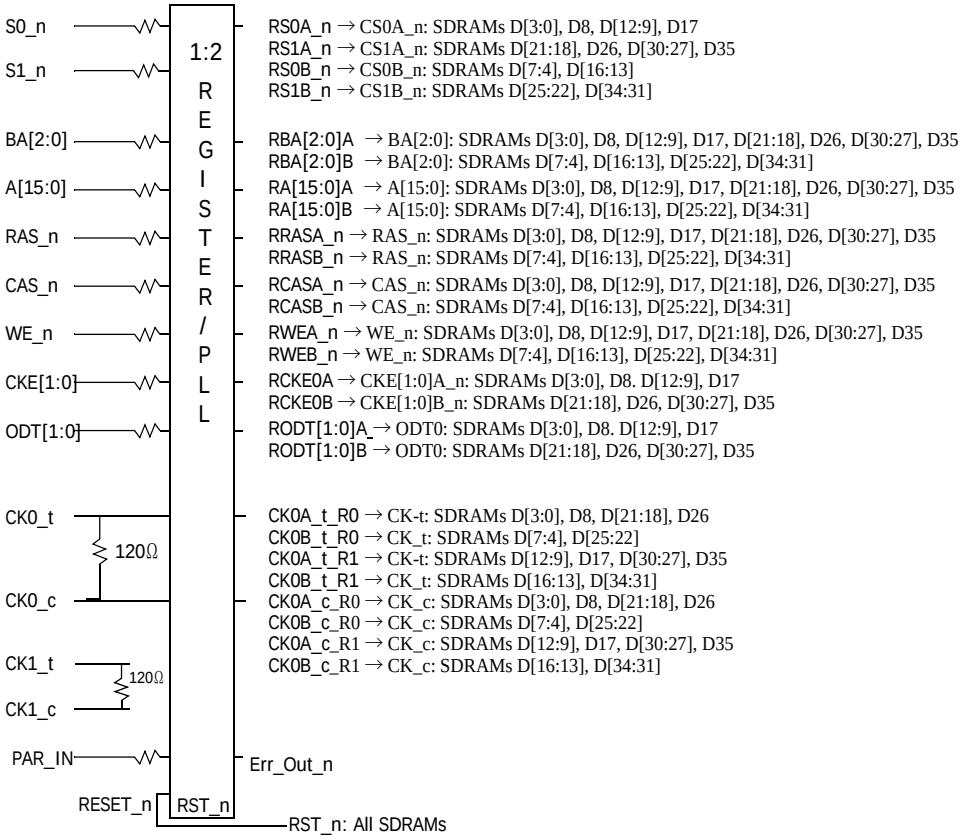


Plan to use SPD with Integrated TS of Class B and might be changed on customer's requests. For more details of SPD and Thermal sensor, please contact local Hynix sales representative

Note:

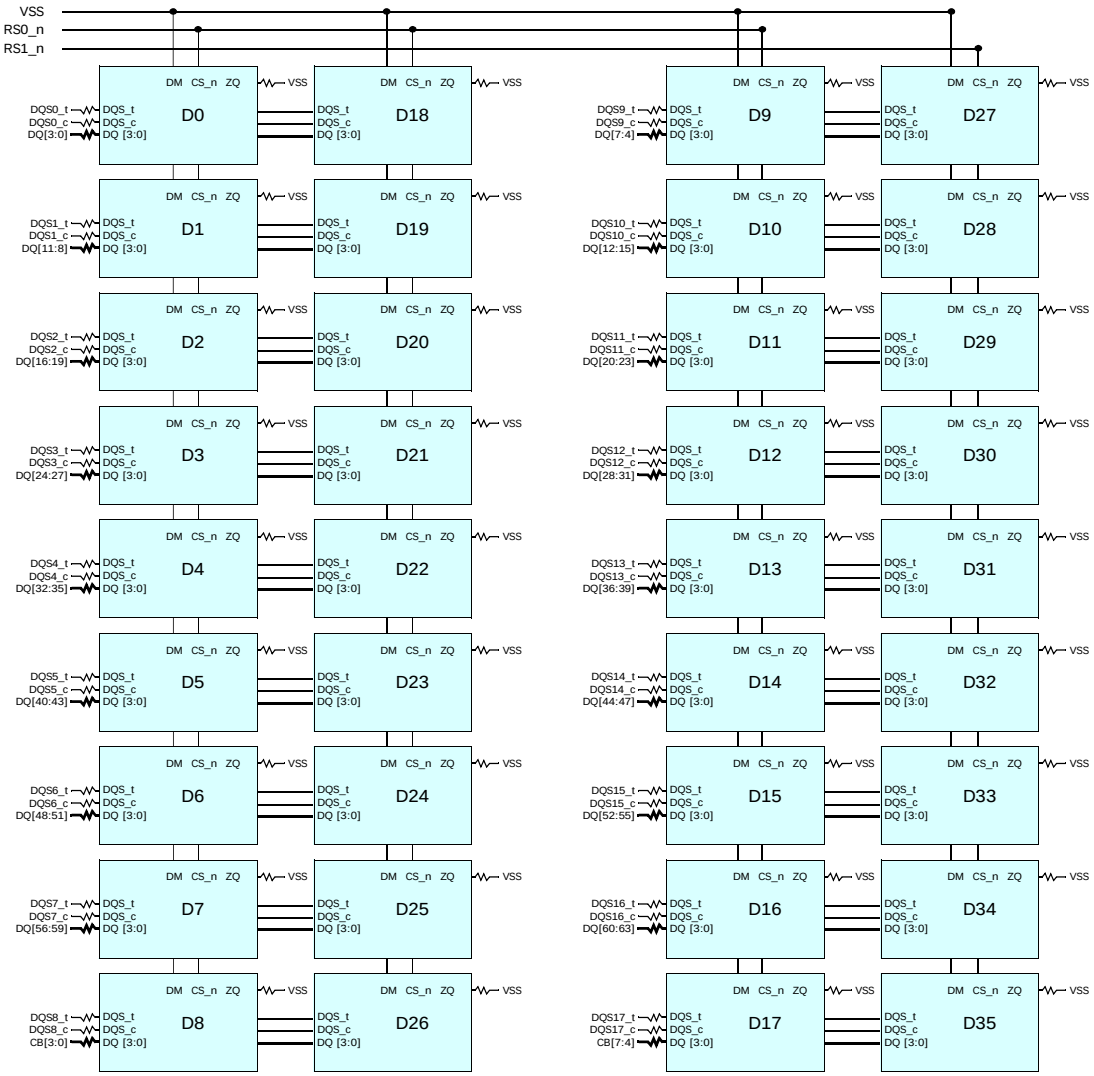
1. DQ-to-I/O wiring may be changed within a nibble.
2. Unless otherwise noted, resistor values are 15Ω ±5%.
3. See the wiring diagrams for all resistors associated with the command, address and control bus.
4. ZQ resistors are 240Ω ±1 %. For all other resistor values refer to the appropriate wiring diagram.

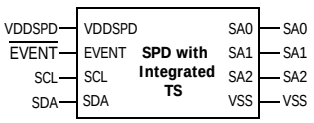




* S[3:2]_n are NC (Note: Otherwise stated differently all resistors values on this base are 22Ω+-5%)

3.4 4GB, 512Mx72 Module(2Rank of x4)





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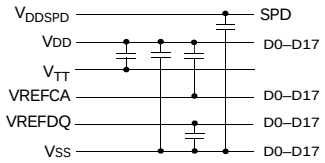
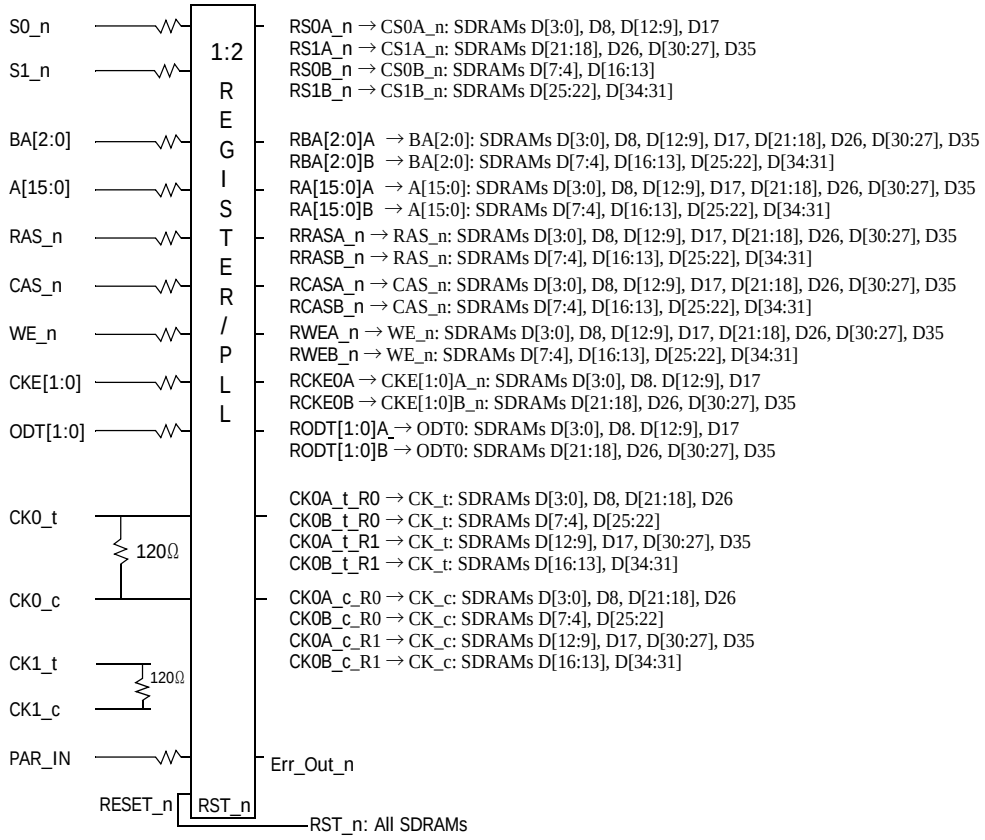


Note:
1. DQ-to-I/O wiring may be changed within a nibble.
2. ZQ pins of each SDRAM are connected to individual RZQ resistors (240+/-1%) ohms.



* S[3:2]_n are NC (Note: Otherwise stated differently all resistors values on this base are 22Ω+-5%)

4. Pin Capacitance (VDD=1.5V, VDDQ=1.5V)

1GB: HMT112V7AFP8C

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	CCK	TBD	TBD	pF
CKE, ODT	CI1	TBD	TBD	pF
$\overline{CS}$	CI2	TBD	TBD	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI3	TBD	TBD	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	TBD	TBD	pF

2GB: HMT125V7AFP8C

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	CCK	TBD	TBD	pF
CKE, ODT	CI1	TBD	TBD	pF
$\overline{CS}$	CI2	TBD	TBD	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI3	TBD	TBD	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	TBD	TBD	pF

2GB: HMT125V7AFP4C

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	CCK	TBD	TBD	pF
CKE, ODT	CI1	TBD	TBD	pF
$\overline{CS}$	CI2	TBD	TBD	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI3	TBD	TBD	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	TBD	TBD	pF

4GB: HMT351V7AMP4C

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	CCK	TBD	TBD	pF
CKE, ODT	CI1	TBD	TBD	pF
$\overline{CS}$	CI2	TBD	TBD	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI3	TBD	TBD	pF
DQ, DM, DQS, $\overline{DQS}$	CIO	TBD	TBD	pF

Note:

1. Pins not under test are tied to GND.
2. These value are guaranteed by design and tested on a sample basis only.

5. IDD Specifications (Tcase: 0 to 95°C)

1GB, 128M x 72 R-DIMM: HMT112V7AFP8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	1484	1592	1664	mA	
IDD1	1664	1799	1889	mA	
IDD2N	1259	1349	1439	mA	
IDD2NT	1304	1394	1484	mA	
IDDQ2NT	1502	1502	1502	mA	
IDD2P0	318	318	318	mA	
IDD2P1	462	480	498	mA	
IDD2Q	1259	1349	1439	mA	
IDD3N	1349	1439	1529	mA	
IDD3P	498	588	633	mA	
IDD4R	2024	2294	2654	mA	
IDDQ4R	1304	1304	1304	mA	
IDD4W	2204	2564	2834	mA	
IDD5B	2474	2564	2654	mA	
IDD6	318	318	318	mA	
IDD6ET	336	336	336	mA	
IDD6TC	336	336	336	mA	
IDD7	2654	3014	3464	mA	

2GB, 256M x 72 R-DIMM: HMT125V7AFP8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	1979	2177	2399	mA	
IDD1	2159	2384	2564	mA	
IDD2N	1754	1934	2114	mA	
IDD2NT	1844	2024	2204	mA	
IDDQ2NT	2240	2240	2240	mA	
IDD2P0	408	408	408	mA	
IDD2P1	696	732	768	mA	
IDD2Q	1754	1934	2114	mA	
IDD3N	1934	2114	2294	mA	
IDD3P	798	948	1038	mA	
IDD4R	2519	2879	3329	mA	
IDDQ4R	1799	1889	1979	mA	
IDD4W	2699	3149	3509	mA	
IDD5B	2969	3149	3329	mA	
IDD6	408	408	408	mA	
IDD6ET	444	444	444	mA	
IDD6TC	444	444	444	mA	
IDD7	3149	3599	4139	mA	

2GB, 256M x 72 R-DIMM: HMT125V7AFP4C

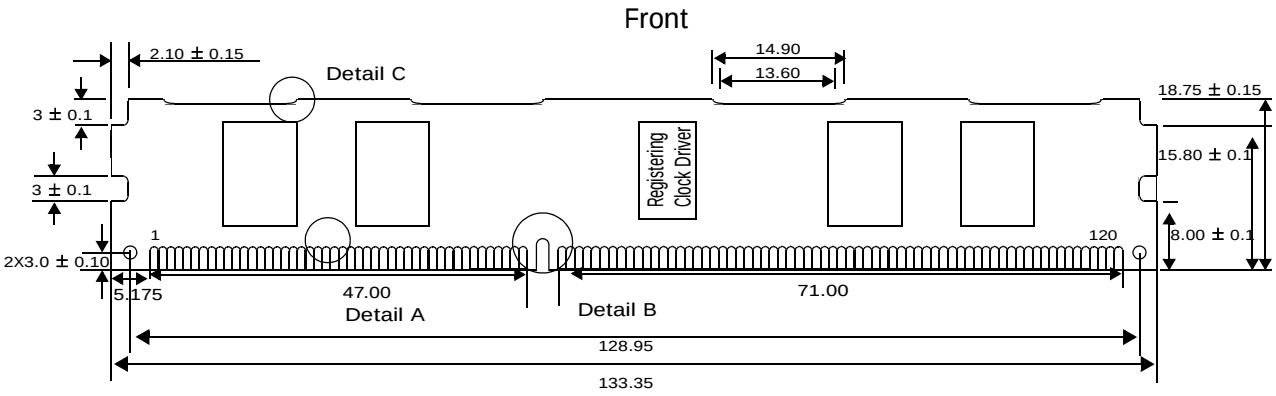
Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	2204	2420	2564	mA	
IDD1	2564	2834	3014	mA	
IDD2N	1754	1934	2114	mA	
IDD2NT	1844	2024	2204	mA	
IDDQ2NT	2240	2240	2240	mA	
IDD2P0	408	408	408	mA	
IDD2P1	696	732	768	mA	
IDD2Q	1754	1934	2114	mA	
IDD3N	1934	2114	2294	mA	
IDD3P	768	948	1038	mA	
IDD4R	3284	3824	4544	mA	
IDDQ4R	1844	1844	1844	mA	
IDD4W	3644	4364	4904	mA	
IDD5B	4184	4364	4544	mA	
IDD6	408	408	408	mA	
IDDET	444	444	444	mA	
IDD6TC	444	444	444	mA	
IDD7	4544	5264	6164	mA	

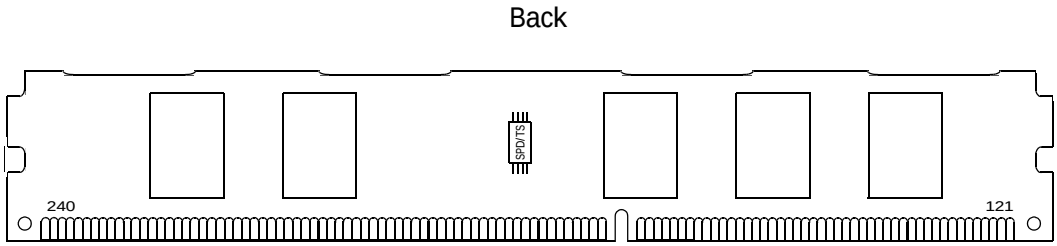
4GB, 512M x 72 R-DIMM: HMT351V7AMP4C

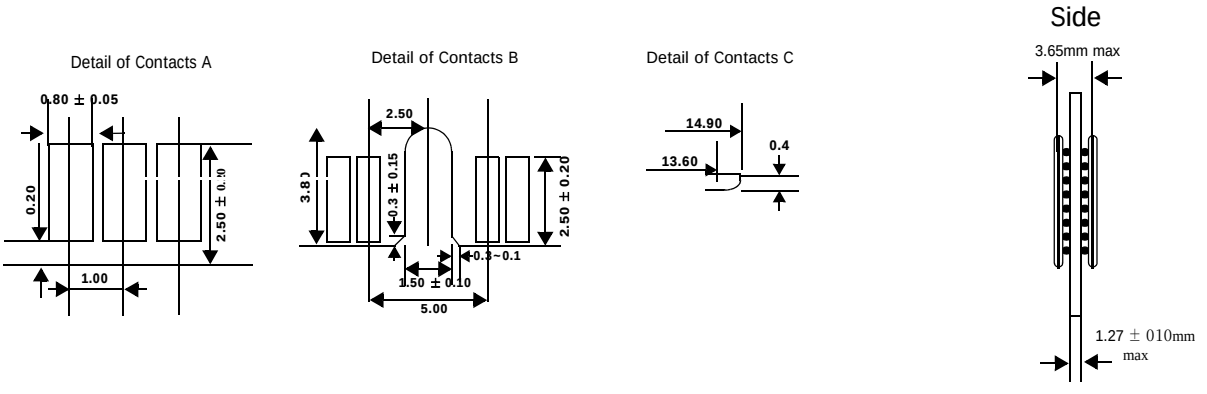
Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	3194	3590	3914	mA	
IDD1	3554	4004	4364	mA	
IDD2N	2744	3104	3464	mA	
IDD2NT	2924	3284	3644	mA	
IDDQ2NT	3716	3716	3716	mA	
IDD2P0	588	588	588	mA	
IDD2P1	1164	1236	1308	mA	
IDD2Q	2744	3104	3464	mA	
IDD3N	3104	3464	3824	mA	
IDD3P	1308	1668	1848	mA	
IDD4R	4274	4994	5894	mA	
IDDQ4R	2834	3014	3194	mA	
IDD4W	4634	5534	6254	mA	
IDD5B	5174	5534	5894	mA	
IDD6	588	588	588	mA	
IDDET	660	660	660	mA	
IDD6TC	660	660	660	mA	
IDD7	5534	6434	7514	mA	

6. Dimm Outline Diagram

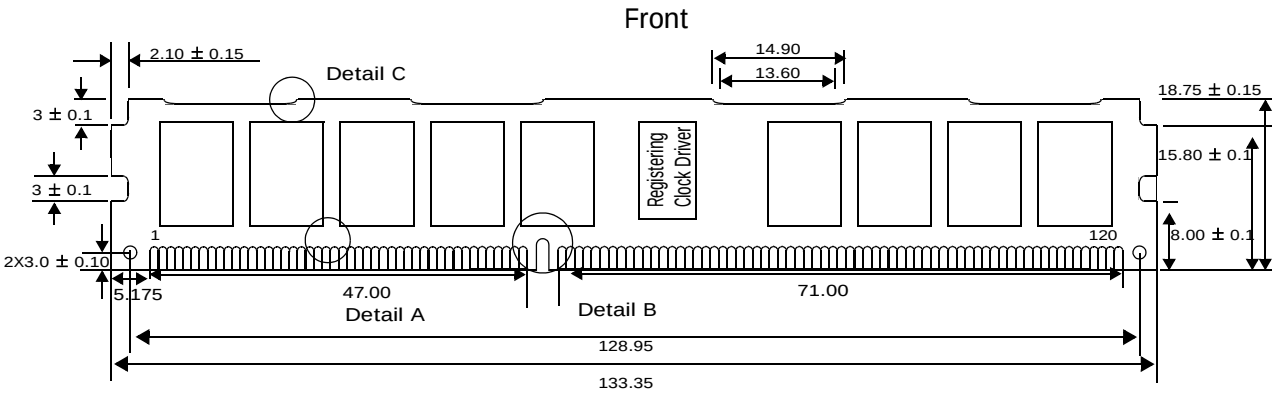
6.1 128Mx72 - HMT112V7AFP8C

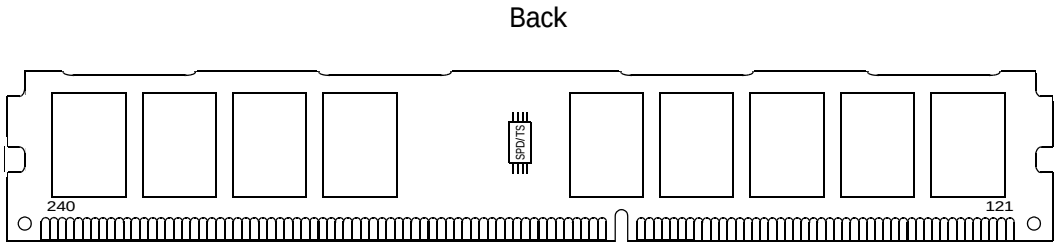


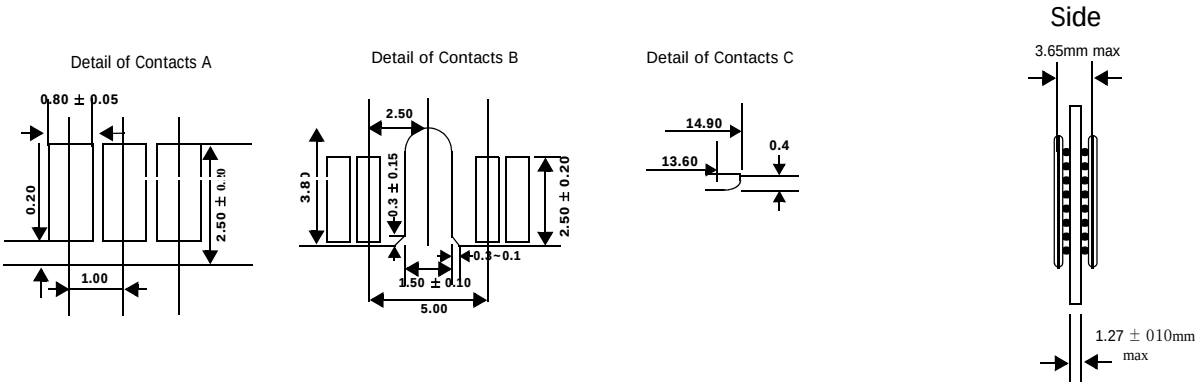




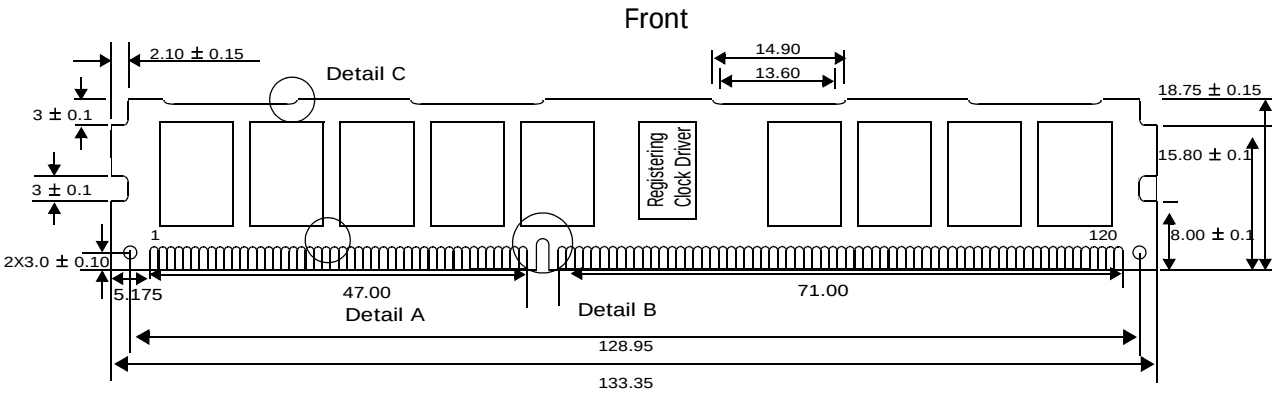
6.2 256Mx72 - HMT125V7AFP8C

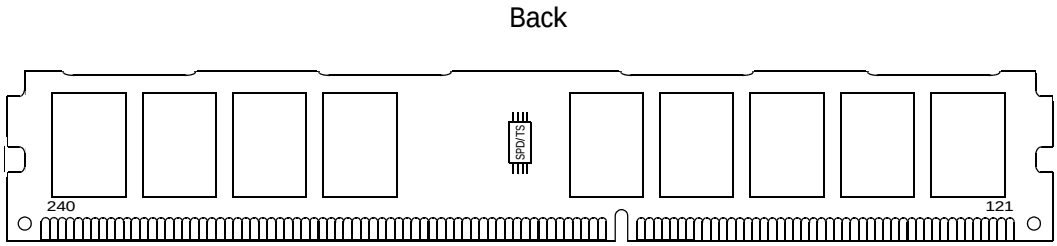


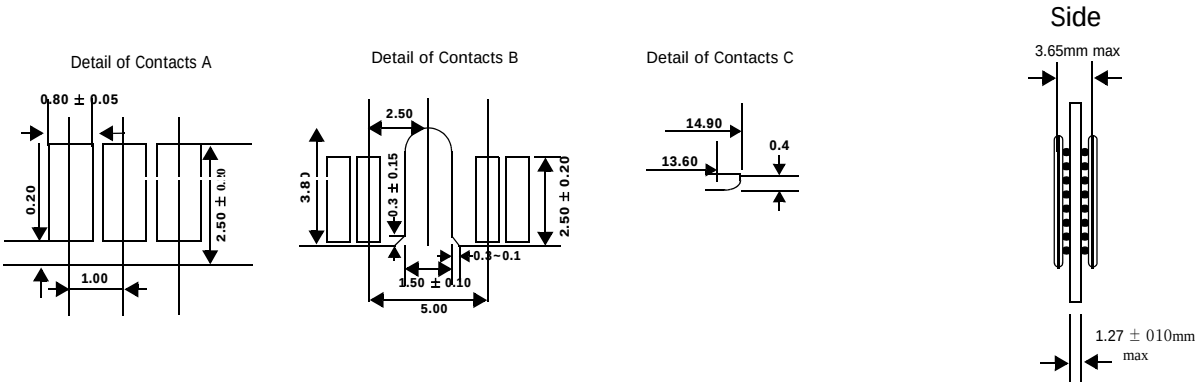




6.3 256Mx72 - HMT125V7AFP4C

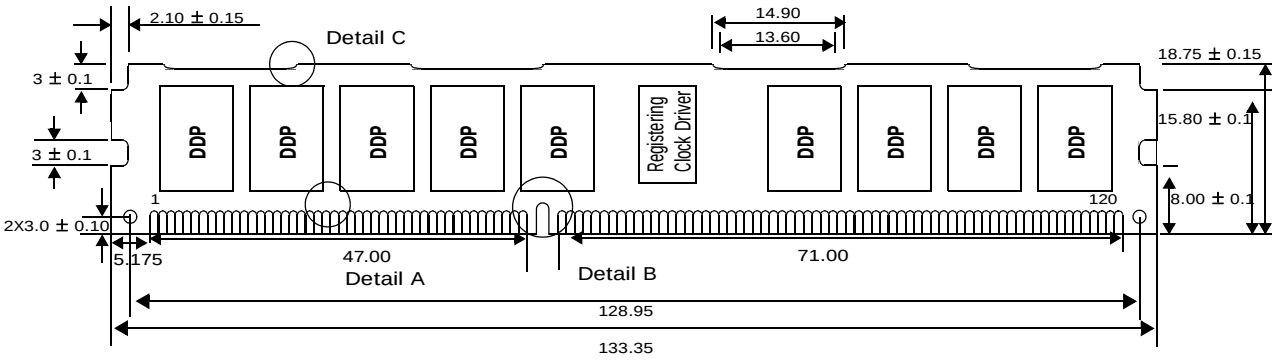




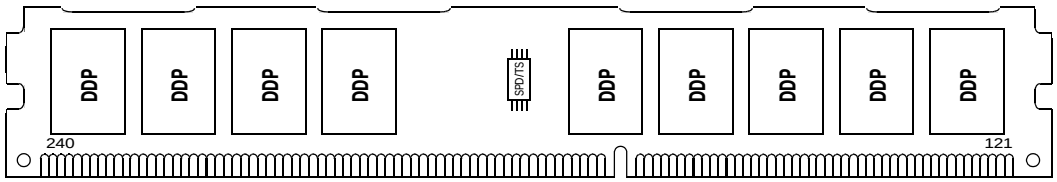


6.4 512Mx72 - HMT351V7AMP4C

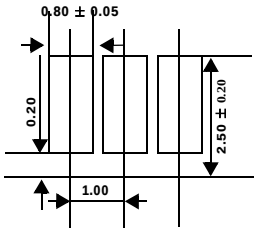
Front



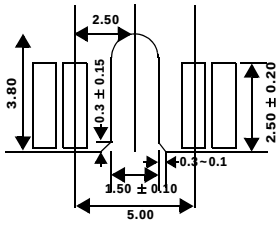
Back



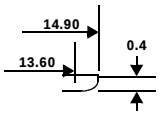
Detail of Contacts A



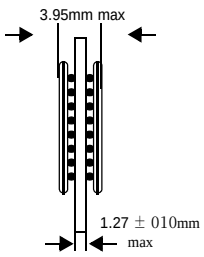
Detail of Contacts B



Detail of Contacts C

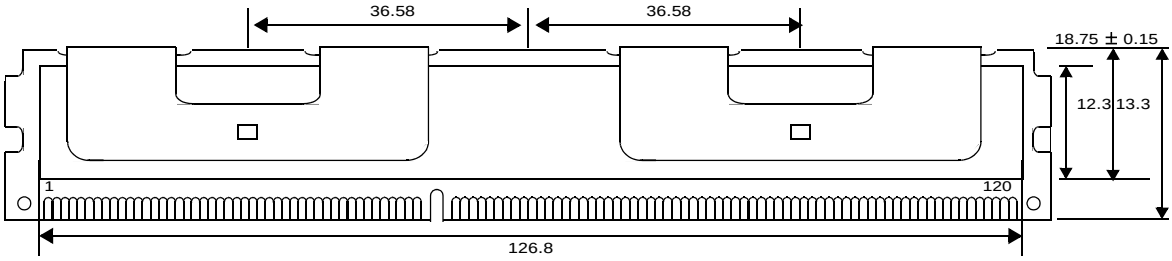


Side

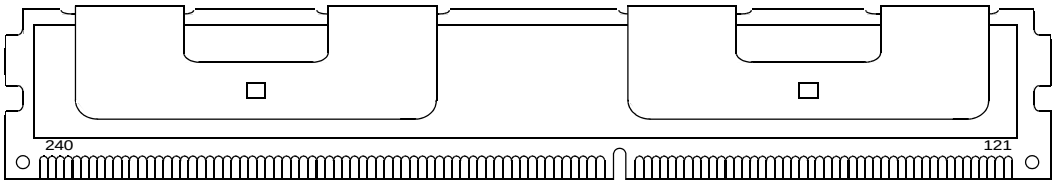


6.4 512Mx72 - HMT351V7AMP4C

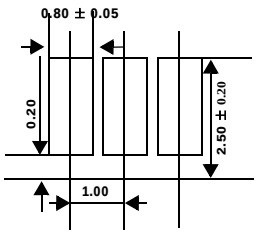
Front



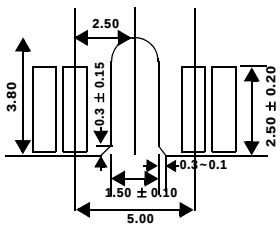
Back



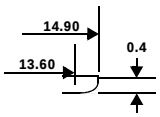
Detail of Contacts A



Detail of Contacts B



Detail of Contacts C



Side