# XC7SH125

## Bus buffer/line driver; 3-state

Rev. 01 — 4 September 2009 Product data sheet

## 1. General description

XC7SH125 is a high-speed Si-gate CMOS device. It provides one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input ($\overline{OE}$). A HIGH at $\overline{OE}$ causes the output to assume a high-impedance OFF-state.

## 2. Features

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- SOT353-1, SOT753, SOT886, and SOT891 package options
- ESD protection:
  - HBM JESD22-A114E: exceeds 2000 V
  - MM JESD22-A115-A: exceeds 200 V
  - CDM JESD22-C101C: exceeds 1000 V
- Specified from –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| XC7SH125GW | –40 °C to +125 °C | TSSOP5 | plastic thin shrink small outline package; 5 leads; body width 1.25 mm | SOT353-1 |
| XC7SH125GV | –40 °C to +125 °C | SC-74A | plastic surface-mounted package; 5 leads | SOT753 |
| XC7SH125GM | –40 °C to +125 °C | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm | SOT886 |
| XC7SH125GF | –40 °C to +125 °C | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm | SOT891 |

NXP founded by Philips

# 4. Marking

**Table 2. Marking codes**

| Type number | Marking[1] |
|---|---|
| XC7SH125GW | fM |
| XC7SH125GV | f25 |
| XC7SH125GM | fM |
| XC7SH125GF | fM |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

# 5. Functional diagram

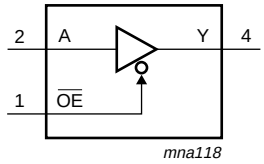



**Fig 1. Logic symbol**

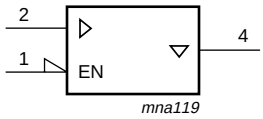



**Fig 2. IEC logic symbol**

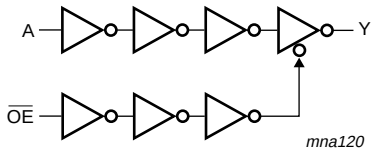



**Fig 3. Logic diagram**

# 6. Pinning information

## 6.1 Pinning

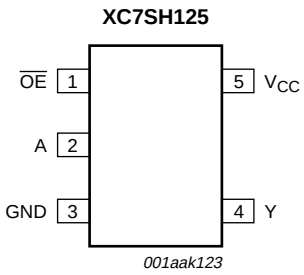
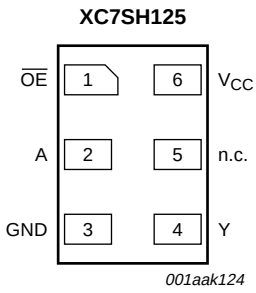
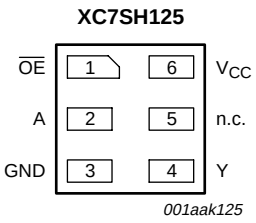



**Fig 4. Pin configuration SOT353-1 and SOT753**




Transparent top view

**Fig 5. Pin configuration SOT886**




Transparent top view

**Fig 6. Pin configuration SOT891**



© NXP B.V. 2009. All rights reserved.

### 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | | Description |
|---|---|---|---|
| | SOT353-1/SOT753 | SOT886/SOT891 | |
| $\overline{OE}$ | 1 | 1 | output enable input |
| A | 2 | 2 | data input |
| GND | 3 | 3 | ground (0 V) |
| Y | 4 | 4 | data output |
| n.c. | - | 5 | not connected |
| $V_{CC}$ | 5 | 6 | supply voltage |

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state*

| Inputs | | Output |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | L | L |
| L | H | H |
| H | X | Z |

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $V_I$ | input voltage | | | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V | [1] | –20 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_O$ | output current | $–0.5 \text{ V} < V_O < V_{CC} + 0.5$ V | | - | ±25 | mA |
| $I_{CC}$ | supply current | | | - | 75 | mA |
| $I_{GND}$ | ground current | | | –75 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = –40$ °C to +125 °C | [2] | - | 250 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP5 and SC-74A packages: above 87.5 °C the value of $P_{tot}$ derates linearly with 4.0 mW/K.
For XSON6 packages: above 118 °C the value of $P_{tot}$ derates linearly with 7.8 mW/K.



© NXP B.V. 2009. All rights reserved.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | - | - | 100 | ns/V |
| | | $V_{CC}$ = 5.0 V ± 0.5 V | - | - | 20 | ns/V |

## 10. Static characteristics

**Table 7. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC}$ = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC}$ = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = –50 µA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = –50 µA; $V_{CC}$ = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O$ = –50 µA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = –4.0 mA; $V_{CC}$ = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | $I_O$ = –8.0 mA; $V_{CC}$ = 4.5 V | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 50 µA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 µA; $V_{CC}$ = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 µA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | $I_O$ = 8.0 mA; $V_{CC}$ = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | 0.25 | - | 2.5 | - | 10 | µA |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 1.0 | - | 10 | - | 40 | µA |
| $C_I$ | input capacitance | | - | 1.5 | 10 | - | 10 | - | 10 | pF |



© NXP B.V. 2009. All rights reserved.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*GND = 0 V; For test circuit see Figure 9.*

| Symbol | Parameter | Conditions | | 25 °C | | | −40 °C to +85 °C | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{pd}$ | propagation delay | A to Y; see Figure 7 | [1] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [2] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.7 | 8.0 | 1.0 | 9.5 | 1.0 | 11.5 | ns |
| | | $C_L$ = 50 pF | | - | 6.6 | 11.5 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 3.4 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| | | $C_L$ = 50 pF | | - | 4.8 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| $t_{en}$ | enable time | $\overline{OE}$ to Y; see Figure 8 | [1] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [2] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 5.0 | 8.0 | 1.0 | 9.5 | 1.0 | 11.5 | ns |
| | | $C_L$ = 50 pF | | - | 6.9 | 11.5 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 3.6 | 5.1 | 1.0 | 6.0 | 1.0 | 6.5 | ns |
| | | $C_L$ = 50 pF | | - | 4.9 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to Y; see Figure 8 | [1] | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [2] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 6.0 | 9.7 | 1.0 | 11.5 | 1.0 | 12.5 | ns |
| | | $C_L$ = 50 pF | | - | 8.3 | 13.2 | 1.0 | 15.0 | 1.0 | 16.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | [3] | | | | | | | | |
| | | $C_L$ = 15 pF | | - | 4.1 | 6.8 | 1.0 | 8.0 | 1.0 | 8.5 | ns |
| | | $C_L$ = 50 pF | | - | 5.7 | 8.8 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| $C_{PD}$ | power dissipation capacitance | per buffer; $C_L$ = 50 pF; f = 1 MHz; $V_I$ = GND to $V_{CC}$ | [4] | - | 9 | - | - | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

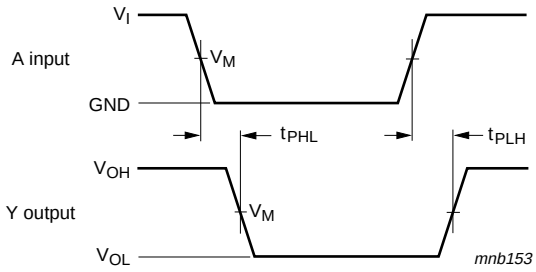
[2] Typical values are measured at $V_{CC}$ = 3.3 V.

[3] Typical values are measured at $V_{CC}$ = 5.0 V.

[4] $C_{PD}$ is used to determine the dynamic power dissipation $P_D$ (µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in Volts.


© NXP B.V. 2009. All rights reserved.

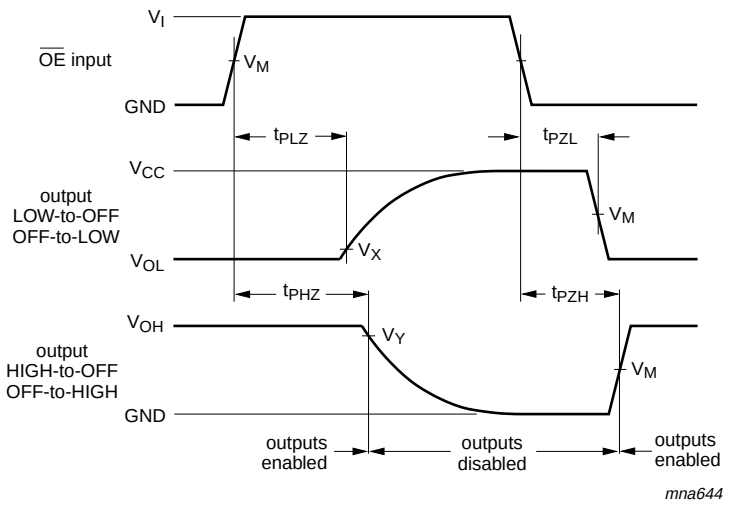
## 12. Waveforms




Measurement points are given in Table 9.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 7. Input (A) to output (Y) propagation delays**




Measurement points are given in Table 9.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

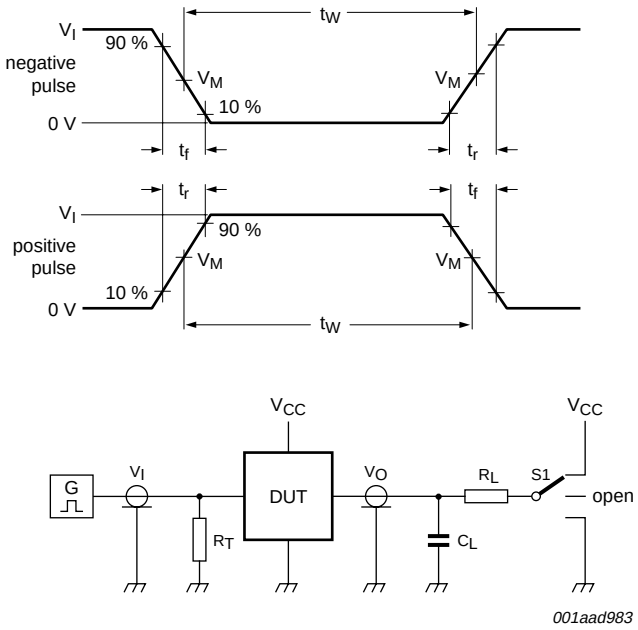
**Fig 8. Enable and disable times**

**Table 9. Measurement points**

| Type | Input | Output | | |
|---|---|---|---|---|
| | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| XC7SH125 | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |



© NXP B.V. 2009. All rights reserved.




Test data is given in Table 10.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

S1 = Test selection switch.

**Fig 9. Test circuit for measuring switching times**

**Table 10. Test data**

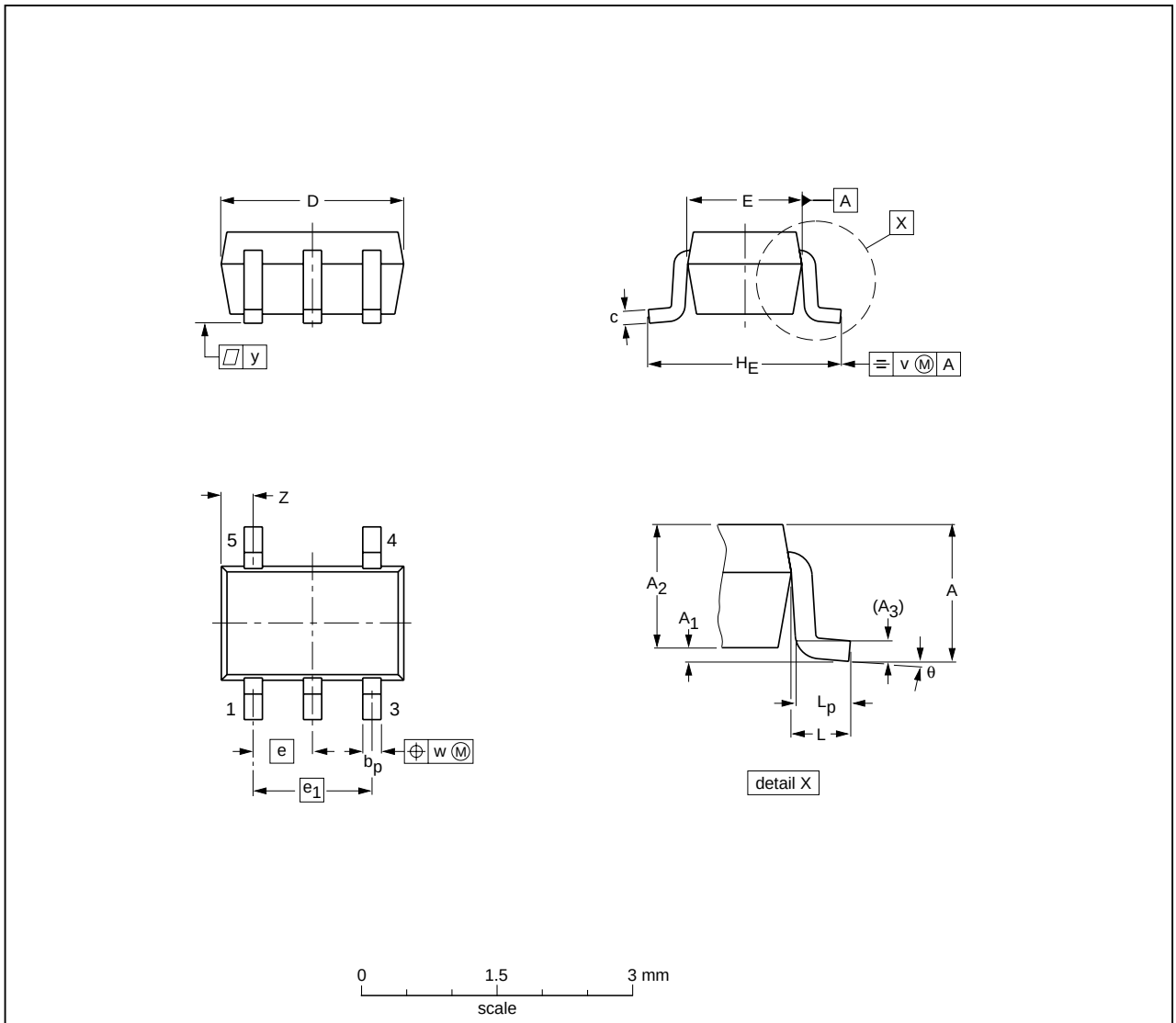
| Type | Input | | Load | | S1 position | | |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| XC7SH125 | $V_{CC}$ | ≤ 3 ns | 15 pF, 50 pF | 1 kΩ | open | GND | $V_{CC}$ |



© NXP B.V. 2009. All rights reserved.

## 13. Package outline

**TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm** **SOT353-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $e_1$ | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.1<br>0 | 1.0<br>0.8 | 0.15 | 0.30<br>0.15 | 0.25<br>0.08 | 2.25<br>1.85 | 1.35<br>1.15 | 0.65 | 1.3 | 2.25<br>2.0 | 0.425 | 0.46<br>0.21 | 0.3 | 0.1 | 0.1 | 0.60<br>0.15 | 7°<br>0° |

**Note**

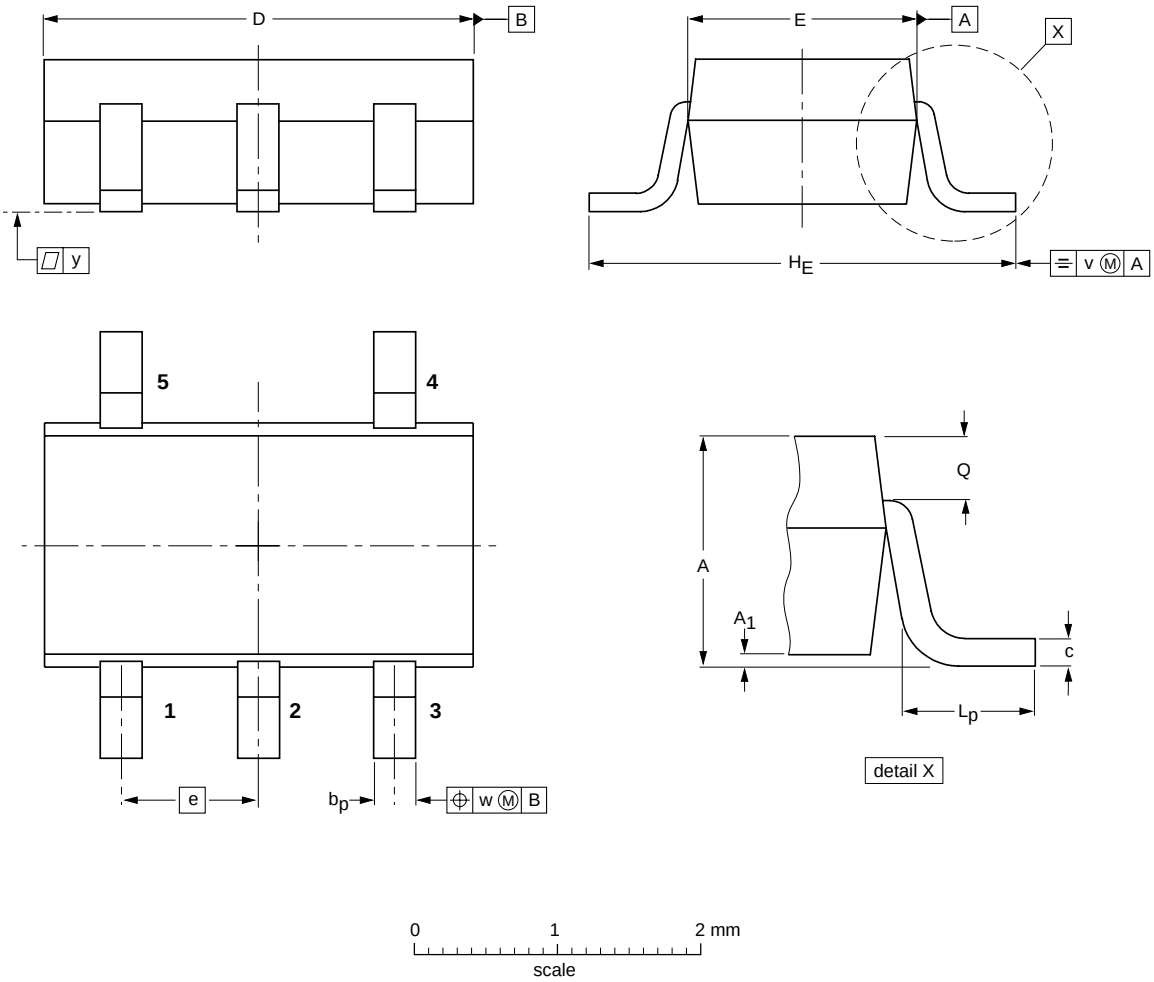
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT353-1 | | MO-203 | SC-88A | | | ~~00-09-01~~<br>03-02-19 |

**Fig 10. Package outline SOT353-1 (TSSOP5)**


© NXP B.V. 2009. All rights reserved.

**Plastic surface-mounted package; 5 leads** **SOT753**




**DIMENSIONS (mm are the original dimensions)**

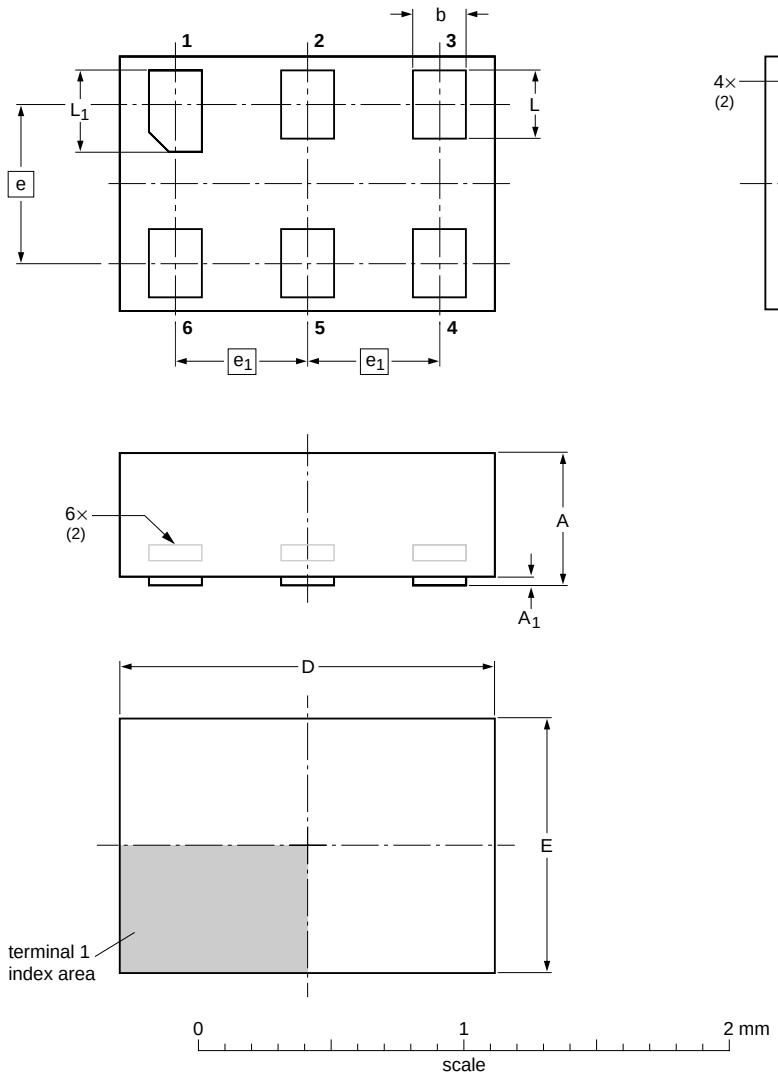
| UNIT | A | $A_1$ | $b_p$ | c | D | E | e | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.100<br>0.013 | 0.40<br>0.25 | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5 | 0.6<br>0.2 | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT753 | | | SC-74A | | | ~~02-04-16~~<br>06-03-16 |

**Fig 11. Package outline SOT753 (SC-74A)**


© NXP B.V. 2009. All rights reserved.

**XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm** **SOT886**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max | A1 max | b | D | E | e | e1 | L | L1 |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.25<br>0.17 | 1.5<br>1.4 | 1.05<br>0.95 | 0.6 | 0.5 | 0.35<br>0.27 | 0.40<br>0.32 |

**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

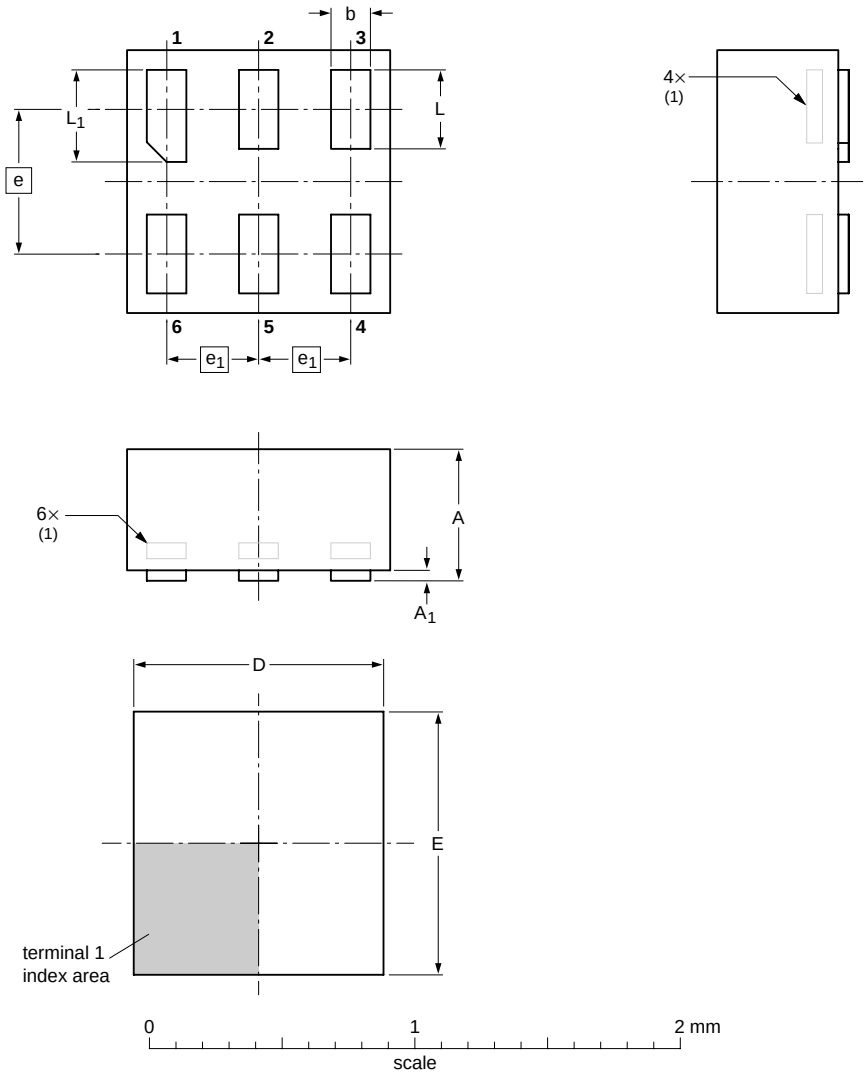
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT886 | | MO-252 | | | | ~~04-07-15~~<br>04-07-22 |

**Fig 12. Package outline SOT886 (XSON6)**



© NXP B.V. 2009. All rights reserved.

**XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm** **SOT891**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ max | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.20<br>0.12 | 1.05<br>0.95 | 1.05<br>0.95 | 0.55 | 0.35 | 0.35<br>0.27 | 0.40<br>0.32 |

**Note**

1. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT891 | | | | | | ~~05-04-06~~<br>07-05-15 |

**Fig 13. Package outline SOT891 (XSON6)**



© NXP B.V. 2009. All rights reserved.

## 14. Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| XC7SH125_1 | 20090904 | Product data sheet | - | - |



© NXP B.V. 2009. All rights reserved.

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 16.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

## 16.3 Disclaimers

**General —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

# 17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**



© NXP B.V. 2009. All rights reserved.

## 18. Contents


| | | |
|---|---|---|
| **1** | **General description** | **1** |
| **2** | **Features** | **1** |
| **3** | **Ordering information** | **1** |
| **4** | **Marking** | **2** |
| **5** | **Functional diagram** | **2** |
| **6** | **Pinning information** | **2** |
| 6.1 | Pinning | 2 |
| 6.2 | Pin description | 3 |
| **7** | **Functional description** | **3** |
| **8** | **Limiting values** | **3** |
| **9** | **Recommended operating conditions** | **4** |
| **10** | **Static characteristics** | **4** |
| **11** | **Dynamic characteristics** | **5** |
| **12** | **Waveforms** | **6** |
| **13** | **Package outline** | **8** |
| **14** | **Abbreviations** | **12** |
| **15** | **Revision history** | **12** |
| **16** | **Legal information** | **13** |
| 16.1 | Data sheet status | 13 |
| 16.2 | Definitions | 13 |
| 16.3 | Disclaimers | 13 |
| 16.4 | Trademarks | 13 |
| **17** | **Contact information** | **13** |
| **18** | **Contents** | **14** |


Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2009. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 September 2009
Document identifier: XC7SH125_1

founded by

PHILIPS