SONY

CXA2013M

EIAJ Sound Multiplexing Decoder

Description

The CXA2013M is a bipolar IC designed as EIAJ TV sound multiplexing decoder, provides various functions including sound multiplexing demodulation, broadcast mode identification (stereo/bilingual discrimination display), volume, tone control and muting.

Features

- Adjustment free of filter
- Audio multiplexing decoder
- Sound processor
  - — One external input
  - — Bass control
  - — Treble control
  - — Volume control
  - — Balance control

  are all included in a single chip. Almost any sort of signal processing is possible through this IC.
- Separation adjustment, each mode control and sound processor control are possible through I^2C BUS.

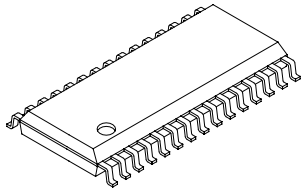
Applications

TVs

Structure

Bipolar silicon monolithic IC

30 pin SOP (Plastic)

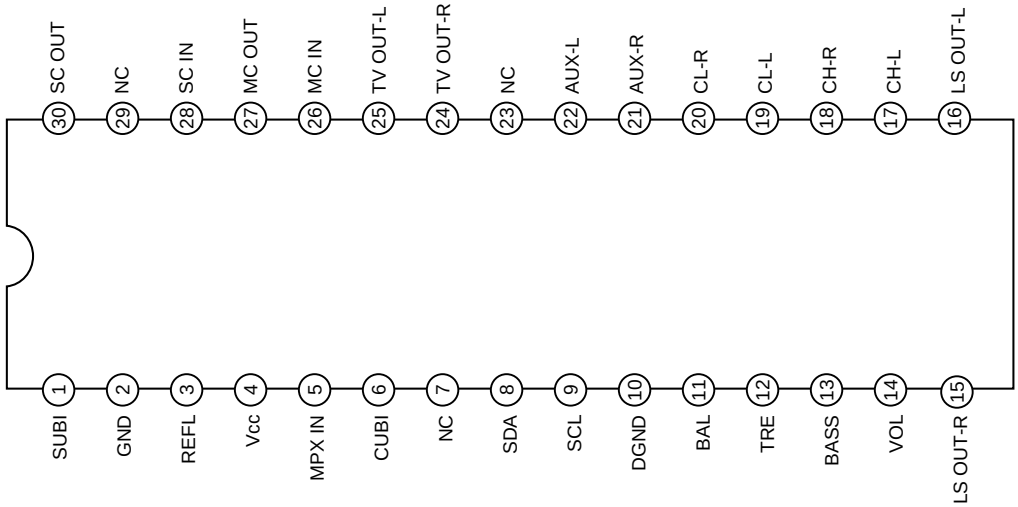


Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1000	mW

Operating Supply Voltage Range 8.5 to 9.5 V

Pin Configuration



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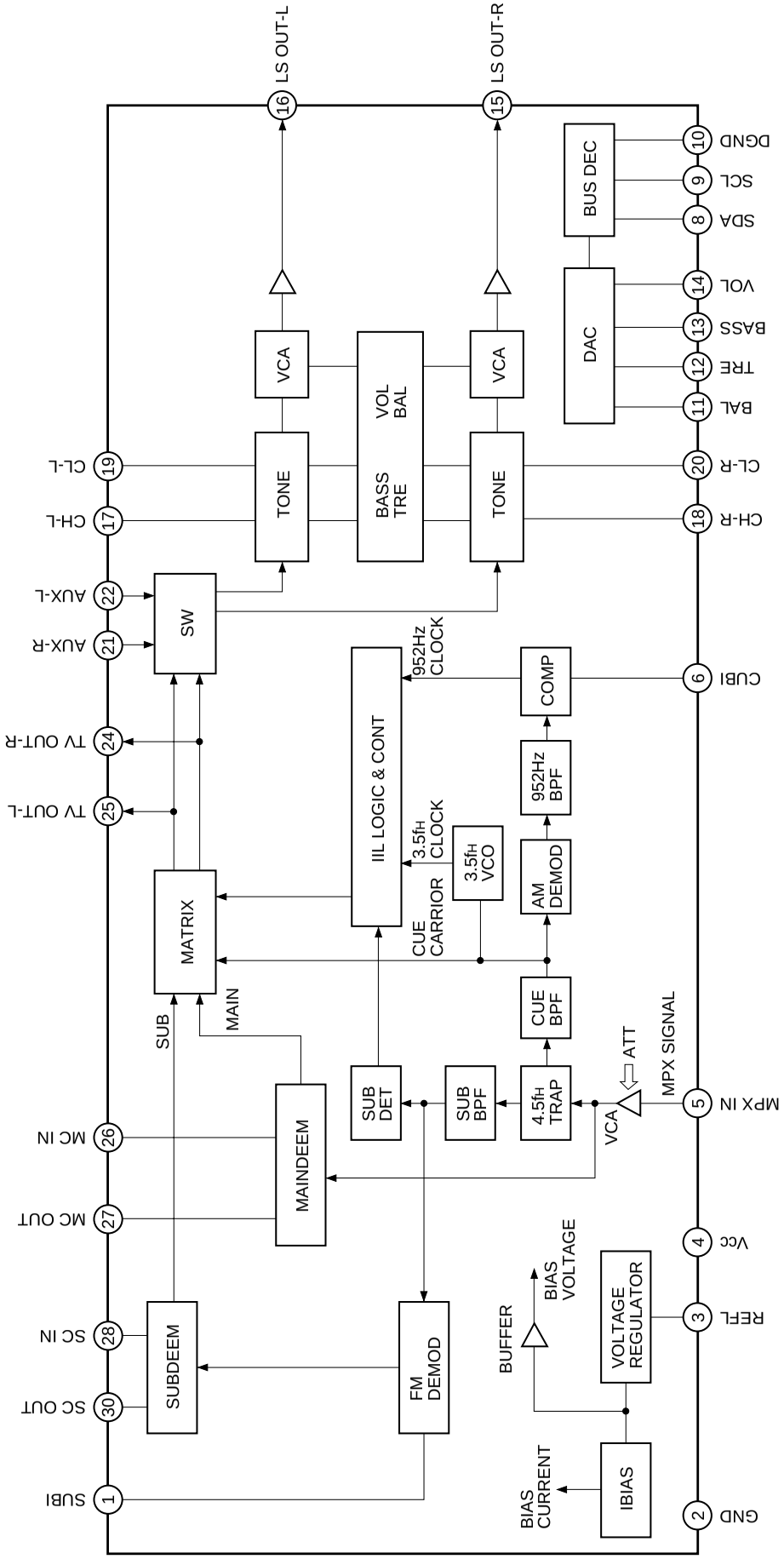
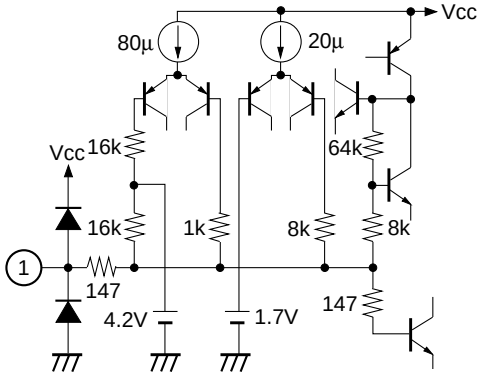
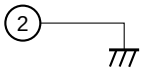
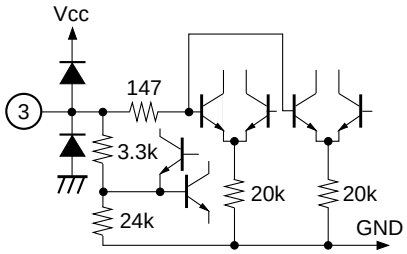
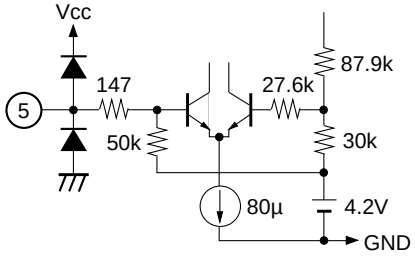
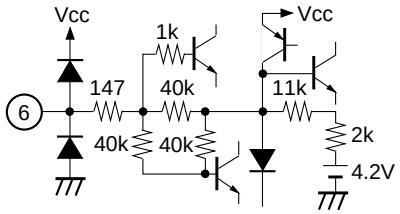
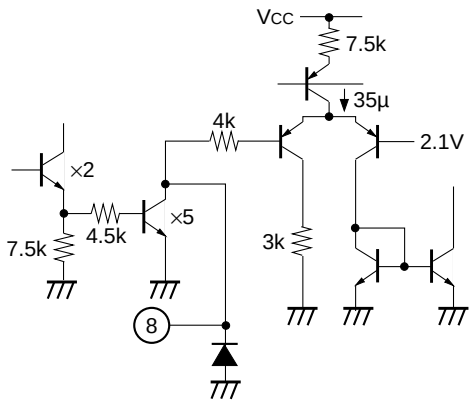
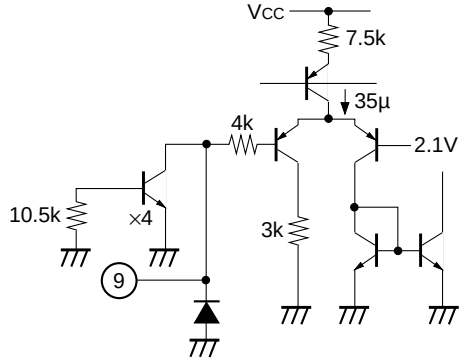
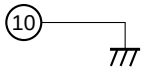
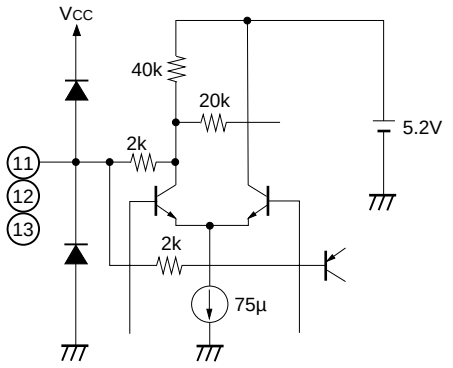
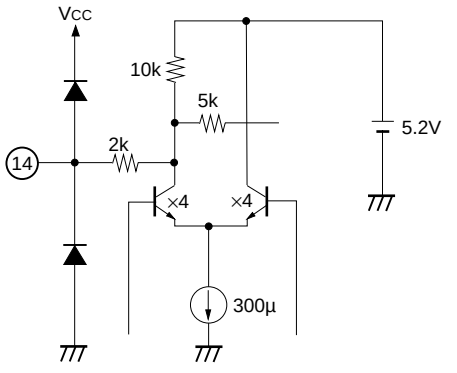
E00Y28A1Y-PS

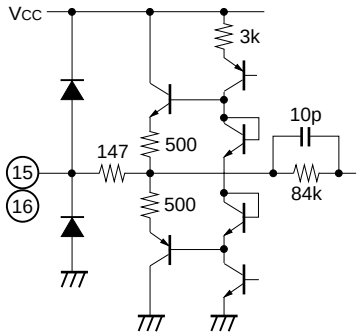
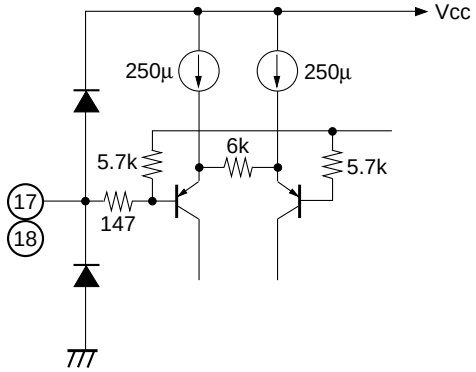
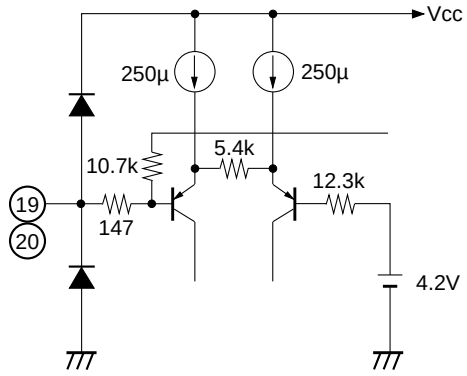
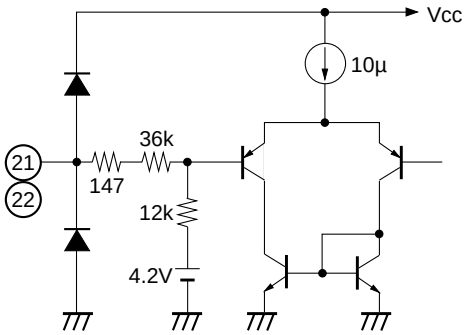
Block Diagram

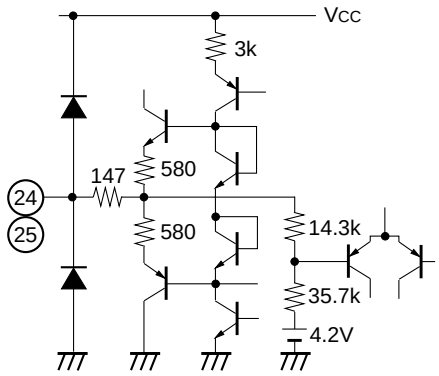
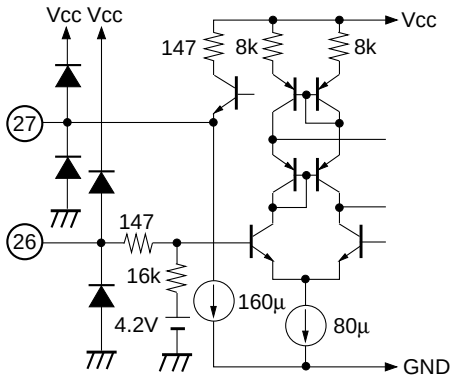
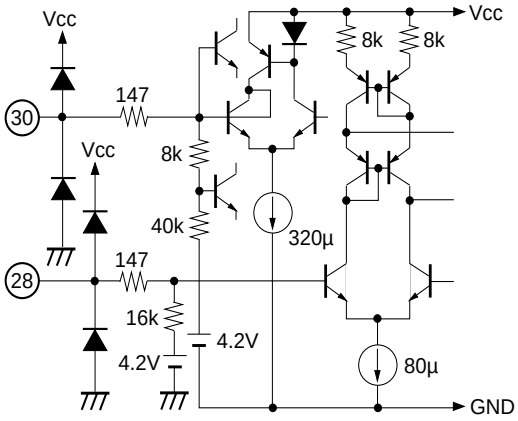


Pin Description (Ta = 25°C, Vcc = 9V)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	SUBI	4.1V		Bias capacitor connection of sub FM detector
2	GND	0		Analog block GND
3	REFL	1.2V		The noise elimination filter connection of internal reference voltage
4	Vcc	—		Power supply
5	MPX IN	4.1V		Sound multiplexing signal input. Typical input level = 110mVrms (monoural 100%)
6	CUBI	4.1V		Bias capacitor connection of Cue pulse generator
7, 23, 29	NC	—	—	—

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
8	SDA	—		Serial data I/O pin V_{IH} > 3.0V V_{IL} < 1.5V
9	SCL	—		Serial clock I/O pin V_{IH} > 3.0V V_{IL} < 1.5V
10	DGND	—		Digital block GND
11	BAL	4.2V		DAC output pin. (BAL) Connect LPF capacitance of DAC. Internal impedance is approximately 20kΩ.
12	TRE	4.2V		DAC output pin. (TRE) Connect LPF capacitance of DAC. Internal impedance is approximately 20kΩ.
13	BASS	4.2V		DAC output pin. (BASS) Connect LPF capacitance of DAC. Internal impedance is approximately 20kΩ.
14	VOL	5.2V		DAC output pin. (VOL) Connect LPF capacitance of DAC. Internal impedance is approximately 5kΩ.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	LS OUT-R	4.2V		LSOUT right channel output pin
16	LS OUT-L	4.2V		LSOUT left channel output pin
17	CH-L	4.2V		Treble filter pin (Left channel)
18	CH-R	4.2V		Treble filter pin (Right channel)
19	CL-L	4.2V		Bass filter pin (Left channel)
20	CL-R	4.2V		Bass filter pin (Right channel)
21	AUX-R	4.2V		Right channel external input pin
22	AUX-L	4.2V		Left channel external input pin

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	TV OUT-R	4.2V		TVOUT right channel output pin
25	TV OUT-L	4.2V		TVOUT left channel output pin
26	MC IN	4.1V		DC cut capacitor connection of main signal
27	MC OUT	3.4V		
28	SC IN	4.1V		DC cut capacitor connection of sub signal
30	SC OUT	3.9V		

Electrical Characteristics

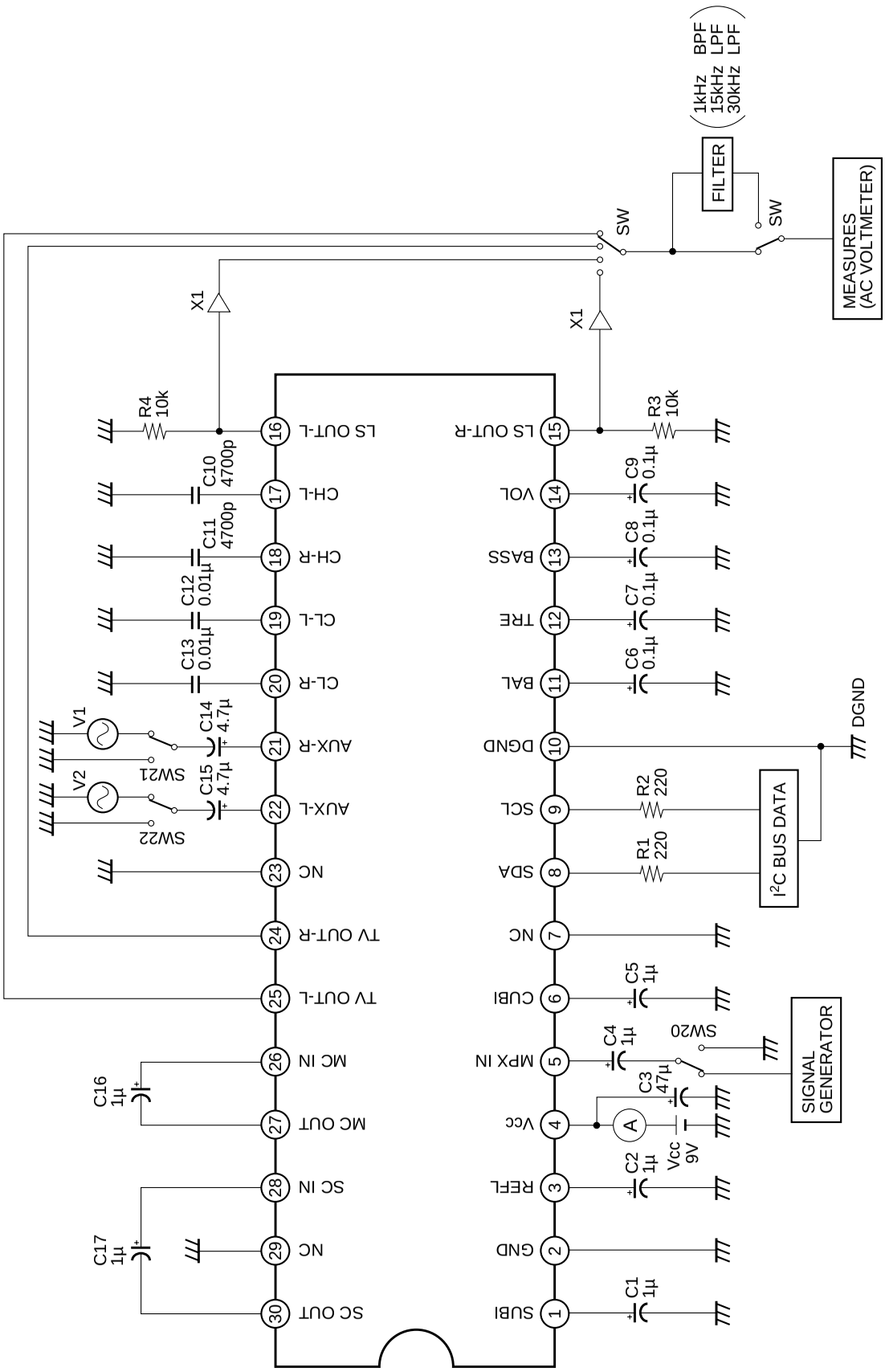
(Ta = 25°C, V_{CC} = 9V)

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
1	Current consumption	Icc		—	No input			4	30	43	60	mA
2	MPX input level	Vin		5	MONO 1kHz, 100% mod.			5	—	110	—	mVrms
3	MPX input level range	Vrange		—	—			—	–3	—	3	dB
4	MONO output level	Vmain	MONO	5	MONO 1kHz 100% mod. Sub: Career OFF, Cue: OFF			24/25	400	500	600	mVrms
5	MONO frequency response	Fcmain	MONO	5	MONO 10kHz 100% mod. Sub: Career OFF, Cue: OFF	20 log ('10k'/'1k')		24/25	–15.4	–13.4	–11.4	dB
6	MONO distortion	THDm	MONO	5	MONO 1kHz 100% mod. Sub: Career OFF, Cue: OFF		15kLPF	24/25	—	0.2	1.0	%
7	MONO distortion at maximum input	THDmmax	MONO	5	MONO 1kHz 300% mod. Sub: Career OFF, Cue: OFF		15kLPF	24/25	—	0.3	2.0	%
8	MONO S/N	SNmain	MONO	5	MONO 1kHz 100% mod. Sub: Career OFF, Cue: OFF	20 log ('100%'/'0%')	15kLPF	24/25	65	73	—	dB
9	Sub output level	Vsub	BIL	5	SUB 1kHz 100% mod. Main 0% mod., Cue: BIL		15kLPF	24/25	400	500	600	mVrms
10	Sub frequency response	Fcsub	BIL	5	SUB 10kHz 100% mod. Main 0% mod., Cue: BIL	20 log ('10k'/'1k')	15kLPF	24/25	–18.4	–15.9	–13.4	dB
11	Sub distortion	THDsub	BIL	5	SUB 1kHz 100% mod. Main 0% mod., Cue: BIL		15kLPF	24/25	—	1.0	2.0	%
12	Sub S/N	SNsub	BIL	5	SUB 1kHz 100% mod. Main 0% mod., Cue: BIL	20 log ('100%'/'0%')	15kLPF	24/25	59	64	—	dB
13	ST output level L-ch	Vstl	ST	5	ST-L 1kHz 100% mod. Cue: Stereo		15kLPF	25	400	500	600	mVrms
14	ST output level R-ch	Vstr	ST	5	ST-R 1kHz 100% mod. Cue: Stereo		15kLPF	24	400	500	600	mVrms

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
15	ST distortion L-ch	THDstl	ST	5	ST-L 1kHz 100% mod. Cue: Stereo		15kLPF	25	—	0.2	1.5	%
16	ST distortion R-ch	THDstr	ST	5	ST-R 1kHz 100% mod. Cue: Stereo		15kLPF	24	—	0.2	1.5	%
17	ST separation L → R	STLsep	ST	5	ST-L 1kHz 100% mod. Cue: Stereo	20 log ('Lch'/'Rch')	15kLPF	24/25	35	45	—	dB
18	ST separation R → L	STRsep	ST	5	ST-R 1kHz 100% mod. Cue: Stereo	20 log ('Rch'/'Lch')	15kLPF	24/25	35	45	—	dB
19	Cross talk Main → Sub	CTms	BIL	5	Main 1kHz 100% mod. Sub: 0% mod., Cue: BIL	20 log (S0 = '0'/S0 = '1')	1kBPF	24/25	55	58	—	dB
20	Cross talk Sub → Main	CTsm	BIL	5	SUB 1kHz 100% mod. Main 0% mod., Cue: BIL	20 log (S0 = '1'/S0 = '0')	1kBPF	24/25	60	70	—	dB
21	Cross talk Main → Sub BOTH mode	CTmsb	BIL	5	Main 1kHz 100% mod. Sub: 0% mod., Cue: BIL	20 log ('Lch'/'Rch') S1 = '1'	1kBPF	24/25	55	58	—	dB
22	Cross talk Sub → Main BOTH mode	CTsmb	BIL	5	SUB 1kHz 100% mod. Main 0% mod., Cue: BIL	20 log ('Rch'/'Lch') S1 = '1'	1kBPF	24/25	60	70	—	dB
23	Sub residual carrier	CLsub	BIL	5	Main 0% mod. Sub: 0% mod., Cue: BIL			24	—	10	30	mVrms
24	Main residual carrier	CLmain	BIL	5	Main 0% mod. Sub: 0% mod., Cue: BIL			25	—	12	20	mVrms
25	TVOUT mute attenuation	Mutv	MONO	5	MONO 1kHz 100% mod. Sub: Career OFF, Cue: OFF	20 log (MUTE TV = '0'/ MUTE TV = '1')	1kBPF	24/25	—	–80	–70	dB
26	DC offset stereo L-ch	OSstl	ST	5	ST 0% mod. Cue: Stereo	MUTE TV = '1' – MUTE TV = '0'		25	–100	0	100	mV
27	DC offset stereo R-ch	OSstr	ST	5	ST 0% mod. Cue: Stereo	MUTE TV = '1' – MUTE TV = '0'		24	–100	0	100	mV
28	Cue detection sensitivity	THcue	BIL	5	Change Cue level	20 log ('100%mod.'/ 'BIL-on level')		BUS RETURN	9	14	17	dB
29	SUB detection sensitivity	THsub	BIL	5	Change SUB career level	20 log ('100%mod.'/ 'BIL-on level')		BUS RETURN	10	13	18	dB
30	Cue BPF gain	BPcue	—	5	Sine wave 55.069kHz, 8.8mVrms	TEST = '1'		25	330	480	620	mVrms

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
31	4.5f_H trap attenuation level	TR45	—	5	Sine wave 66mVrms	20 log ('31.47kHz'/ '70.8kHz')		1	20	38	—	dB
32	LSOUT output level	Vls	EXT	21/22	Sine wave 1kHz 500mVrms	EXT = '1'		15/16	400	500	630	mVrms
33	LSOUT cross talk EXT → INT	CTls1	INT	21/22	Sine wave 1kHz 500mVrms	20 log (EXT = '1'/EXT = '0')	1kBPF	15/16	62	—	—	dB
34	LSOUT cross talk INT → EXT	CTls2	EXT	5	Main 1kHz 100% mod. Sub: 0% mod. , Cue: BIL	20 log (EXT = '0'/EXT = '1')	1kBPF	15/16	70	—	—	dB
35	LSOUT mute attenuation	MUls	EXT	21/22	Sine wave 1kHz 500mVrms	EXT = '1' MUTE LS = '0'	1kBPF	15/16	—	—	–70	dB
36	LSOUT DC offset	OSls	EXT	21/22	No input	EXT = '1' MUTE LS = '1' – MUTE LS = '0'		15/16	–50	0	50	mV
37	LSOUT S/N	SNls	EXT	21/22	Sine wave 1kHz 500mVrms	EXT = '1'	15kLPF	15/16	65	75	—	dB
38	LSOUT distortion	THDls	EXT	21/22	Sine wave 1kHz 500mVrms	EXT = '1'	15kLPF	15/16	—	0.1	0.5	%
39	BASS maximum boost	TBmax	EXT	21/22	Sine wave 100Hz 500mVrms	EXT = '1' BASS = '1F'		15/16	8.5	11.0	13.5	dB
40	BASS maximum attenuation	TBmin	EXT	21/22	Sine wave 100Hz 500mVrms	EXT = '1' BASS = '0'		15/16	–13.5	–11.0	–8.5	dB
41	TREBLE maximum boost	TTmax	EXT	21/22	Sine wave 10kHz 500mVrms	EXT = '1' TREBLE = '1F'		15/16	8.5	11.0	13.5	dB
42	TREBLE maximum attenuation	TTmin	EXT	21/22	Sine wave 10kHz 500mVrms	EXT = '1' TREBLE = '0 '		15/16	–13.5	–11.0	–8.5	dB
43	Volume maximum attenuation	VOLmin	EXT	21/22	Sine wave 1kHz 500mVrms	EXT = '1' VOL = '0'	1kBPF	15/16	—	–90	–70	dB
44	Volume minimum noise	VOLminn	EXT	21/22	No input	EXT = '1', 20 log (VOL = '0'/ '500mVrms')	15kLPF	15/16	—	–90	–80	dB

Electrical Characteristics Measurement Circuit



Adjustment method

Separation adjustment

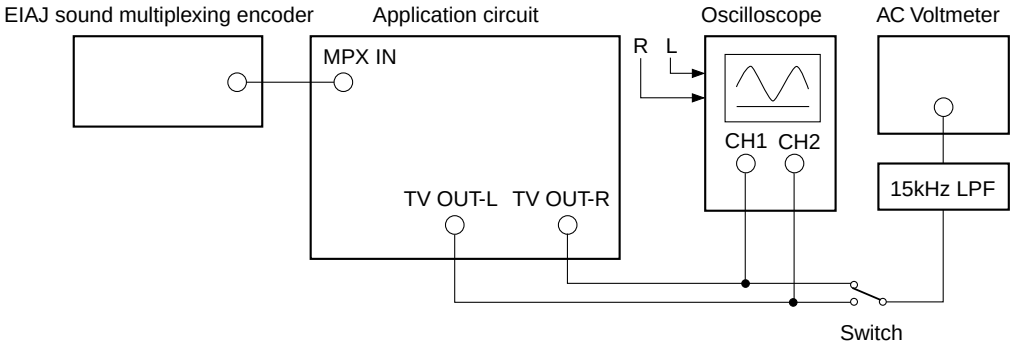


Fig. 1

Procedure

1) Connect components as shown in Fig.1. (TEST = 0)
2) Set the encoder to MONO mode, and input 110mVrms (1kHz 100% modulation) to MPX IN (Pin 5).
3) Set the encoder to stereo mode, and input only left channel signal (1kHz 100% modulation) to MPX IN (Pin 5).
4) Monitor the oscilloscope and AC voltmeter and adjust ATT so that the R-ch is at a minimum. (Separation standard: more than 35dB)

Register Specification

Slave address

SLAVE RECEIVER	SLAVE TRANSMITTER
84H	85H

Register table

SUB ADDRESS	DATA							
MSB LSB	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
****0000	TEST	ATT (7)						
****0001	*	*	EXT	FOMO	S1	S0	MUTE TV	MUTE LS
****0010	*	*	*	BASS (5)				
****0011	*	*	*	TREBLE (5)				
****0100	VOL (8)							
****0101	*	*	BAL (6)					

*: Don't care

Status resigter

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PON	ST	BIL	—	—	—	—	—

Note) When the IC is powered on, the registers "MUTE TV", "MUTE LS" and "VOL" are set to "0".

Description of registers

Control registers

Register	Number of bits	Classification*	Standard setting	Contents
TEST	1	T	0	DAC test mode for VCA, checking Cue BPF mode. 1: TEST
ATT	7	A	34	Adjustment of stereo separation
EXT	1	U	0	Selection of TV mode or external input mode for LSOUT output 1: External
FOMO	1	U	0	Selection of forced MONO mode ON/OFF 1: Forced MONO
S1	1	U	0	Selection of TV OUT, LS OUT output signal
S0	1	U	0	Selection of TV OUT, LS OUT output signal
MUTE TV	1	U	1	Selection of TV OUT mute ON/OFF 0: Mute ON, 1: Mute OFF
MUTE LS	1	U	1	Selection of LS OUT mute ON/OFF 0: Mute ON, 1: Mute OFF
BASS	5	U	10	LS OUT output bass control
TREBLE	5	U	10	LS OUT output treble control
VOL	8	U	FF	LS OUT output signal level control
BAL	6	U	20	LS OUT-L, R output signal level (balance) control

* Classification U: User control
A: Adjustment
T: Test (when IC manufactured)

Status Registers

Register	Number of bits	Contens	
PON	1	POWER ON RESET detection	1: RESET
ST	1	Stereo detection of the MPXIN input signal	1: Stereo
BIL	1	Bilingual detection of the MPXIN input signal	1: Bilingual

Description of Control Registers

TEST (1) : DAC test mode for VCA and checking Cue BPF mode.
Use only for the electrical characteristics inspection process of IC.
0 = Normal mode
1 = Test mode, the Cue signal component through Cue BPF to TV OUT-L.
Output DAC voltage for VCA to TV OUT-R.

ATT (7) : Perform the separation adjustment by varying the signal level input to MPX IN (Pin 5).
Variable range of the input signal: Normal input level ±3.0dB
0 = Level Min.
34 = Center
7F = Level Max.

EXT (1) : Select TV mode or external input mode for LS OUT output
0 = TV mode
1 = External input mode

FOMO (1) : Select ON/OFF forced MONO mode
0 = Forced MONO OFF
1 = Forced MONO ON

S1 (1) : Select output signal for TV OUT, LS OUT

S0 (1) : Select output signal for TV OUT, LS OUT

MUTE TV (1) : Mute TV OUT output
0 = Mute ON
1 = Mute OFF

MUTE LS (1) : Mute LS OUT output
0 = Mute ON
1 = Mute OFF

BASS (5) : LS OUT output bass control
0 = Bass Min.
10 = Bass Center (0dB)
1F = Bass Max.

TREBLE (5) : LS OUT output treble contorl
0 = Treble Min.
10 = Treble Center (0dB)
1F = Treble Max.

VOL (8) : LS OUT output signal level control
0 = Volume Min. (–90dB Typ.)
FF = Volume Max. (0dB)

BAL (6) : LS OUT-L, R output signal level (balance) control
0 = Lch Min., Rch Max.
20 = Center (Lch 0dB, Rch 0dB)
3F = Lch Max., Rch Min.

Description of Mode Control

TV OUT output mode control table (TEST = 0 normal mode)

Input signal	Mode detection		Mode control				TV OUT output	
	ST	BIL	FOMO	S1	S0	MUTE TV	L	R
MONO	0	0	*	*	*	0	MUTE	MUTE
			*	*	*	1	MAIN	MAIN
Stereo	1	0	*	*	*	0	MUTE	MUTE
			1	*	*	1	L + R	L + R
			0	0	0	1	L	R
			0	0	1	1	L	R
			0	1	0	1	L	R
Bilingual	0	1	*	*	*	0	MUTE	MUTE
			*	0	0	1	MAIN	MAIN
			*	0	1	1	SUB	SUB
			*	1	0	1	MAIN	SUB

*: Don't care

LS OUT output mode control table (TEST = 0 normal mode, EXT = 0 TV mode)

Input signal	Mode detection		Mode control				LS OUT output	
	ST	BIL	FOMO	S1	S0	MUTE LS	L	R
MONO	0	0	*	*	*	0	MUTE	MUTE
			*	*	*	1	MAIN	MAIN
Stereo	1	0	*	*	*	0	MUTE	MUTE
			1	*	*	1	L + R	L + R
			0	0	0	1	L	R
			0	0	1	1	L	R
			0	1	0	1	L	R
Bilingual	0	1	*	*	*	0	MUTE	MUTE
			*	0	0	1	MAIN	MAIN
			*	0	1	1	SUB	SUB
			*	1	0	1	MAIN	SUB

*: Don't care

TV OUT/LS OUT output mode control table (TEST = 0 normal mode)

	EXT	TV OUT		LS OUT	
		L	R	L	R
TV mode	0	TV mode Lch	TV mode Rch	TV mode Lch	TV mode Rch
External mode	1	TV mode Lch	TV mode Rch	EXT Lch	EXT Rch

Description of Operation

The sound mutiplexing signal input from Pin 5 is passed through IN AMP and is applied to the Cue BPF, Sub BPF, and Main de-emphasis circuit.

1. Discrimination circuits
   Cue BPF passes only the Cue signal component from the multiplex signal. In the AM demodulator, the signal (AM wave) is AM detected and one of two sine waves is generated, either a 922.5Hz signal for bilingual broadcasts or a 982.5Hz signal for stereo broadcasts.
   In the 952Hz BPF, the 3.5fH carrier component is eliminated from the Cue signal after AM wave detection. The Cue signal, from which the carrier component has been eliminated, is waveform shaped by COMP, with the resulting 922.5Hz or 982.5Hz pulse being applied to the Logic section.
   In the $3.5f_H$ VCO, a $3.5f_H$ pulse locked onto the Cue signal carrier ($3.5f_H$) is created and sent to the Logic section.
   In the Logic section, the broadcast mode is identified using the countdown method. Depending on this result as well as the presence of a SUB signal from SUB detector and the MUTE ON/OFF, MODE switching, and FOMO ON/OFF instructions from CONT, the output switching control signal is created. This signal is used to control the output condition of OUTPUT SW and MAIN OUT.

2. Main circuits
   In MAIN DEEM, de-emphasis is applied to the Main signal component and the Sub and Cue components are removed.
   After passing through the MAIN DEEM, the Main signal is applied to MATRIX, OUTPUT AMP, and MAINOUT.

3. Sub circuits
   In SUB BPF, only the SUB signal component out of multiplex signals is passed through. In the $4.5f_H$ trap, the digital facsimile signal component is removed.
   In FM Demod, the SUB signal is FM demodulated.
   In SUB DEEM, the FM demodulated Sub signal is de-emphasized and the carrier component is removed.
   After passing through SUB DEEM, the Sub signal is applied to MATRIX and OUTPUT AMP.

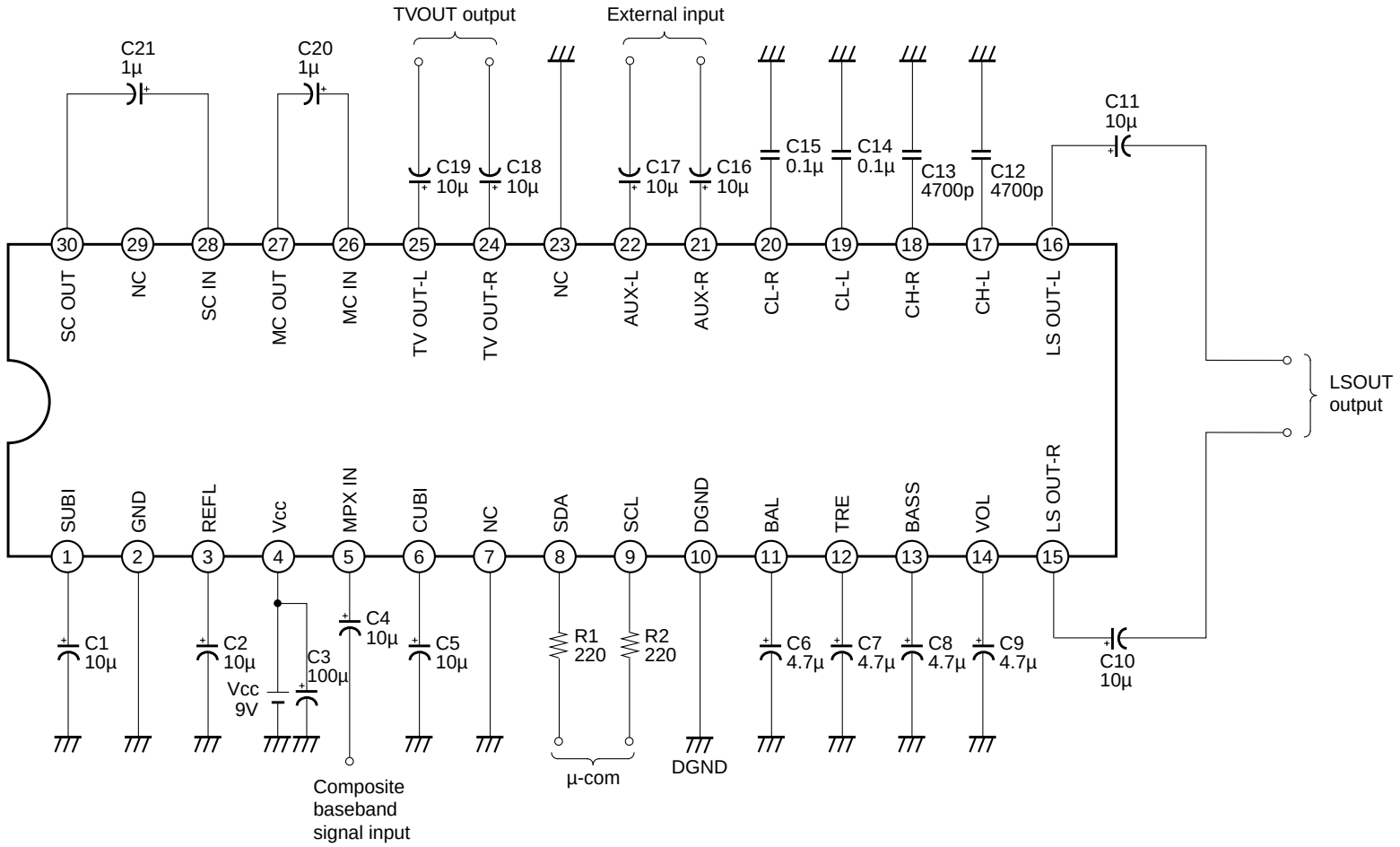
4. MATRIX and output circuits
   In MATRIX, the L and R signals are created by adding and subtracting the Main signal from MAIN DEEM and the Sub signal from SUB DEEM in stereo broadcast.
   In OUTPUT AMP and OUTPUT SW, the output signal is switched under the control of Logic.
   In addition, MAIN OUT always outputs the MAIN signal component, regardless of the broadcast mode.

5. TONE circuit
   Control BASS and TREBLE. Bass and TREBLE characteristics are decided by each C_L and C_H external capacitance.

6. BALANCE, VOLUME curcuit
   Control BALANCE and VOLUME. BALANCE has 64steps and VOLUME has 256 steps.

7. DAC
   DAC is the circuit that control BASS, TREBLE, VOLUME and BALANCE.
   Internal impedance is approximately 20kΩ (approximately 5kΩ for VOLUME).
   Connect the external capacitance for LPF to each pins.

Application Circuit



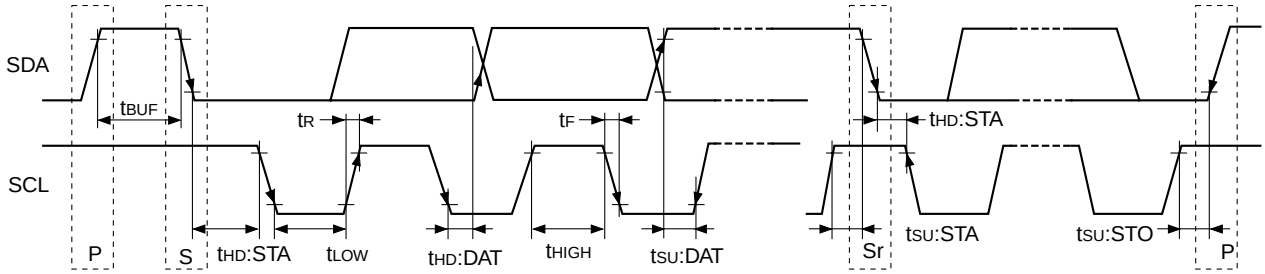
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

I²C Bus Block Items (SDA, SCL)

No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	
3	High level input current	I_{IH}	—	—	10	µA
4	Low level input current	I_{IL}	—	—	10	
5	Low level output voltage SDA (Pin 8) during 3mA inflow	V_{OL}	0	—	0.4	V
6	Maximum inflow current	I_{OL}	3	—	—	mA
7	Input capacitance	C_I	—	—	10	pF
8	Maximum clock frequency	f_{SCL}	0	—	100	kHz
9	Minimum waiting time for data change	t_{BUF}	4.7	—	—	µs
10	Minimum waiting time for start of data transfer	t_{HD}:STA	4.0	—	—	
11	Low level clock pulse width	t_{LOW}	4.7	—	—	
12	High level clock pulse width	t_{HIGH}	4.0	—	—	
13	Minimum waiting time for start preparation	t_{SU}:STA	4.7	—	—	
14	Minimum data hold time	t_{HD}:DAT	0	—	—	
15	Minimum data preparation time	t_{SU}:DAT	250	—	—	ns
16	Rise time	t_R	—	—	1	µs
17	Fall time	t_F	—	—	300	ns
18	Minimum waiting time for stop preparation	t_{SU}:STO	4.7	—	—	µs

I²C bus load conditions: Pull-up resistor 4kΩ (Connect to +5V)
Load capacitor 200pF (Connect to GND)

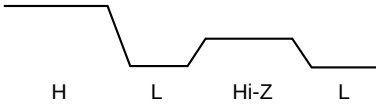
I²C Bus Control Signal



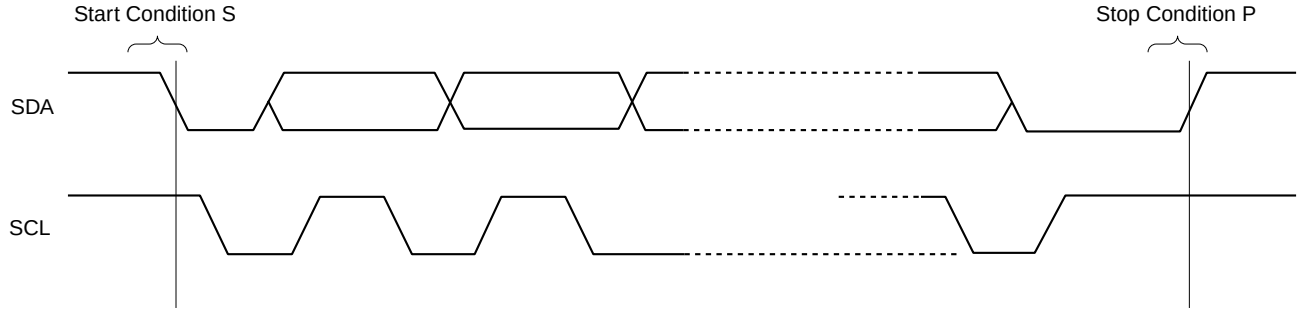
I²C Bus Signal

There are I²C signals, SDA (Serial DATA) and SCL (Serial CLOCK) signals. SDA is a bidirectional signal.

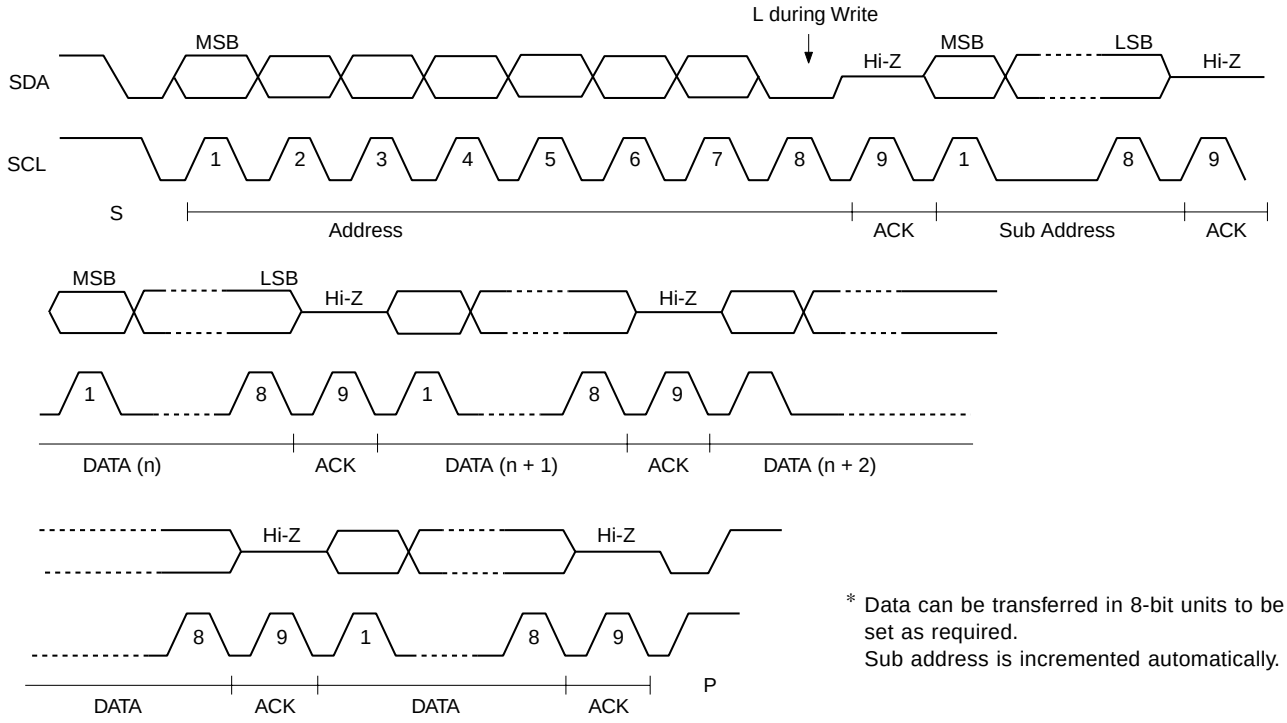
• Accordingly there are 3 values outputs, H, L, and Hi-Z.



• I²C transfer begins with Start Condition and ends with STOP condition.

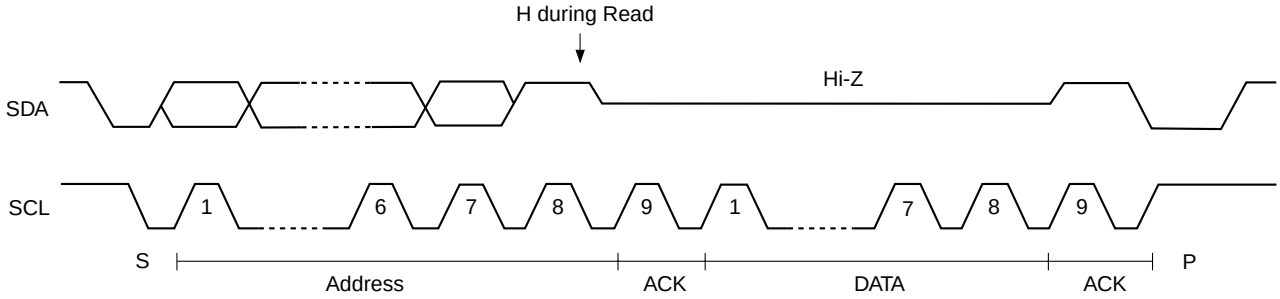


• **I²C data write (Write from I²C controller to the IC)**

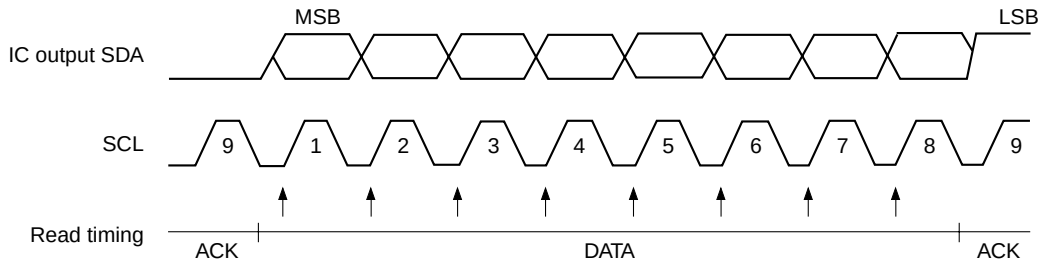


* Data can be transferred in 8-bit units to be set as required.
Sub address is incremented automatically.

• **I²C data read (Read from the IC to I²C controller)**



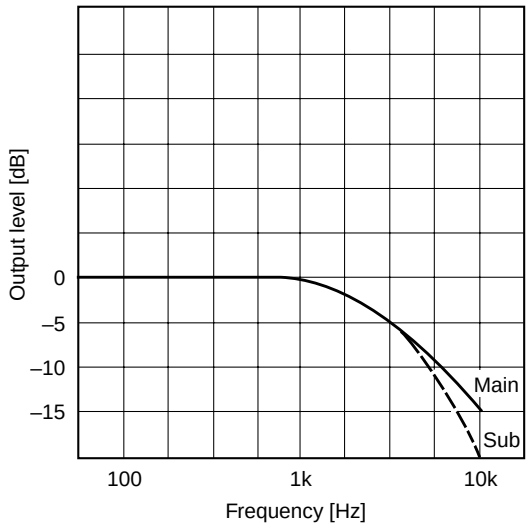
• **Read timing**



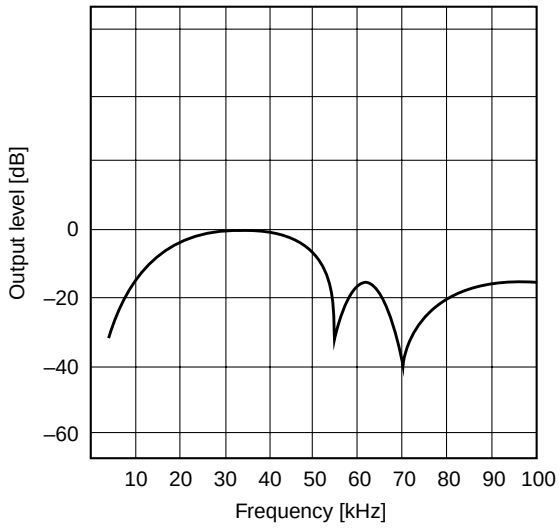
* Data Read is performed during SCL rise.

Example of Representative Characteristics

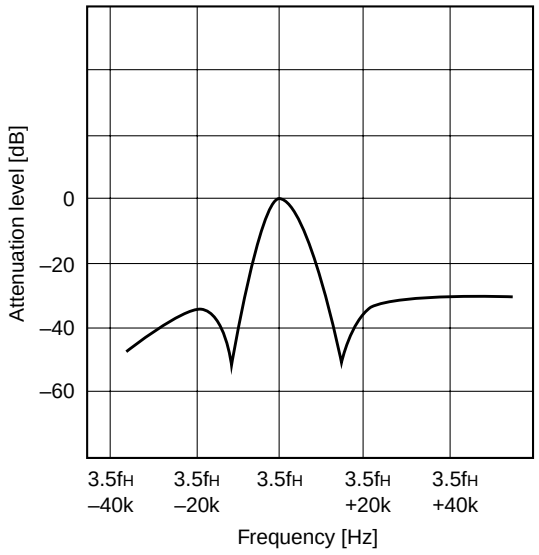
De-emphasis characteristics



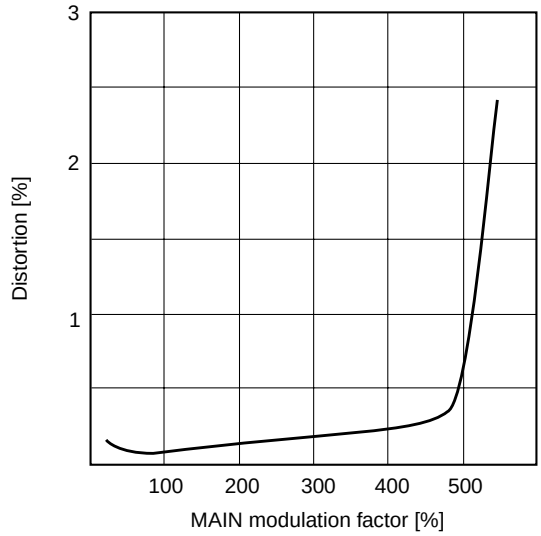
SUB BPF frequency characteristics



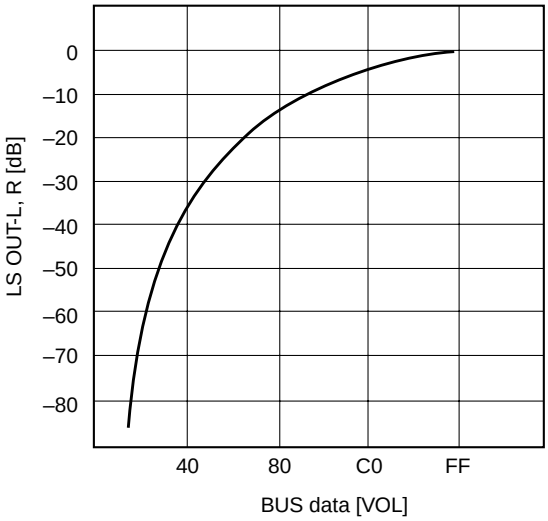
Cue BPF frequency characteristics



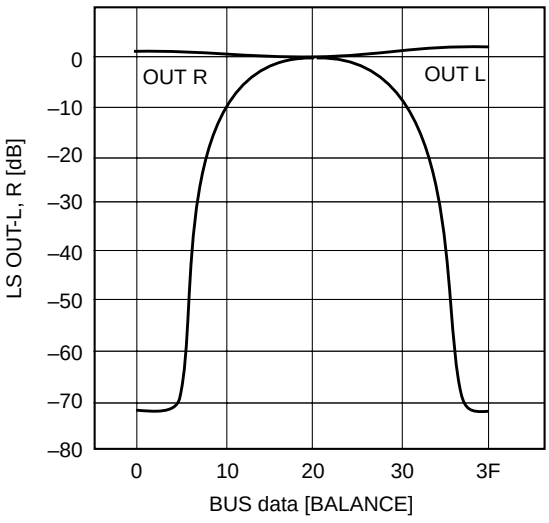
MAIN distortion characteristics



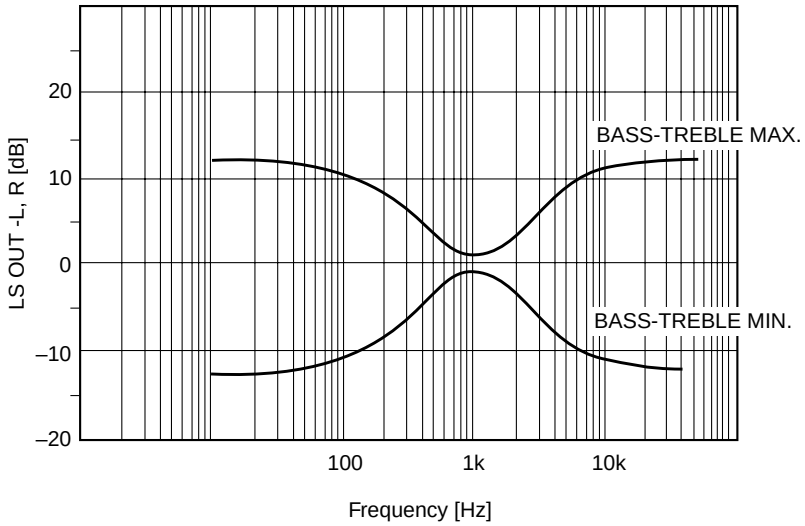
VOL CONTROL characteristics



BALANCE CONTROL characteristics

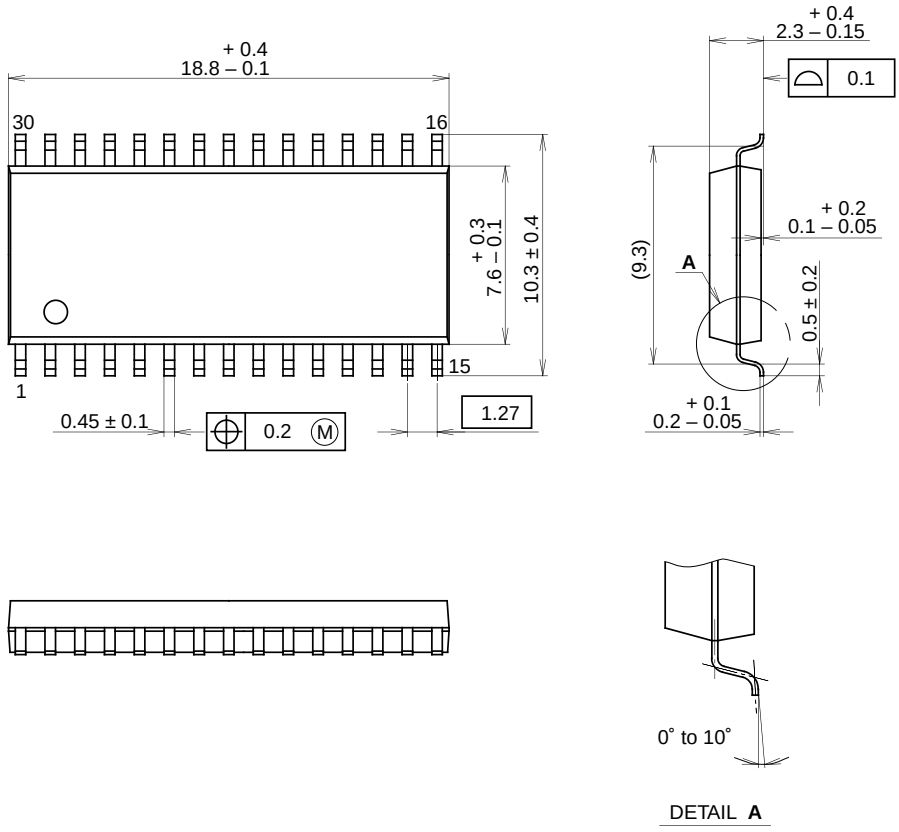


TONE characteristics



Package Outline Unit: mm

30PIN SOP (PLASTIC)



SONY CODE	SOP-30P-L03
EIAJ CODE	SOP030-P-0375
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm