

TPS6116xA Dual-Channel WLED Drivers For Smart Phones

1 Features

- 2.7V to 6.5V input voltage
- Integrated 1.5A/40V MOSFET
- 1.2MHz switching frequency
- Dual current sinks of up to 30mA current each
- 1% typical current matching and accuracy
- Optional 26.5V/37.5V OVP threshold
 - TPS61162A: 26.5V OVP
 - TPS61163A: 37.5V OVP
- Adaptive boost output to WLED voltages
- Very low voltage headroom control (90mV)
- Flexible digital and PWM brightness control
- One-Wire control interface (EasyScale™)
- PWM dimming control interface
- Up to 100:1 PWM dimming ratio
- Up to 9-bit dimming resolution
- Up to 90% efficiency
- Built-in soft start
- PFM mode at light load
- Overvoltage protection
- Built-in WLED open/short protection
- Thermal shutdown
- Supports 4.7μH inductor application

2 Applications

- Smart phones
- PDAs, handheld computers
- GPS receivers
- Backlight for small and media form-factor LCD display with single-cell battery input

3 Description

The TPS61162A and TPS61163A are dual-channel WLED drivers which provide highly integrated solutions for single-cell Li-ion battery powered smart phone backlight. The devices have a built-in high efficiency boost regulator with integrated 1.5A, 40V power MOSFET and support as low as 2.7V input voltage. With two high current-matching capability current sink regulators, the devices can drive up to 10s2p WLED diodes. The boost output can automatically adjust to the WLED forward voltage and allow very low voltage headroom control, thus to improve LED strings efficiency effectively.

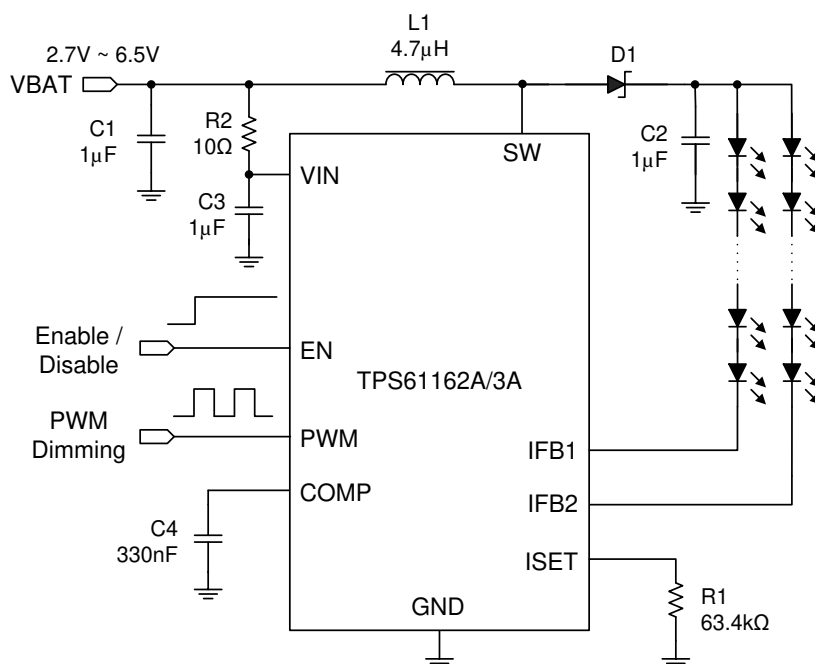
The TPS61162A and TPS61163A support both the PWM dimming interface and one-wire digital EasyScale™ dimming interface and can realize 9-bit brightness code programming.

The TPS61162A and TPS61163A integrate built-in soft start, as well as overvoltage, overcurrent, and thermal shutdown protections.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	OPEN LED PROTECTION
TPS61162A	DSBGA (9)	TPS61162A use 26.5V (typical)
TPS61163A		TPS61163A use 37.5V (typical)

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



Table of Contents

1 Features	1	6.3 Feature Description.....	9
2 Applications	1	6.4 Device Functional Modes.....	13
3 Description	1	6.5 Programming.....	15
4 Pin Configuration and Functions	3	7 Application and Implementation	18
Pin Functions.....	3	7.1 Application Information.....	18
5 Specifications	4	7.2 Typical Application.....	18
5.1 Absolute Maximum Ratings.....	4	7.3 Power Supply Recommendations.....	26
5.2 ESD Ratings.....	4	7.4 Layout.....	26
5.3 Recommended Operating Conditions.....	4	8 Device and Documentation Support	28
5.4 Thermal Information.....	5	8.1 Device Support.....	28
5.5 Electrical Characteristics.....	5	8.2 Related Links.....	28
5.6 EasyScale Timing Requirements.....	6	8.3 Community Resources.....	28
5.7 Typical Characteristics.....	7	8.4 Trademarks.....	28
6 Detailed Description	8	9 Revision History	28
6.1 Overview.....	8	10 Mechanical, Packaging, and Orderable Information	28
6.2 Functional Block Diagram.....	8		

4 Pin Configuration and Functions

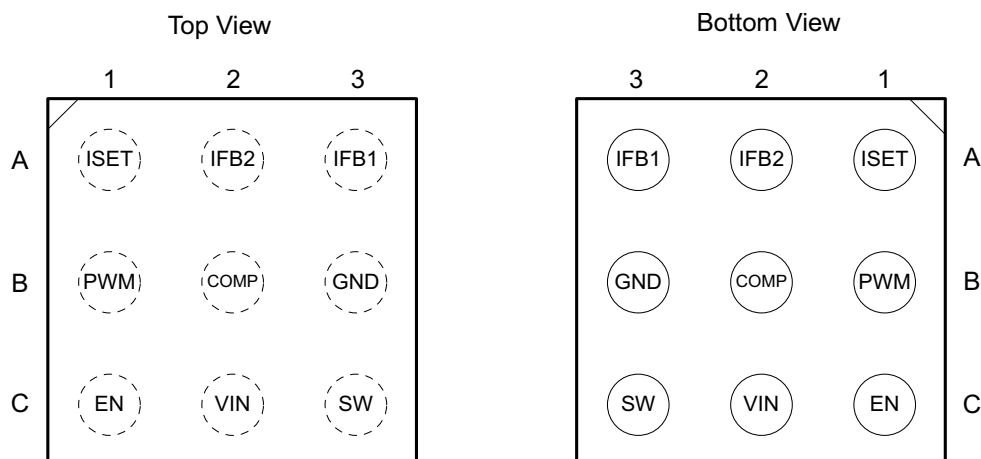


Figure 4-1. YFF Package 9-Pin DSBGA

Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
A1	ISET	I	Full-scale LED current set pin. Connecting a resistor to the pin programs the full-scale LED current.
A2	IFB2	I	Regulated current sink input pin
A3	IFB1	I	Regulated current sink input pin
B1	PWM	I	PWM dimming signal input
B2	COMP	O	Output of the transconductance error amplifier. Connect external capacitor to this pin to compensate the boost loop.
B3	GND	—	Ground
C1	EN	I	Enable control and one-wire digital signal input
C2	VIN	I	Supply input pin
C3	SW	I	Drain connection of the internal power MOSFET

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	VIN, EN, PWM, IFB1, IFB2	−0.3	7	V
	COMP, ISET	−0.3	3	
	SW	−0.3	40	
P _D	Continuous power dissipation	See Section 5.4		
T _J	Operating junction temperature	−40	150	°C
T _{stg}	Storage temperature	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	
		Machine model (MM)	200 (max)	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	2.7		6.5	V
V _{OUT}	Output voltage	TPS61162A			
		TPS61163A			
L	Inductor	4.7		10	μH
C _I	Input capacitor	1			μF
C _O	Output capacitor	1		2.2	μF
C _{COMP}	Compensation capacitor		330		nF
F _{PWM}	PWM dimming signal frequency	10		100	kHz
T _J	Operating junction temperature	−40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS61162A/63A	UNIT
		YFF (DSBGA)	
		9 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	107	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	18.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	18	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

V_{IN} = 3.6V, EN = high, PWM = high, IFB current = 20mA, T_J = –40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
V _{IN} Input voltage range		2.7		6.5	V
V _{VIN_UVLO} Undervoltage lockout threshold	V _{IN} falling		2.2	2.3	V
	V _{IN} rising			2.45	
V _{VIN_HYS} VIN UVLO hysteresis			100		mV
I _q Operating quiescent current into VIN	Device enable, switching 1.2MHz and no load, V _{IN} = 3.6V		1.2	2	mA
I _{SD} Shutdown current	EN = low		1	2	μA
EN and PWM					
V _H EN Logic high		1.2			V
V _L EN Logic Low				0.4	V
V _H PWM Logic high		1.2			V
V _L PWM Logic Low				0.4	V
R _{PD} EN pin and PWM pin internal pulldown resistor		400	800	1600	kΩ
t _{PWM_SD} PWM logic low width to shutdown	PWM high to low	20			ms
t _{EN_SD} EN logic low width to shutdown	EN high to low	2.5			ms
CURRENT REGULATION					
V _{ISET_full} ISET pin voltage	Full brightness	1.204	1.229	1.253	V
K _{ISET_full} Current multiplier	Full brightness		1030		
I _{FB_avg} Current accuracy	I _{ISET} = 20μA, D = 100%, 0°C to 70°C	–2%		2%	
	I _{ISET} = 20μA, D = 100%, –40°C to 85°C	–2.3%		2.3%	
K _M (I _{MAX} – I _{AVG}) / I _{AVG}	D = 100%		1%	2%	
	D = 25%		1%		
I _{IFB_max} Current sink max output current	I _{ISET} = 35μA, each IFBx pin	30			mA
POWER SWITCH					
R _{DS(on)} Switch MOSFET on-resistance	V _{IN} = 3.6V		0.25		Ω
	V _{IN} = 3V		0.3		
I _{LEAK_SW} Switch MOSFET leakage current	V _{SW} = 35V, T _J = 25°C			1	μA

TPS61162A, TPS61163A

SLVSC26B – NOVEMBER 2013 – REVISED MAY 2024

$V_{IN} = 3.6V$, EN = high, PWM = high, IFB current = 20mA, $T_J = -40^{\circ}C$ to $125^{\circ}C$, typical values are at $T_J = 25^{\circ}C$ (unless otherwise noted).

other pins listed).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f _{SW}	Oscillator frequency		1000	1200	1500	kHz
D _{max}	Maximum duty cycle	Measured on the drive signal of switch MOSFET	89%	95%		
BOOST VOLTAGE CONTROL						
V _{IFB_reg}	IFBx feedback regulation voltage	I _{IFBx} = 20mA, measured on IFBx pin which has a lower voltage		90		mV
I _{sink}	COMP pin sink current			12		μA
I _{source}	COMP pin source current			5		μA
G _{ea}	Error amplifier transconductance		30	55	80	μmho
R _{ea}	Error amplifier output resistance			45.5		MΩ
f _{ea}	Error amplifier crossover frequency	5pF connected to COMP pin		1.65		MHz
PROTECTION						
I _{LIM}	Switch MOSFET current limit	D = D _{max} , 0°C to 70°C	1	1.5	2	A
I _{LIM_Start}	Switch MOSFET start-up current limit	D = D _{max}		0.7		A
t _{Half_LIM}	Time window for half current limit			5		ms
V _{OVP_SW}	SW pin overvoltage threshold	TPS61162A	25	26.5	28	V
		TPS61163A	36	37.5	39	
V _{OVP_IFB}	IFBx pin overvoltage threshold	Measured on IFBx pin	4.2	4.5	5	V
V _{ACKNL}	Acknowledge output voltage low Open drain, R _{pullup} = 15kΩ to V _{IN} (2)				0.4	V
THERMAL SHUTDOWN						
T _{shutdown}	Thermal shutdown threshold			160		°C
T _{hys}	Thermal shutdown hysteresis			15		°C

- (1) To select EasyScale interface, after t_{es_delay} delay from EN low to high, drive EN pin to low for more than t_{es_det} before t_{es_win} expires.
- (2) Acknowledge condition active 0, this condition is only applied when the RFA bit is set to 1. To use this feature, master must have an open drain output, and the data line needs to be pulled up by the master with a resistor load.

5.6 EasyScale Timing Requirements

	MIN	NOM	MAX	UNIT
t_{es_delay}	EasyScale detection delay, measured from EN low to high		100	μs
t_{es_det}	EasyScale detection time, EN pin low time		260	μs
t_{es_win}	EasyScale detection window, easured from EN low to high ⁽¹⁾		1	ms
t_{start}	Start time of program stream		2	μs
t_{EOS}	End time of program stream		360	μs
t_{H_LB}	High time of low bit (Logic 0)		180	μs
t_{L_LB}	Low time of low bit (Logic 0)		$2 \times t_{H_LB}$	μs
t_{H_HB}	High time of high bit (Logic 1)		$2 \times t_{L_HB}$	μs
t_{L_HB}	Low time high bit (Logic 1)		2	μs
$t_{valACKN}$	Acknowledge valid time		2	μs
t_{ACKN}	Duration of acknowledge condition		512	μs

5.7 Typical Characteristics

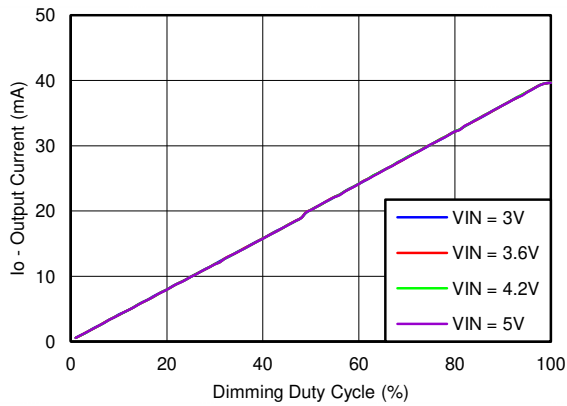


Figure 5-1. Dimming Linearity

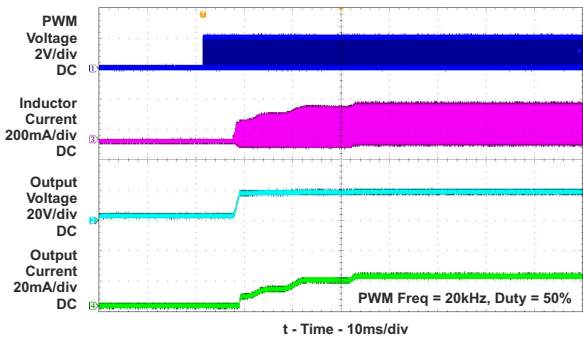


Figure 5-2. Startup Waveform

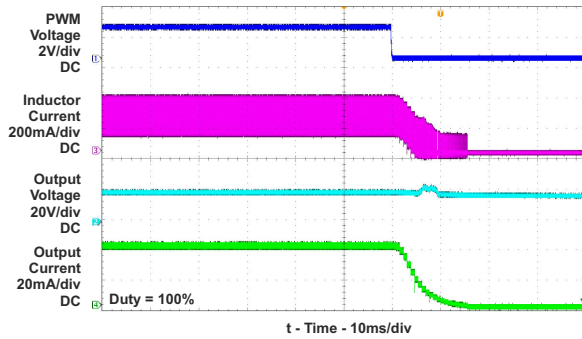


Figure 5-3. Shutdown Waveform

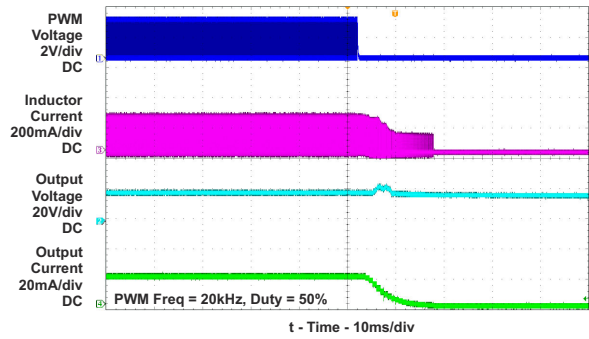


Figure 5-4. Shutdown Waveform

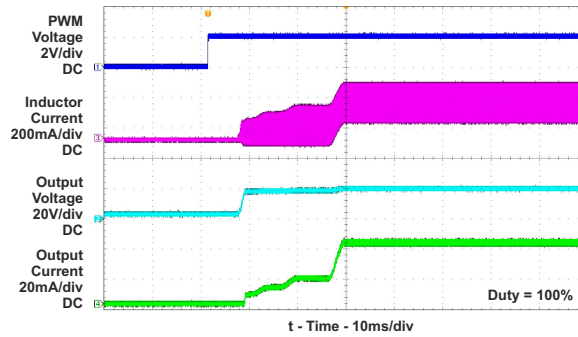


Figure 5-5. Startup Waveform

6 Detailed Description

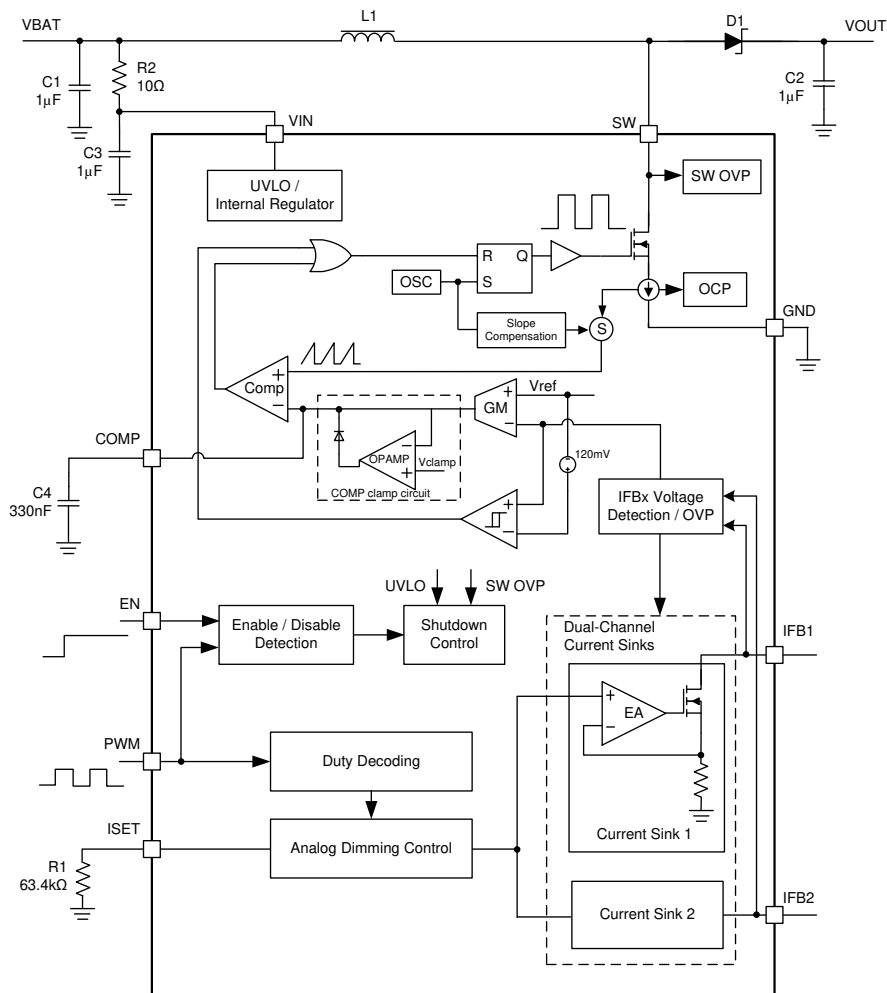
6.1 Overview

The TPS61162A, TPS61163A is a high-efficiency, dual-channel white LED driver for smart-phone backlighting applications. Two current sink regulators of high current-matching capability are integrated in the TPS61162A, TPS61163A to support dual LED strings connection and to improve the current balance and protect the LED diodes when either LED string is open or short.

The TPS61162A, TPS61163A has integrated all of the key function blocks to power and control up to 20 white LED diodes. It includes a 1.5A, 40V boost converter, two current-sink regulators, and protection circuit for overcurrent, overvoltage, and thermal shutdown protection.

In order to provide high brightness backlighting for large size or high resolution smart phone panels, more and more white LED diodes are used. Having all LED diodes in a string improves overall current matching; however, the output voltage of a boost converter will be limited when input voltage is low, and normally the efficiency will drop when output voltage goes very high. Thus, the LED diodes are arranged in two parallel strings.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Boost Converter

The boost converter of the TPS61162A, TPS61163A integrates a 1.5A, 40V low-side switch MOSFET and has a fixed switching frequency of 1.2MHz. The control architecture is based on traditional current-mode Pulse Width Modulation (PWM) control. For operation see the [Section 6.2](#). Two current sinks regulate the dual-channel current, and the boost output is automatically set by regulating voltage on the IFBx pin. The output of error amplifier and the sensed current of switch MOSFET are applied to a control comparator to generate the boost switching duty cycle; slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%.

The forward voltages of two LED strings are normally different due to the LED diode forward voltage inconsistency; thus, the IFB1 and IFB2 voltages are normally different. The TPS61162A, TPS61163A can select out the IFBx pin which has a lower voltage than the other and regulate its voltage to a very low value (90mV typical), which is enough for the two current sinks' headroom. In this way, the output voltage of the boost converter is automatically set and adaptive to LED strings' forward voltages, and the power dissipation of the current sink regulators can be reduced remarkably with this very low headroom voltage.

In order to improve the boost efficiency at light load, Pulse Frequency Modulation (PFM) mode is automatically enabled under light load conditions. When the load current decreases along with the dimming duty, the output of gm amplifier — COMP pin voltage decreases until it is clamped at an internal reference voltage. Because COMP pin voltage controls the inductor peak current, when it is clamped the inductor peak current is also clamped and cannot decrease. As a result, more energy than needed is transferred to the output stage, and the output voltage and IFBx pin voltage increase. An internal hysteresis comparator detects the minimum IFBx pin voltage. When the minimum IFBx voltage is detected as higher than the regulation voltage 90mV by around 120mV, the boost stops switching. Then the output voltage, as well as IFBx pin voltage, decrease. When the minimum IFBx voltage is lower than the hysteresis (around 40mV), the boost switches again. Thus, during PFM mode the boost output trips between the low and high thresholds. When the load increases along with the dimming duty, the COMP pin voltage will exit from the clamped status, and the boost will exit the PFM mode and return to the PWM operation, during which the minimum IFBx pin voltage is regulated at 90mV again. Refer to [Figure 7-10](#) and [Figure 7-11](#) for PFM mode operation.

6.3.2 IFBx Pin Unused

If only one channel is needed, a user can easily disable the unused channel by connecting its IFBx pin to ground. If both IFBx pins are connected to ground, the device will not start up.

6.3.3 Enable and Start-up

In order to enable the device from shutdown mode, three conditions have to be met:

1. POR (Power On Reset, that is, V_{IN} voltage is higher than UVLO threshold);
2. Logic high on EN pin; and
3. PWM signal (logic high or PWM pulses) on PWM pin.

When these conditions are all met, an internal LDO linear regulator is enabled to provide supply to internal circuits and the device can start up.

The TPS61162A, TPS61163A support two dimming interfaces: one-wire digital interface (EasyScale interface) and PWM interface. TPS61162A, TPS61163A begin an EasyScale detection window after start-up to detect which interface is selected. If the EasyScale interface is needed, signals of a specific pattern should be input into EN pin during the EasyScale detection window; otherwise, PWM dimming interface will be enabled (see details in [Section 6.4.1](#)).

After the EasyScale detection window, the TPS61162A, TPS61163A check the status of IFBx pins. If one IFBx pin is detected to connect to ground, the corresponding channel will be disabled and removed from the control loop. Then the soft-start begins, and the boost converter starts switching. If both IFBx pins are shorted to ground, the TPS61162A, TPS61163A will not start up.

Either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms can disable the device, and the TPS61162A, TPS61163A enters into shutdown mode.

If the EasyScale is selected as unique control to enable/disable and change brightness for TPS61162A, TPS61163A, it is required to pull EN pin more than 100ms to enable the TPS61162A, TPS61163A from the previous disable. The 100ms time period can ensure the fully voltage discharge remained on IFBx pin.

6.3.4 Soft Start

Soft start is implemented internally to prevent voltage over-shoot and in-rush current. After the IFBx pin status detection, the COMP pin voltage starts ramp up, and the boost starts switching. During the beginning 5ms (t_{Half_LIM}) of the switching, the peak current of the switch MOSFET is limited at I_{LIM_Start} (0.7A typical) to avoid the input inrush current. After the 5ms, the current limit is changed to I_{LIM} (1.5A typical) to allow the normal operation of the boost converter.

6.3.5 Full-Scale Current Program

The dual channels of the TPS61162A, TPS61163A can provide up to 30mA current each. It does not matter whether either the EasyScale interface or PWM interface is selected, the full-scale current (current when dimming duty cycle is 100%) of each channel should be programmed by an external resistor R_{ISET} at the ISET pin according to [Equation 1](#).

$$I_{FB_full} = \frac{V_{ISET_full}}{R_{ISET}} \times K_{ISET_full} \quad (1)$$

where

- I_{FB_full} , full-scale current of each channel
- $K_{ISET_full} = 1030$ (Current multiple when dimming duty cycle = 100%)
- $V_{ISET_full} = 1.229V$ (ISET pin voltage when dimming duty cycle = 100%)
- R_{ISET} = ISET pin resistor

6.3.6 Brightness Control

The TPS61162A, TPS61163A controls the DC current of the dual channels to realize the brightness dimming. The DC current control is normally referred to as analog dimming mode. When the DC current of LED diode is reduced, the brightness is dimmed.

The TPS61162A, TPS61163A can receive either the PWM signals at the PWM pin (PWM interface) or digital commands at the EN pin (EasyScale interface) for brightness dimming. If the EasyScale interface is selected, the PWM pin should be kept high; if PWM interface is selected, the EN pin should be kept high.

6.3.7 Undervoltage Lockout

An undervoltage lockout circuit prevents the operation of the device at input voltages below undervoltage threshold (2.2 V typical). When the input voltage is below the threshold, the device is shut down. If the input voltage rises by undervoltage lockout hysteresis, the device restarts.

6.3.8 Overvoltage Protection

Overvoltage protection circuitry prevents device damage as the result of white LED string disconnection or shortage.

The TPS61162A/TPS61163A monitors the voltages at SW pin and IFBx pin during each switching cycle. No matter either SW OVP threshold V_{OVP_SW} or IFBx OVP threshold V_{OVP_FB} is reached due to the LED string open or short issue, the protection circuitry will be triggered. Refer to [Figure 6-1](#) and [Figure 6-2](#) for the protection actions.

If one LED string is open, its IFBx pin voltage drops, and the boost output voltage is increased by the control loop as it tries to regulate this lower IFBx voltage to the target value (90mV typical). For the normal string, its current is still under regulation but its IFBx voltage increases along with the output voltage. During the process, either the SW voltage reaches its OVP threshold V_{OVP_SW} or the normal string's IFBx pin voltage reaches the IFBx OVP threshold V_{OVP_FB} , then the protection circuitry will be triggered accordingly.

If both LED strings are open, both IFBx pins' voltages drop to ground, and the boost output voltage is increased by the control loop until reaching the SW OVP threshold V_{OVP_SW} , the SW OVP protection circuitry is triggered, and the device is latched off. Only VIN POR or EN/PWM pin toggling can restart the IC.

One LED diode short in a string is allowed for the TPS61162A, TPS61163A. If one LED diode in a string is short, the normal string's IFBx voltage is regulated to about 90 mV, and the abnormal string's IFBx pin voltage will be higher. Normally with only one diode short, the higher IFBx pin voltage does not reach the IFBx OVP threshold V_{OVP_FB} , so the protection circuitry will not be triggered.

If more than one LED diodes are short in a string, as the boost loop regulates the normal string's IFBx voltage to 90 mV, this abnormal string's IFBx pin voltage is much higher and will reach V_{OVP_FB} , then the protection circuitry is triggered.

The SW OVP protection will also be triggered when the forward voltage drop of an LED string exceeds the SW OVP threshold. In this case, the device turns off the switch FET and shuts down.

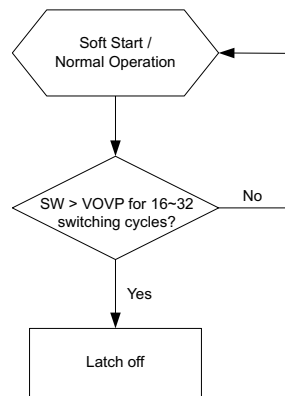
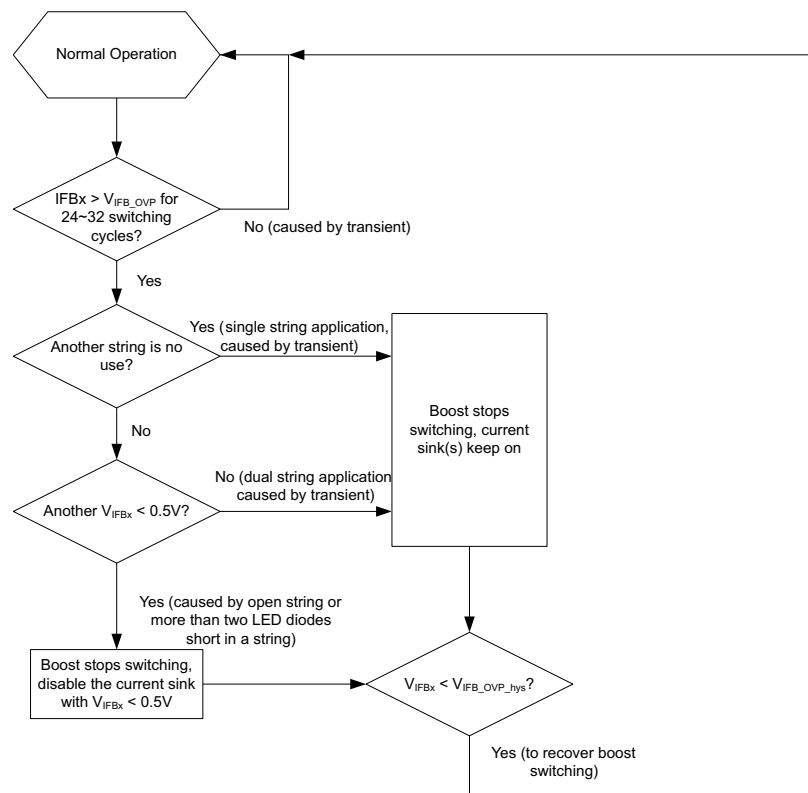


Figure 6-1. SW OVP Action

Figure 6-2. V_{IFBx} OVP Action

6.3.9 Overcurrent Protection

The TPS61162A, TPS61163A have a pulse-by-pulse overcurrent limit. The boost switch turns off when the inductor current reaches this current threshold, and it remains off until the beginning of the next switching cycle. This protects the TPS61162A, TPS61163A and external component under overload conditions.

6.3.10 Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

6.4 Device Functional Modes

6.4.1 One-Wire Digital Interface (EasyScale Interface)

The EN pin features a simple digital interface to allow digital brightness control. The digital dimming interface can save the processor power and battery life as it does not require PWM signals all the time, and the processor can enter idle mode if possible. In order to enable the EasyScale interface, the following conditions must be satisfied, and the specific digital pattern on the EN pin must be recognized by the device every time the TPS61162A, TPS61163A starts up from shutdown mode.

1. V_{IN} voltage is higher than UVLO threshold, and PWM pin is pulled high.
2. Pull EN pin from low to high to enable the TPS61162A, TPS61163A. At this moment, the EasyScale detection window starts.
3. After EasyScale detection delay time (t_{es_delay} , 100 μ s), drive EN to low for more than EasyScale detection time (t_{es_detect} , 260 μ s).

The third step must be finished before the EasyScale detection window (t_{es_win} , 1ms) expires, and once this step is finished, the EasyScale interface is enabled, and the EasyScale communication can start. Refer to [Figure 6-3](#) for a graphical explanation.

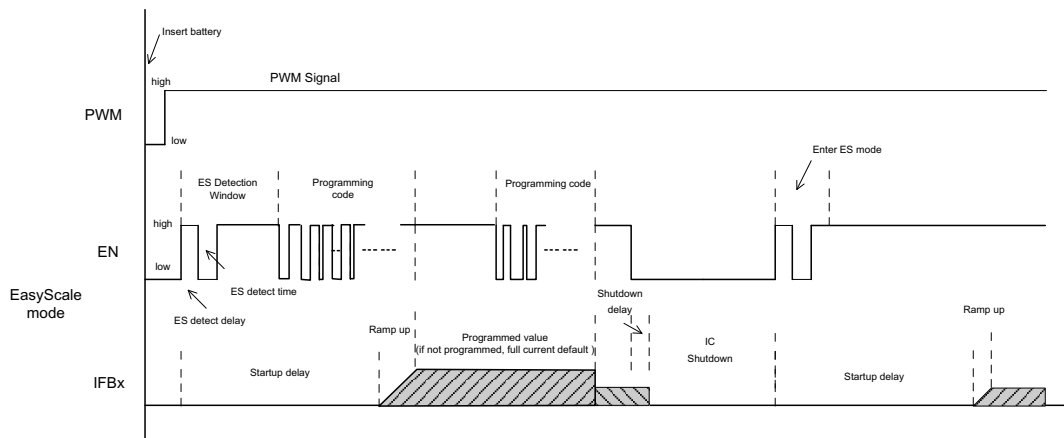


Figure 6-3. Easyscale Interface Detection

The TPS61162A, TPS61163A support 9-bit brightness code programming. By the EasyScale interface, a master can program the 9-bit code D8(MSB) to D0(LSB) to any of 511 steps with a single command. The default code value of D8~D0 is “11111111” when the device is first enabled, and the programmed value will be stored in an internal register and set the dual-channel current according to [Equation 2](#). The code will be reset to default value when the device is shut down or disabled.

$$I_{FBx} = I_{FB_full} \times \frac{\text{Code}}{511} \quad (2)$$

where

- I_{FB_full} : the full-scale LED current set by the R_{ISET} at ISET pin.
- Code: the 9-bit brightness code D8~D0 programmed by EasyScale interface

When the one-wire digital interface at EN pin is selected, the PWM pin can be connected to either the VIN pin or a GPIO (refer to [Section 7.2.4](#)). If PWM pin is connected to VIN pin, EN pin alone can enable and disable the device — pulling EN pin low for more than 2.5ms disables the device; if PWM pin is connected to a GPIO, both PWM and EN signals should be high to enable the device, and either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms disables the device.

6.4.2 PWM Control Interface

The PWM control interface is automatically enabled if the EasyScale interface fails to be enabled during startup. In this case, the TPS61162A, TPS61163A receives PWM dimming signals on the PWM pin to control the backlight brightness. When using PWM interface, the EN pin can be connected to VIN pin or a GPIO (refer to [Section 7.2.4](#)). If EN pin is connected to VIN pin, PWM pin alone is used to enable and disable the device: pulling PWM pin high or apply PWM signals at PWM pin to enable the device and pulling PWM pin low for more than 20ms to disable the device; if EN pin is connected to a GPIO, either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms can disable the device. Only after both EN and PWM signals are applied, the TPS61162A/TPS61163A can start up. Refer to [Figure 6-4](#) for a graphical explanation.

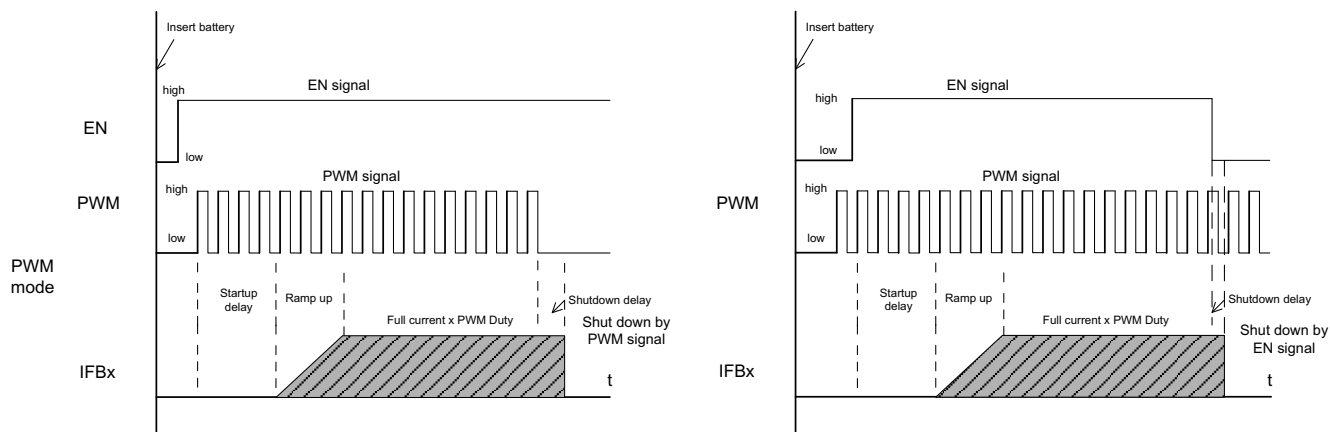


Figure 6-4. PWM Control Interface Detection

When the PWM pin is constantly high, the dual channel current is regulated to full scale according to [Equation 1](#). The PWM pin allows PWM signals to reduce this regulation current according to the PWM duty cycle; therefore, it achieves LED brightness dimming. The relationship between the PWM duty cycle and IFBx current is given by [Equation 3](#).

$$I_{FBx} = I_{FB_full} \times \text{Duty} \quad (3)$$

where

- I_{FBx} is the current of each current sink
- I_{FB_full} is the full-scale LED current
- Duty is the duty cycle information detected from the PWM signals

6.5 Programming

6.5.1 EasyScale Programming

EasyScale is a simple, but flexible, one-pin interface to configure the current of the dual channels. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor and the device is the slave. Figure 6-5 and Table 6-1 give an overview of the protocol used by TPS61162A/TPS61163A. A command consists of 24 bits, including an 8-bit device address byte and a 16-bit data byte. All of the 24 bits should be transmitted together each time, and the LSB bit should be transmitted first. The device address byte D7(MSB)~D0(LSB) is fixed to 0x8F. The data byte includes 9 bits D8(MSB)~D0(LSB) for brightness information and an RFA bit. The RFA bit set to "1" indicates the Request for Acknowledge condition. The Acknowledge condition is only applied when the protocol is received correctly. The advantage of EasyScale compared with other one pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7kBit/sec and up to 160kBit/sec.

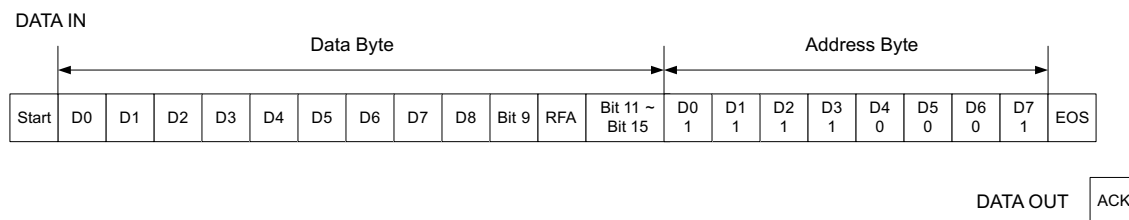


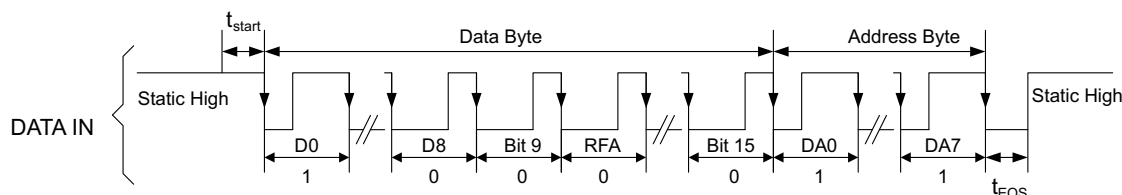
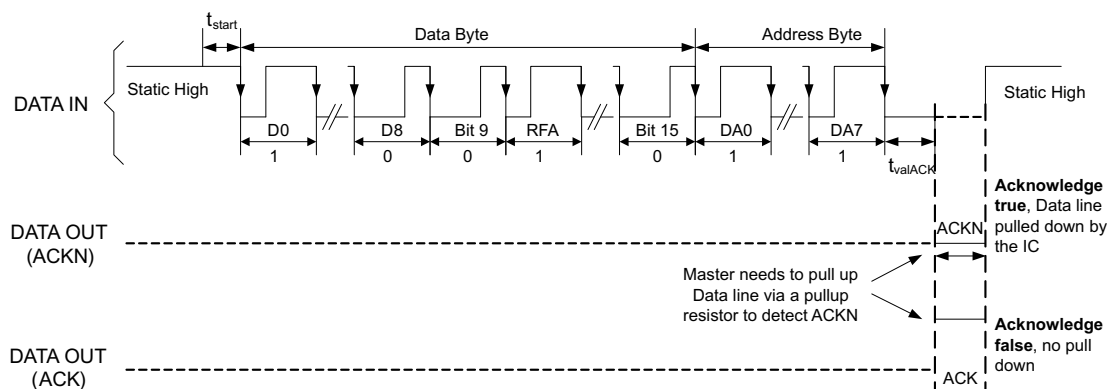
Figure 6-5. Easyscale Protocol Overview

Table 6-1. Easyscale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte (0x8F)	23 (MSB)	DA7	IN	DA7 = 1, MSB of device address
	22	DA6		DA6 = 0
	21	DA5		DA5 = 0
	20	DA4		DA4 = 0
	19	DA3		DA3 = 1
	18	DA2		DA2 = 1
	17	DA1		DA1 = 1
	16	DA0		DA0 = 1, LSB of device address

Table 6-1. Easyscale Bit Description (continued)

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Data Byte	15	Bit 15	IN	No information. Write 0 to this bit.
	14	Bit 14		No information. Write 0 to this bit.
	13	Bit 13		No information. Write 0 to this bit.
	12	Bit 12		No information. Write 0 to this bit.
	11	Bit 11		No information. Write 0 to this bit.
	10	RFA		Request for acknowledge. If set to 1, device will pull low the data line when it receives the command well. This feature can only be used when the master has an open drain output stage and the data line needs to be pulled high by the master with a pullup resistor; otherwise, acknowledge condition is not allowed and don't set this bit to 1.
	9	Bit 9		No information. Write 0 to this bit.
	8	D8		Data bit 8, MSB of brightness code
	7	D7		Data bit 7
	6	D6		Data bit 6
	5	D5		Data bit 5
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0, LSB of brightness code

**Figure 6-6. Easyscale Timing, With RFA = 0****Figure 6-7. Easyscale Timing, With RFA = 1**

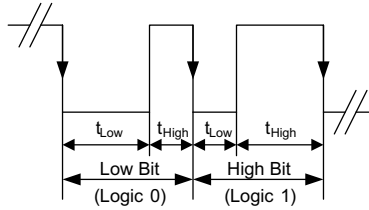


Figure 6-8. Easyscale — Bit Coding

The 24-bit command should be transmitted with LSB first and MSB last. [Figure 6-6](#) shows the protocol without acknowledge request (Bit RFA = 0), [Figure 6-7](#) with acknowledge request (Bit RFA = 1). Before the command transmission, a start condition must be applied. For this, the EN pin must be pulled high for at least t_{start} (2 μ s) before the bit transmission starts with the falling edge. If the EN pin is already at high level, no start condition is needed. The transmission of each command is closed with an End of Stream condition for at least t_{EOS} (2 μ s).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH} (refer to [Figure 6-8](#)). It can be simplified to:

Low Bit (Logic 0): $t_{LOW} \geq 2 \times t_{HIGH}$

High Bit (Logic 1): $t_{HIGH} \geq 2 \times t_{LOW}$

The bit detection starts with a falling edge on the EN pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW} , the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by setting RFA bit to 1.
- The transmitted device address matches with the device address of the IC.
- Total 24 bits are received correctly.

If above conditions are met, after t_{valACK} delay from the moment when the last falling edge of the protocol is detected, an internal ACKN-MOSFET is turned on to pull the EN pin low for the time t_{ACKN} , which is 512 μ s maximum, then the Acknowledge condition is valid. During the t_{valACK} delay, the master controller keeps the line low; after the delay, it should release the line by outputting high impedance and then detect the acknowledge condition. If it reads back a logic 0, it means the device has received the command correctly. The EN pin can be used again by the master when the acknowledge condition ends after t_{ACKN} time.

The acknowledge condition can only be requested when the master device has an open drain output. For a push-pull output stage, the use of a series resistor in the EN line to limit the current to 500 μ A is recommended to for such cases as:

- An accidentally requested acknowledge, or
- To protect the internal ACKN-MOSFET.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The TPS61162A, TPS61163A provide a complete high-performance LED lighting solution for mobile handsets. They can drive up to 2 strings of white LEDs with up to 10 LEDs per string. A boost converter generates the high voltage required for the LEDs. LED brightness can be controlled either by the PWM dimming interface or by the single-wire EasyScale dimming interface.

7.2 Typical Application

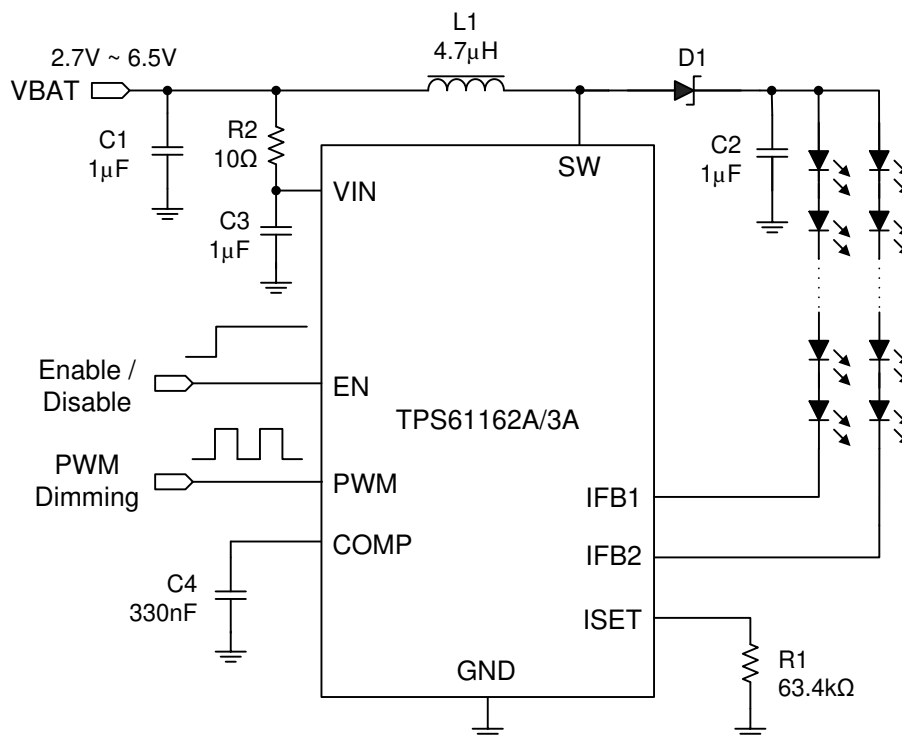


Figure 7-1. TPS61162A/3A Typical Application

7.2.1 Design Requirements

For TPS61162A, TPS61163A typical applications, use the parameters listed in [Table 7-1](#) as the input parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7V to 6.5V
Boost switching frequency	1.2MHz
Efficiency	up to 90%

7.2.2 Detailed Design Procedure

7.2.2.1 Inductor Selection

Because the selection of inductor affects power supply's steady-state operation, transient behavior, loop stability and the boost converter efficiency, the inductor is one of the most important components in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance, and saturation current. The TPS61162A, TPS61163A are designed to work with inductor values from 4.7μH to 10μH to support all applications. A 4.7μH inductor is typically available in a smaller or lower profile package, while a 10μH inductor produces lower inductor ripple. If the boost output current is limited by the overcurrent protection of the device, using a 10μH inductor may maximize the controller's output current capability. A 22μH inductor can also be used for some applications, such as 6s2p and 7s2p, but may cause stability issue when more than eight WLED diodes are connected per string. Therefore, customers need to verify the inductor in their application if it is different from the values in [Section 5.3](#).

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. When selecting an inductor, please make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow [Equation 4](#) to [Equation 6](#) to calculate the inductor's peak current. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage and maximum load current of the application. In order to leave enough design margin, the minimum switching frequency (1 MHz for TPS61162A, TPS61163A), the inductor value with –30% tolerance, and a low power conversion efficiency, such as 80% or lower are recommended for the calculation.

In a boost regulator, the inductor DC current can be calculated as [Equation 4](#).

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (4)$$

where

- V_{OUT} = boost output voltage
- I_{OUT} = boost output current
- V_{IN} = boost input voltage
- η = boost power conversion efficiency

The inductor current peak-to-peak ripple can be calculated as [Equation 5](#).

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times F_S} \quad (5)$$

where

- I_{PP} = inductor peak-to-peak ripple
- L = inductor value
- F_S = boost switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage

Therefore, the peak current I_P seen by the inductor is calculated with [Equation 6](#).

$$I_P = I_{DC} + \frac{I_{PP}}{2} \quad (6)$$

Select an inductor with saturation current over the calculated peak current. If the calculated peak current is larger than the switch MOSFET current limit I_{LIM} , use a larger inductor, such as 10 μ H, and make sure its peak current is below I_{LIM} .

Boost converter efficiency is dependent on the resistance of its current path, the switching losses associated with the switch MOSFET and power diode, and the inductor's core loss. The TPS61162A, TPS61163A has optimized the internal switch resistance; however, the overall efficiency is affected a lot by the inductor's DC Resistance (DCR), Equivalent Series Resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR/ESR conduction losses as well as higher core loss. Normally a datasheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, an inductor with lower DCR/ESR is recommended for TPS61162A, TPS61163A applications. However, there is a trade-off among an inductor's inductance, DCR/ESR resistance, and its footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones. Table 7-2 lists some recommended inductors for the TPS61162A and TPS61163A. Verify whether the recommended inductor can support target application by the calculations above as well as bench validation.

Table 7-2. Recommended Inductors

PART NUMBER	L (μ H)	DCR MAX (m Ω)	SATURATION CURRENT (A)	SIZE (L x W x H mm)	VENDOR
LPS4018-472ML	4.7	125	1.9	4 x 4 x 1.8	Coilcraft
LPS4018-682ML	6.8	150	1.3	4 x 4 x 1.8	Coilcraft
LPS4018-103ML	10	200	1.3	4 x 4 x 1.8	Coilcraft
PIMB051B-4R7M	4.7	163	2.7	5.4 x 5.2 x 1.2	Cyntec
PIMB051B-6R8M	6.8	250	2.3	5.4 x 5.2 x 1.2	Cyntec

7.2.2.2 Schottky Diode Selection

The TPS61162A, TPS61163A demands a low forward-voltage, high-speed and low-capacitance Schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. ONSem MBR0540 and NSR05F40, and Vishay MSS1P4 are recommended for the TPS61162A, TPS61163A.

7.2.2.3 Compensation Capacitor Selection

The compensation capacitor C4 (refer to [Section 7.2.4](#)) connected from the COMP pin to GND, is used to stabilize the feedback loop of the TPS61162A, TPS61163A. A 330nF ceramic capacitor for C4 is suitable for most applications. A 470nF is also OK for some applications and customers are suggested to verify it in their applications.

7.2.2.4 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for the output ripple and loop stability. A 1-μF to 2.2-μF capacitor is recommended for the loop stability consideration. This ripple voltage is related to the capacitor's capacitance and its ESR. Due to its low ESR, $V_{\text{ripple_ESR}}$ could be neglected for ceramic capacitors. Assuming a capacitor with zero ESR, the output ripple can be calculated with [Equation 7](#).

$$V_{\text{ripple}} = \frac{(V_{\text{OUT}} - V_{\text{IN}}) \times I_{\text{OUT}}}{V_{\text{OUT}} \times F_{\text{S}} \times C_{\text{OUT}}} \quad (7)$$

where

- V_{ripple} = peak-to-peak output ripple.

The additional part of ripple caused by the ESR is calculated using $V_{\text{ripple_ESR}} = I_{\text{OUT}} \times R_{\text{ESR}}$ and can be ignored for ceramic capacitors.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50-V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

7.2.3 Application Curves

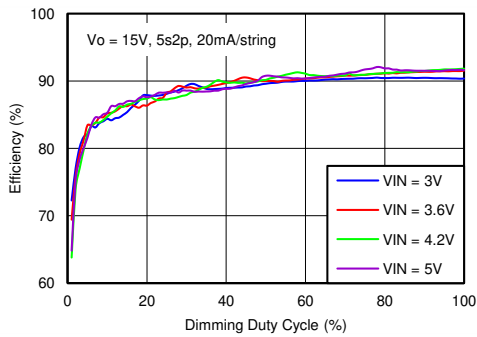


Figure 7-2. Dimming Efficiency

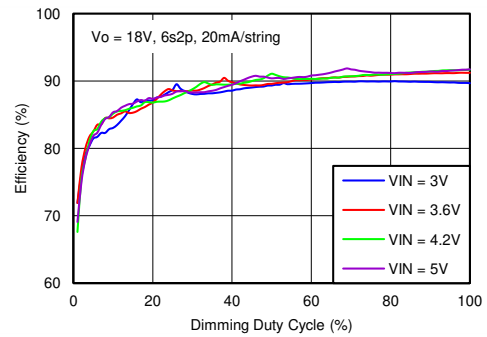


Figure 7-3. Dimming Efficiency

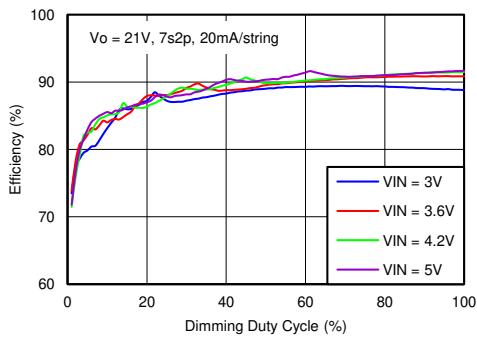


Figure 7-4. Dimming Efficiency

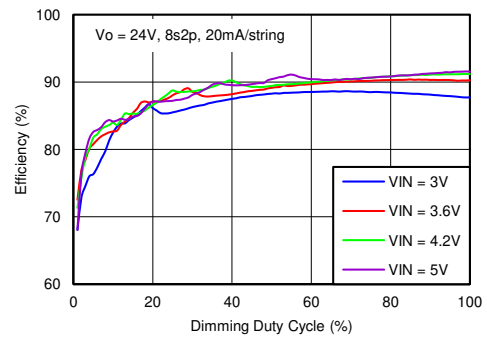


Figure 7-5. Dimming Efficiency

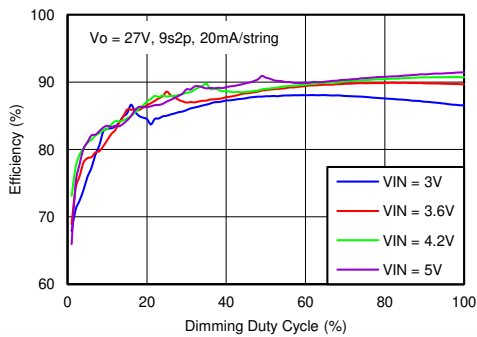


Figure 7-6. Dimming Efficiency

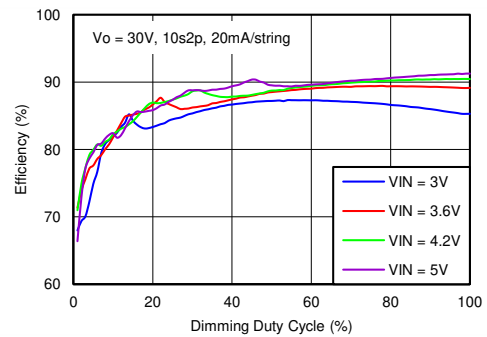


Figure 7-7. Dimming Efficiency

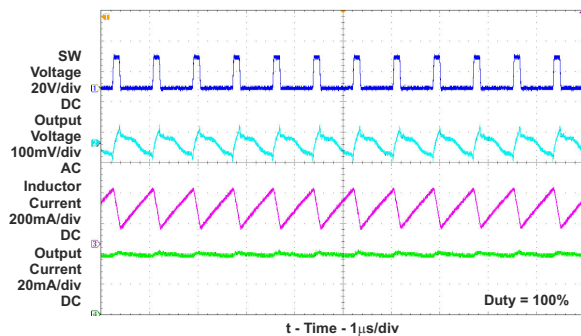


Figure 7-8. Switching Waveform

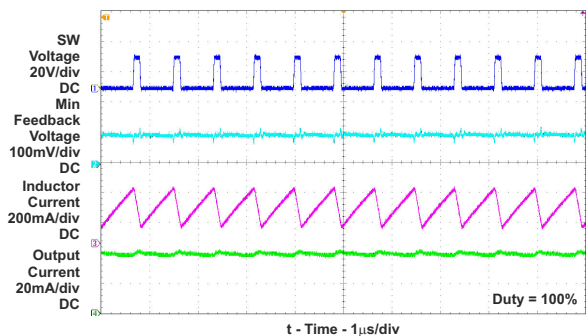


Figure 7-9. Switching Waveform

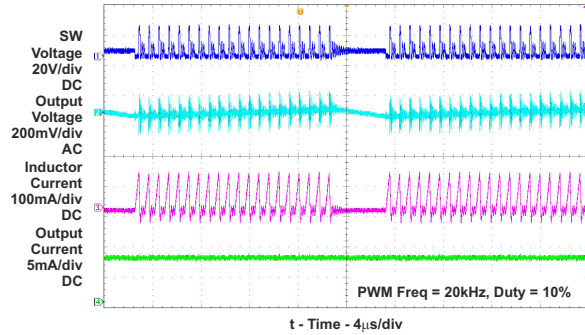


Figure 7-10. Switching Waveform

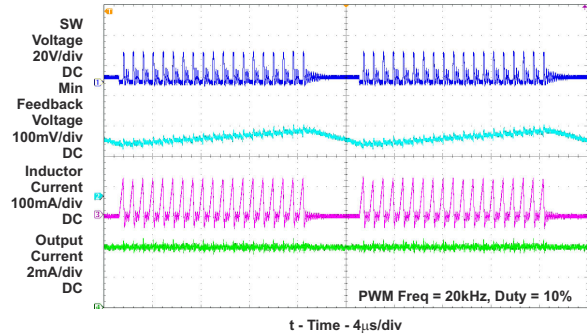


Figure 7-11. Switching Waveform

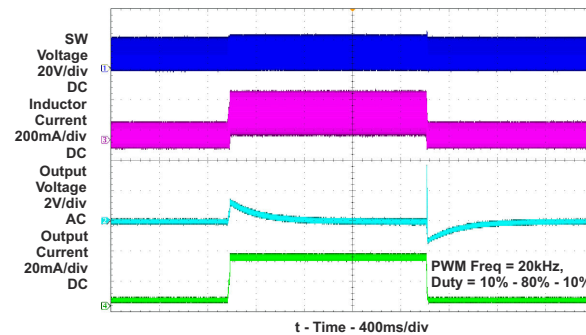


Figure 7-12. Dimming Transient Waveform

7.2.4 Additional Application Circuits

In [Figure 7-13](#) the PWM Interface is enabled, and the PWM input signal is used to adjust the brightness level. The PWM pin as well as the EN pin can be used to enable or disable the TPS61162A, TPS61163A.

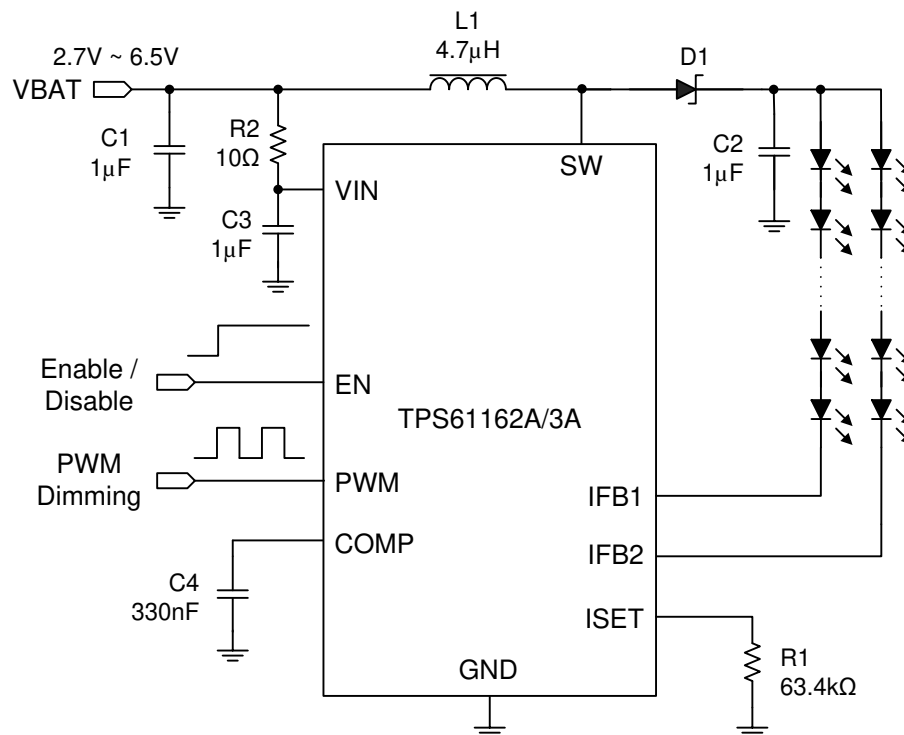


Figure 7-13. TPS61162A/TPS61163A Typical Application

Figure 7-14 shows PWM interface enabled, EN pin connected to VIN, with only the PWM Signal used to adjust the brightness level and to enable or disable the TPS61162A, TPS61163A.

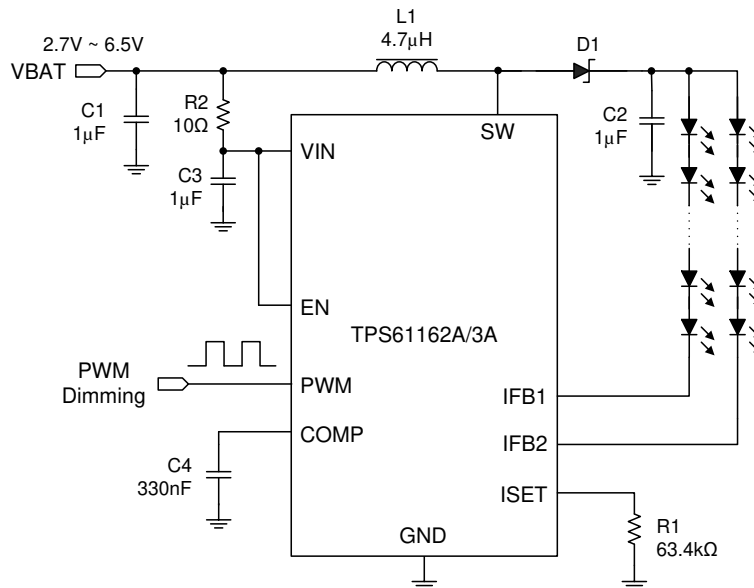


Figure 7-14. TPS61162A/TPS61163A Typical Application

In [Figure 7-15](#) the one-wire digital interface is enabled. Brightness level is adjusted with the PWM pin using EasyScale commands. The PWM signal must remain high for the device to be enabled.

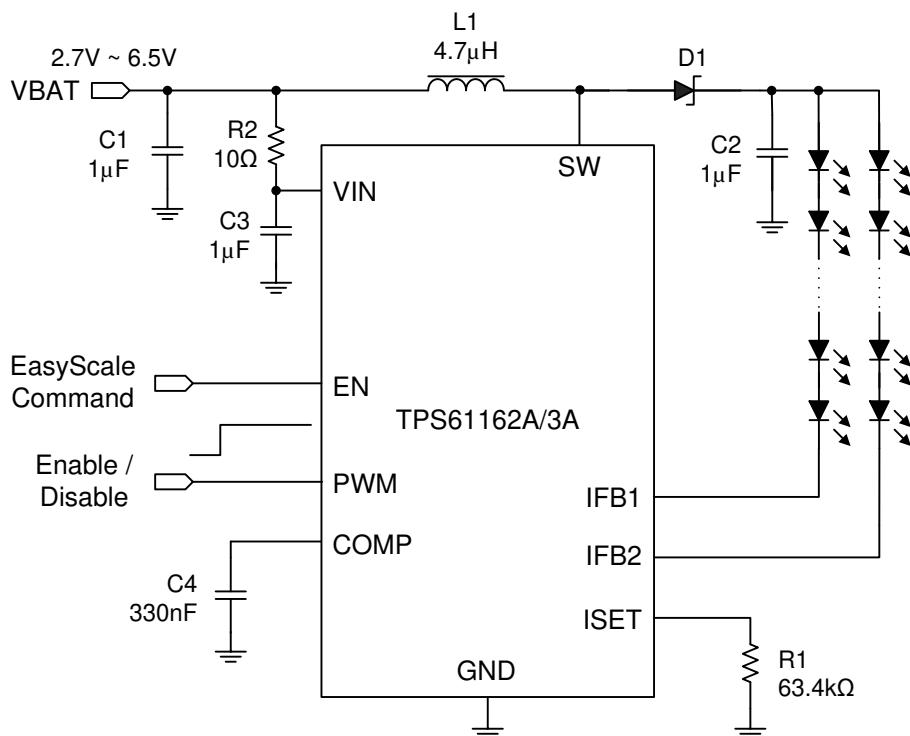


Figure 7-15. TPS61162A/TPS61163A Typical Application

Figure 7-16 shows one-wire digital interface enabled, PWM pin connected to VIN, with only the EN signal used to enable or disable the device. Brightness level adjustments (using EasyScale Commands) can be achieved via the EN pin only.

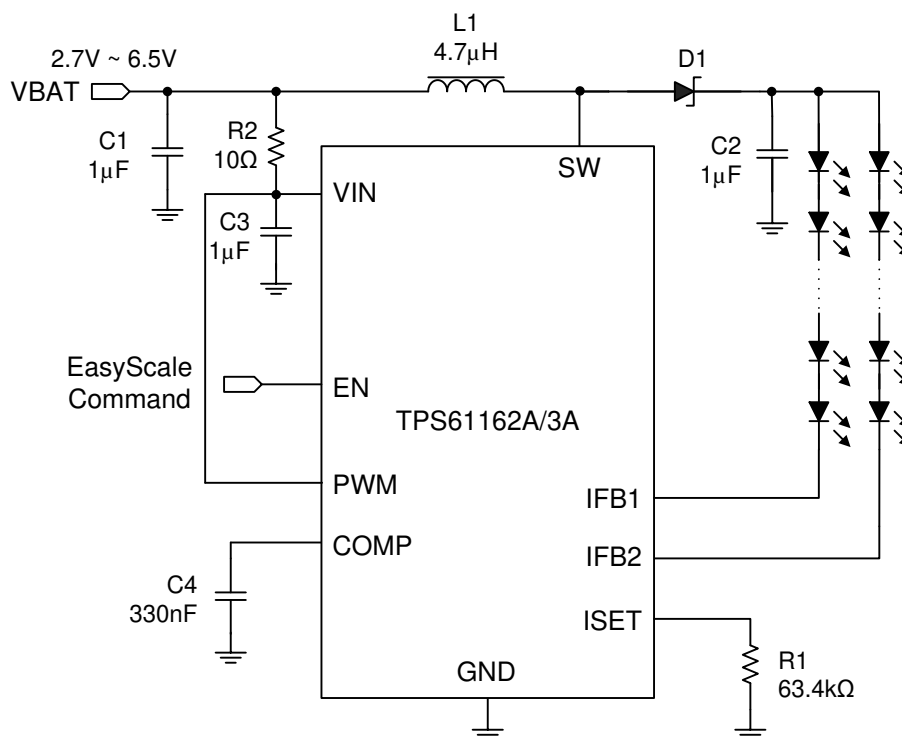


Figure 7-16. TPS61162A/TPS61163A Typical Application

7.3 Power Supply Recommendations

The TPS61162A and TPS61163A are designed to operate from an input supply range of 2.7V to 6.5V. This input supply should be well regulated and be able to provide the peak current required by the LED configuration and inductor selected without voltage drop under load transients (start-up or rapid brightness change). If the input supply is located far from the TPS6116xA additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

7.4 Layout

7.4.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in [Section 7.2.4](#), needs to be close to the inductor, as well as the VIN pin and GND pin in order to reduce the input ripple seen by the device. If possible, choose higher capacitance value for it. If the ripple seen at VIN pin is so large that it affects the boost loop stability or internal circuits operation, R2 and C3 are recommended to filter and decouple the noise. In this case, C3 should be placed as close as possible to the VIN and GND pins. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor and Schottky diode should be kept as short and wide as possible. The trace between Schottky diode and the output capacitor C2 should also be as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the GND pin since there is a large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point close to the GND pin.

7.4.2 Layout Example

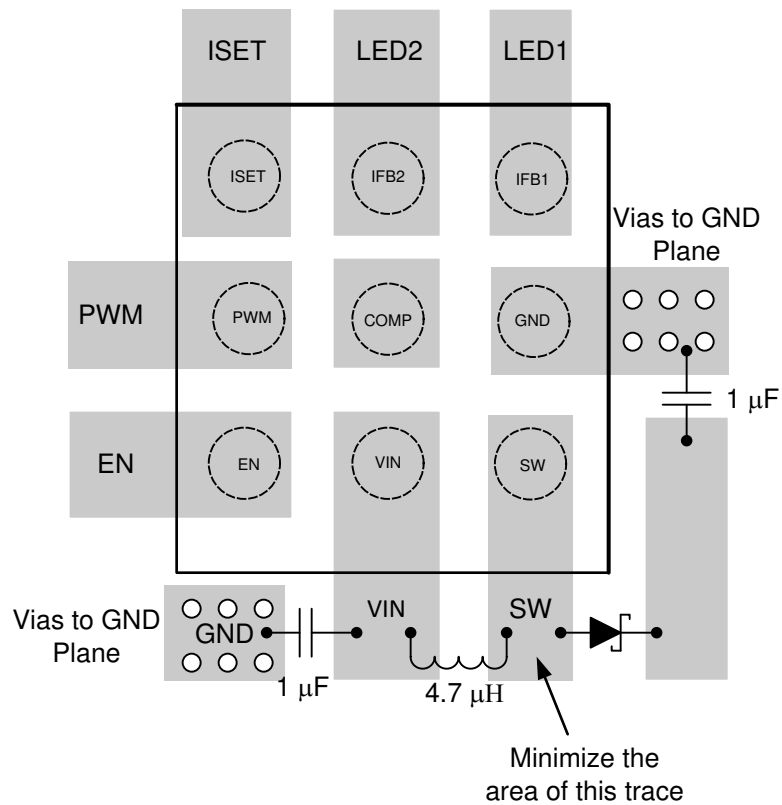


Figure 7-17. TPS61162A/TPS61163A Layout

8 Device and Documentation Support

8.1 Device Support

8.2 Related Links

Table 8-1 below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61162A	Click here	Click here	Click here	Click here	Click here
TPS61163A	Click here	Click here	Click here	Click here	Click here

8.3 Community Resources

8.4 Trademarks

EasyScale™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2015) to Revision B (May 2024) Page

- Updated *Device Information Table*..... 1

Changes from Revision * (November 2013) to Revision A (May 2015) Page

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; 1
- Deleted *Ordering Information* 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61162AYFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 125	TPS 61162A	Samples
TPS61163AYFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS 61163A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61162AYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS61163AYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61162AYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61163AYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0

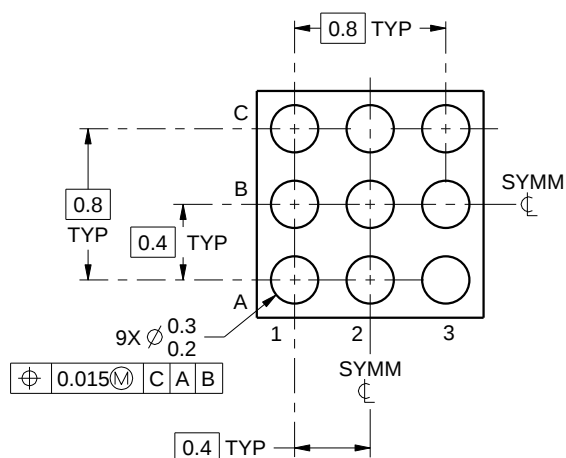
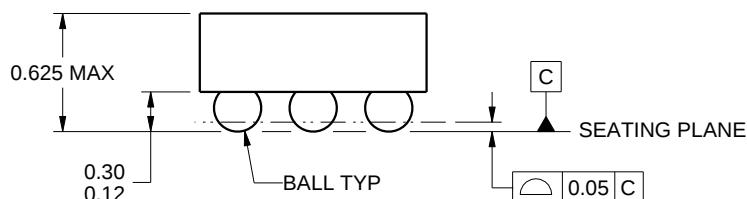
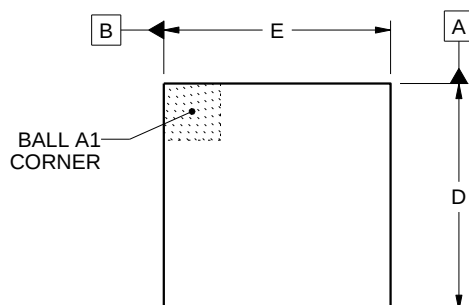
YFF0009



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.336 mm, Min =1.276 mm

E: Max = 1.336 mm, Min =1.276 mm

4219552/A 05/2016

NOTES:

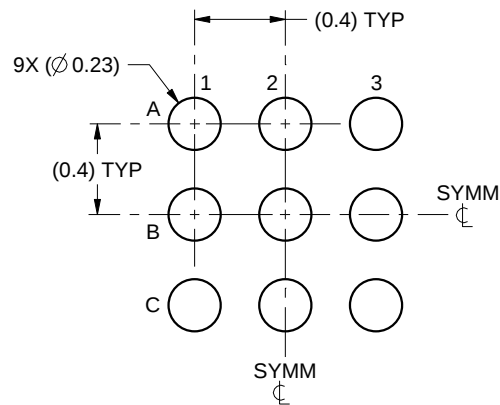
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

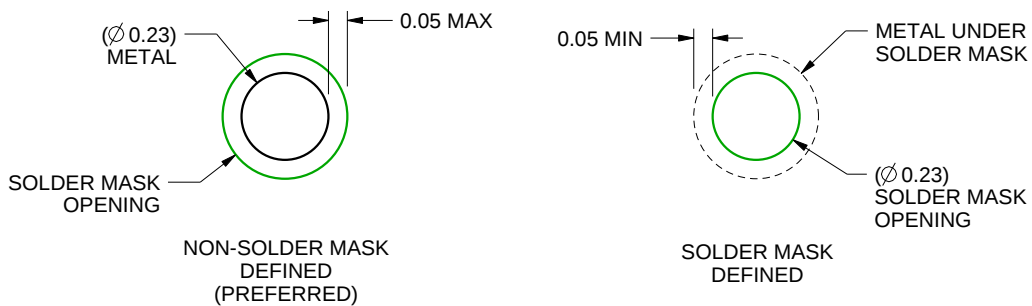
YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219552/A 05/2016

NOTES: (continued)

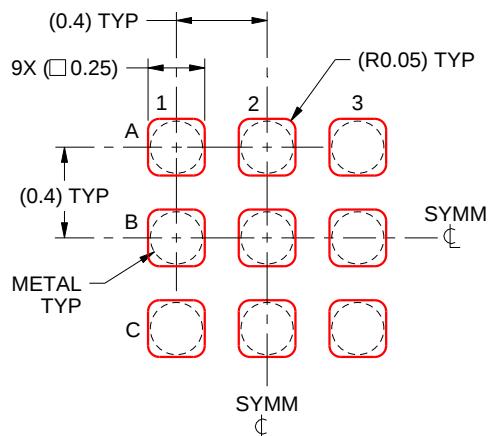
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219552/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated