SONY

CXG1050TN

Receiving Dual-Band Mixer

Description

The CXG1050TN is a receiving dual-band mixer MMIC. This IC is designed using the Sony's GaAs J-FET process.

Features

- High conversion gain Gc = 9.5dB (Typ.)
- Low noise figure NF = 4.9 to 5.2dB (Typ.)
- Low distortion Input IP3 = –0.5 to 0dBm (Typ.)
- Single 2.7V power supply operation
- Low LO input power operation PLO = –15dBm
- 16-pin TSSOP small package

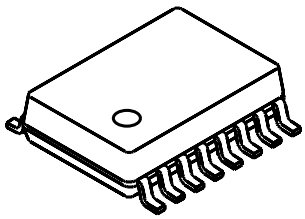
Applications

800MHz Japan digital cellular telephones (PDC)

Structure

GaAs J-FET MMIC

16 pin TSSOP (Plastic)



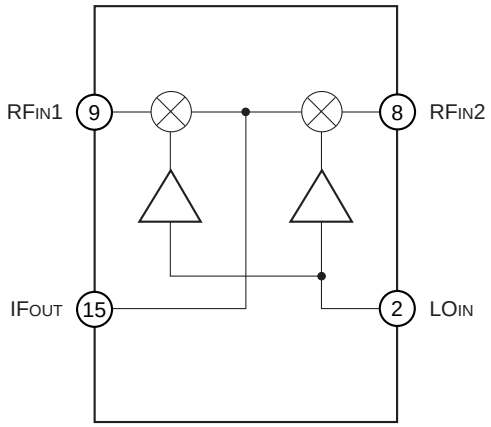
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	4.5	V
• Input power	P_{IN}	+5	dBm
• Current consumption	I_{DD} (Mixer block)	20	mA
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

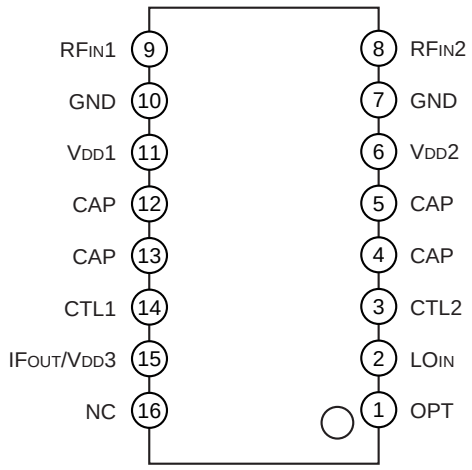
Recommended Operating Conditions

• Supply voltage	V_{DD}	2.7 to 3.3	V
• Control voltage	V_{CTL} (H)	2.4 to 3.3	V
	V_{CTL} (L)	0 to 0.3	V

Block Diagram



Pin Configuration



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E98432-PS

Electrical Characteristics

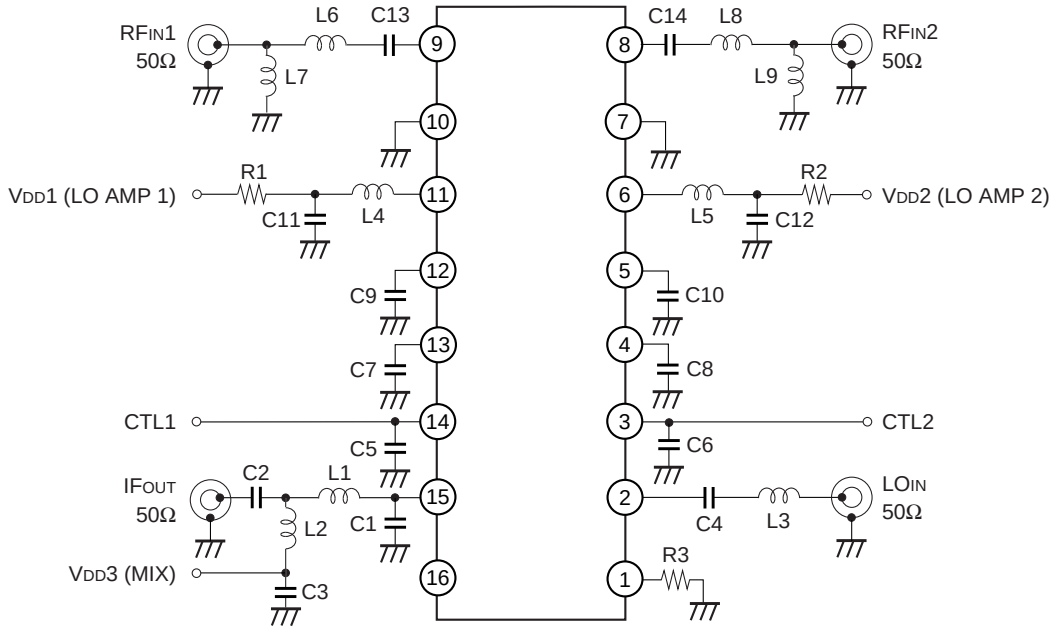
Conditions: V_{DD} = 2.7V, V_{CTL} (H) = 2.7V, V_{CTL} (L) = 0V, $f_{RF}1$ = 820MHz, $f_{RF}2$ = 870MHz, $f_{LO} = f_{RF} – 130MHz$, P_{LO} = –15dBm, unless otherwise specified

(Ta = 25°C)

Item	Symbol	Path	Control pin condition		Min.	Typ.	Max.	Unit	Measurement condition
			$V_{CTL}1$	$V_{CTL}2$					
Current consumption	I_{DD}	$V_{DD}1$, $V_{DD}2$ $V_{DD}3 \rightarrow$ GND	H	L	—	6.3	7.5	mA	When no signal
			L	H					
Control current	I_{CTL}	CTL1 → GND	H	L	—	18	35	µA	
		CTL2 → GND	L	H					
Conversion gain	G_C	$RF_{IN}1 \rightarrow IF_{OUT}$	H	L	7	9.5	12	dB	When a small signal
			L	H	—	–16	–12		
		$RF_{IN}2 \rightarrow IF_{OUT}$	H	L	—	–13	–9		
			L	H	7	9.5	12		
Noise figure	NF	$RF_{IN}1 \rightarrow IF_{OUT}$	H	L	—	4.9	6.5	dB	
		$RF_{IN}2 \rightarrow IF_{OUT}$	L	H	—	5.2	6.5		
Input IP3	IIP3	$RF_{IN}1 \rightarrow IF_{OUT}$	H	L	–2.5	0	—	dBm	PRF = –25dBm, offset = 100kHz Conversion by the IM3 suppression ratio for two-wave input
		$RF_{IN}2 \rightarrow IF_{OUT}$	L	H	–3	–0.5	—		
LO to RF leak level	P_{LK}	$LO_{IN} \rightarrow RF_{IN}1$	H	L	—	–37	–30	dBm	f_{LO} = 690MHz
		$LO_{IN} \rightarrow RF_{IN}2$	L	H	—	–37	–30		f_{LO} = 740MHz

Note) The values shown above are the specified values on the Sony's recommended evaluation board.

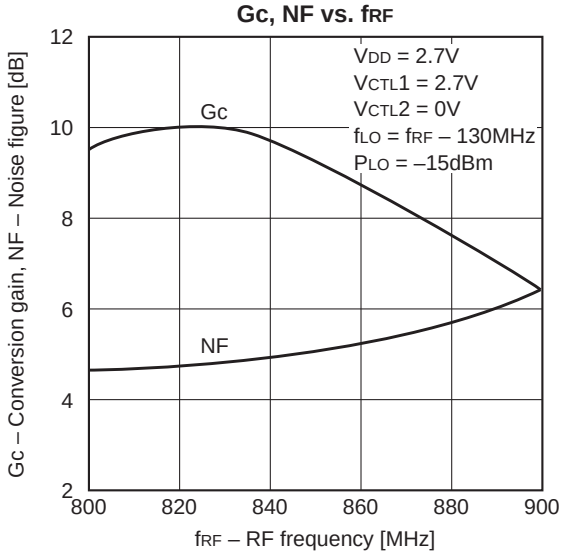
Recommended Evaluation Circuit



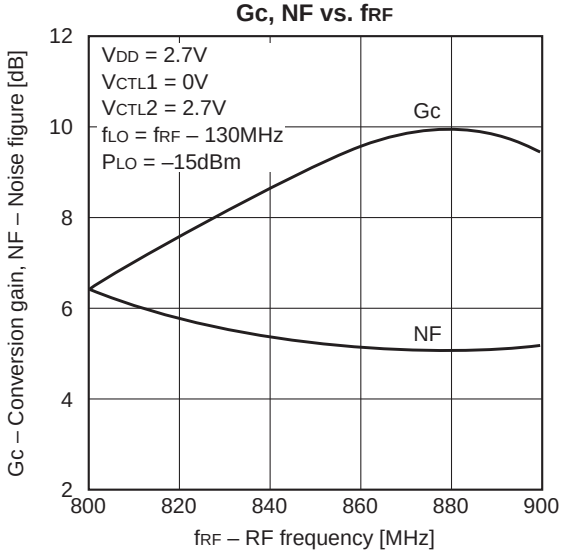
L1	82nH	C1	12pF	C10	100pF
L2	39nH	C2	1000pF	C11	100pF
L3	27nH	C3	1000pF	C12	100pF
L4	47nH	C4	100pF	C13	2pF
L5	39nH	C5	100pF	C14	2pF
L6	39nH	C6	100pF	R1	680Ω
L7	10nH	C7	1000pF	R2	680Ω
L8	33nH	C8	1000pF	R3	820Ω
L9	8.2nH	C9	100pF		

Example of Representative Characteristics (Ta = 25°C)

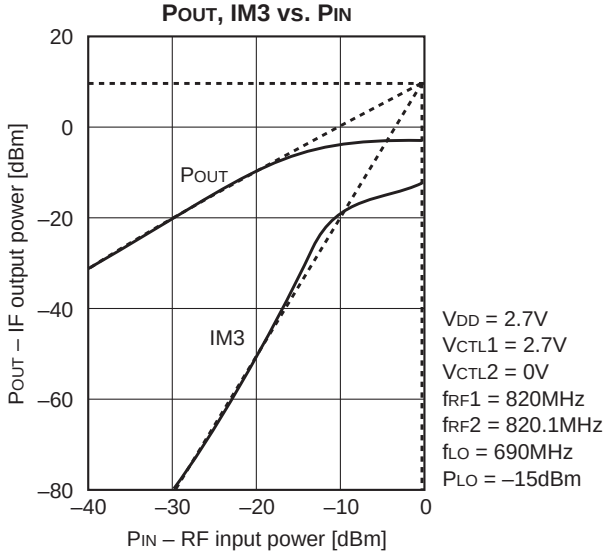
Path $RF_{IN}1 \rightarrow IF_{OUT}$
Gc, NF vs. f_{RF}



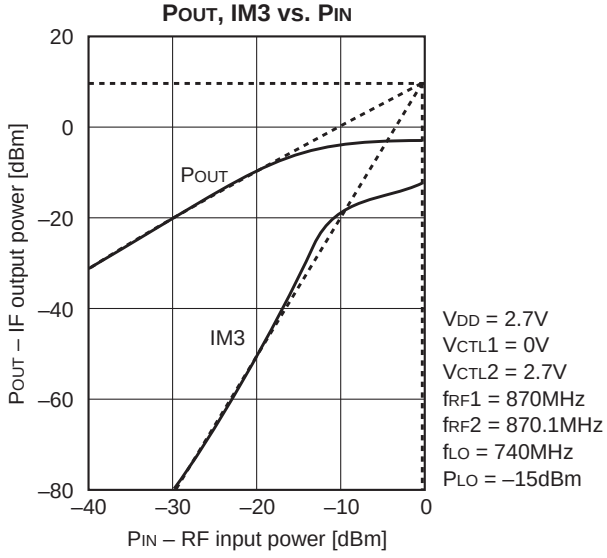
Path $RF_{IN}2 \rightarrow IF_{OUT}$
Gc, NF vs. f_{RF}



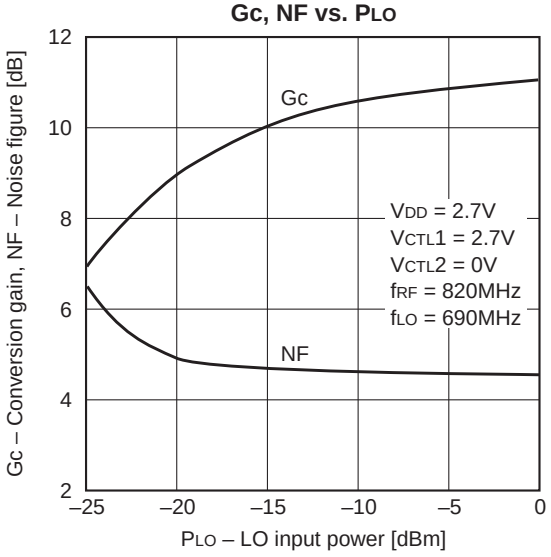
Path $RF_{IN}1 \rightarrow IF_{OUT}$
P_{OUT}, IM3 vs. P_{IN}



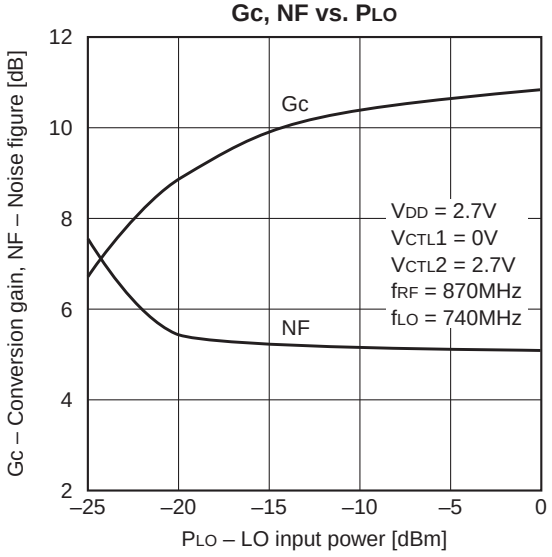
Path $RF_{IN}2 \rightarrow IF_{OUT}$
P_{OUT}, IM3 vs. P_{IN}



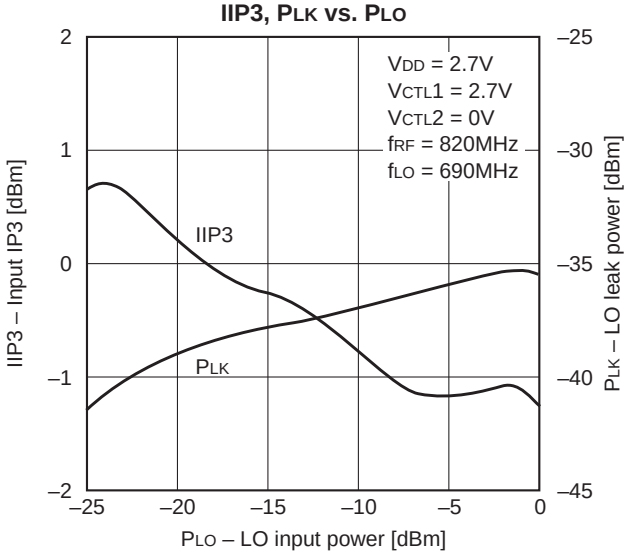
Path $RF_{IN}1 \rightarrow IF_{OUT}$
Gc, NF vs. P_{LO}



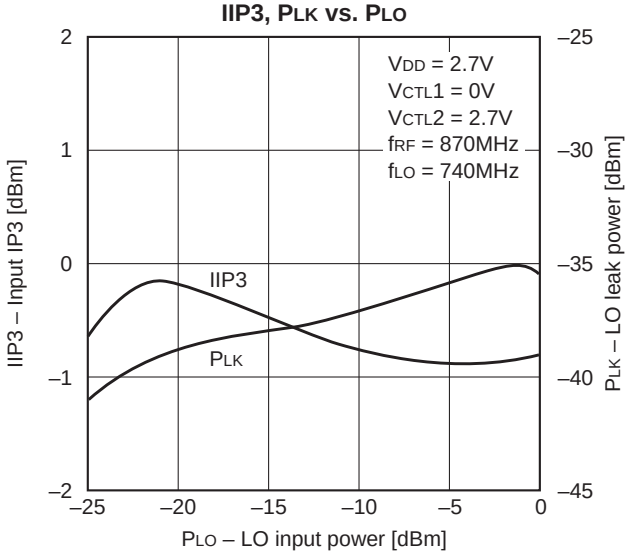
Path $RF_{IN}2 \rightarrow IF_{OUT}$
Gc, NF vs. P_{LO}



Path $RF_{IN}1 \rightarrow IF_{OUT}$
IIP3, P_{LK} vs. P_{LO}

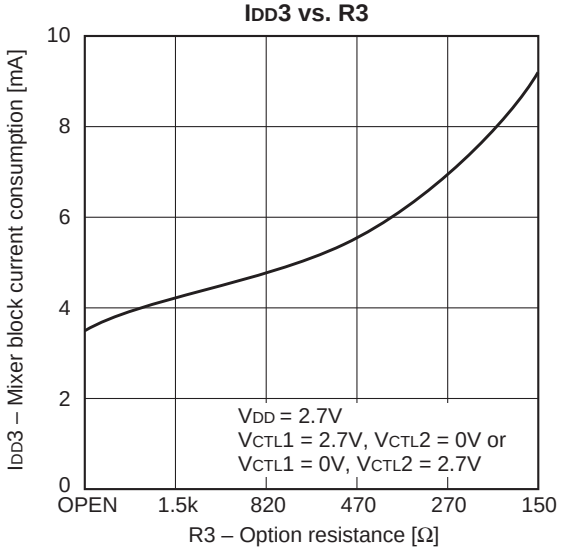


Path $RF_{IN}2 \rightarrow IF_{OUT}$
IIP3, P_{LK} vs. P_{LO}

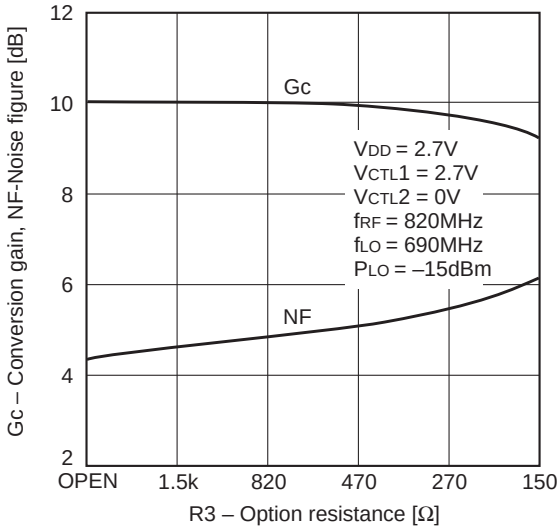


Example of Characteristics for Option Resistance R3 Changed (Ta = 25°C)

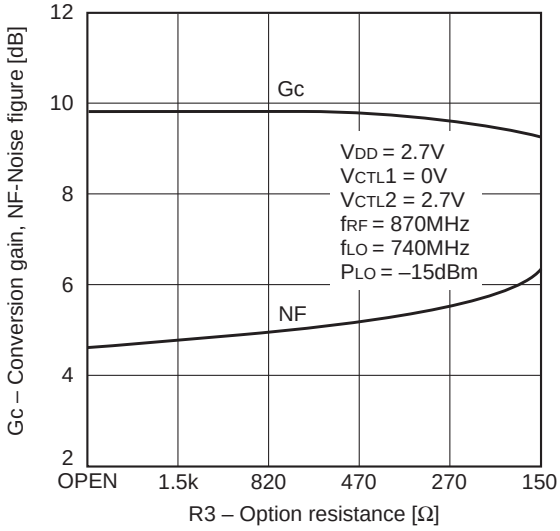
IDD3 vs. R3



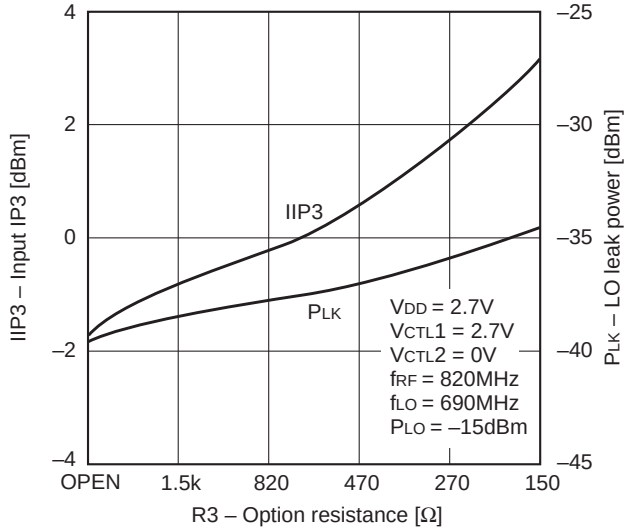
Path RFIN1 → IFOUT
Gc, NF vs. R3



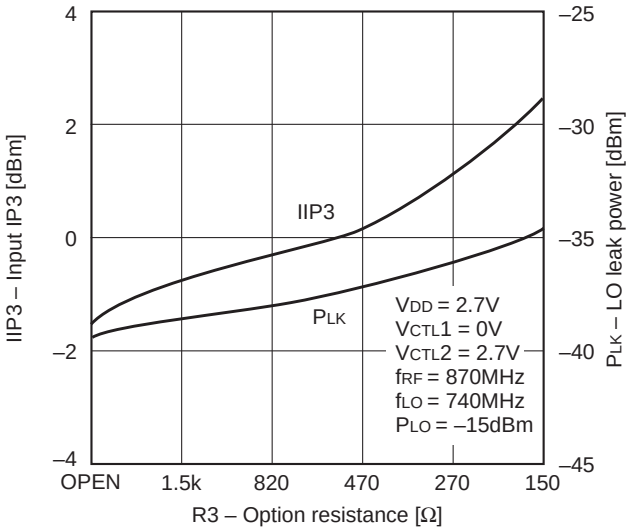
Path RFIN2 → IFOUT
Gc, NF vs. R3



Path RFIN1 → IFOUT
IIP3, PLK vs. R3

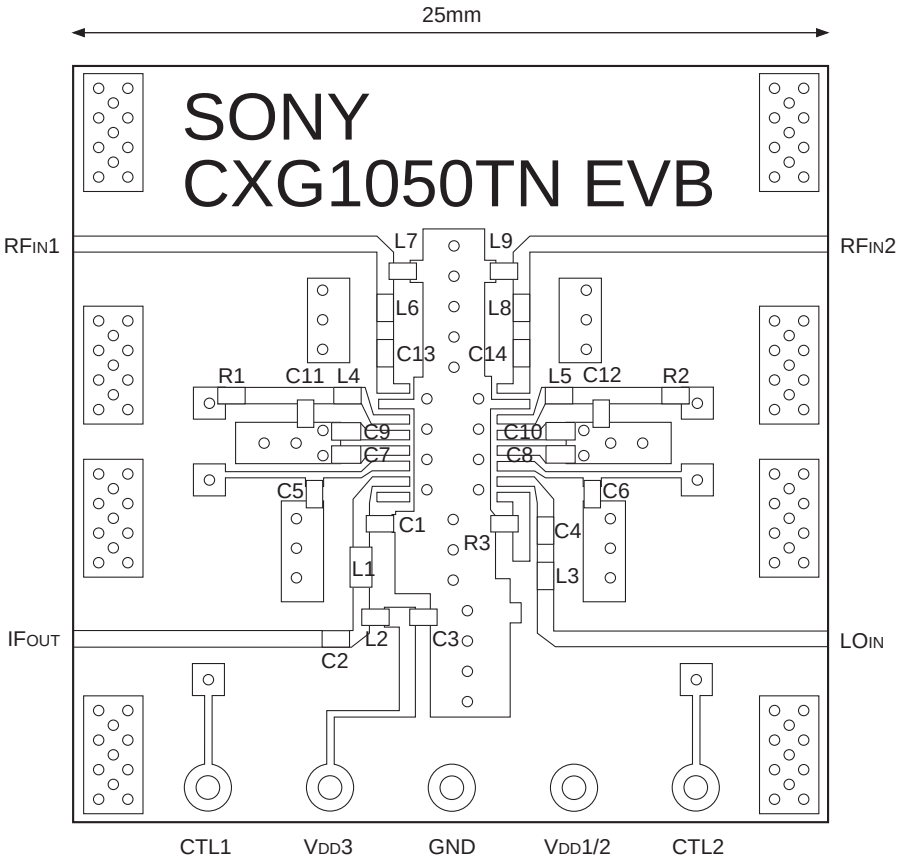


Path RFIN2 → IFOUT
IIP3, PLK vs. R3

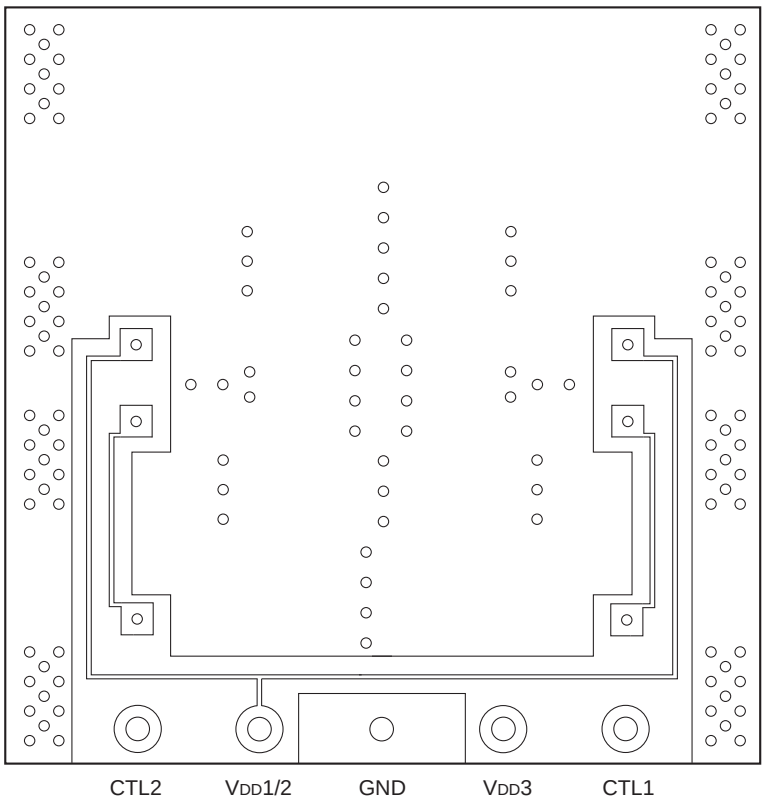


Recommended Evaluation Board

Front



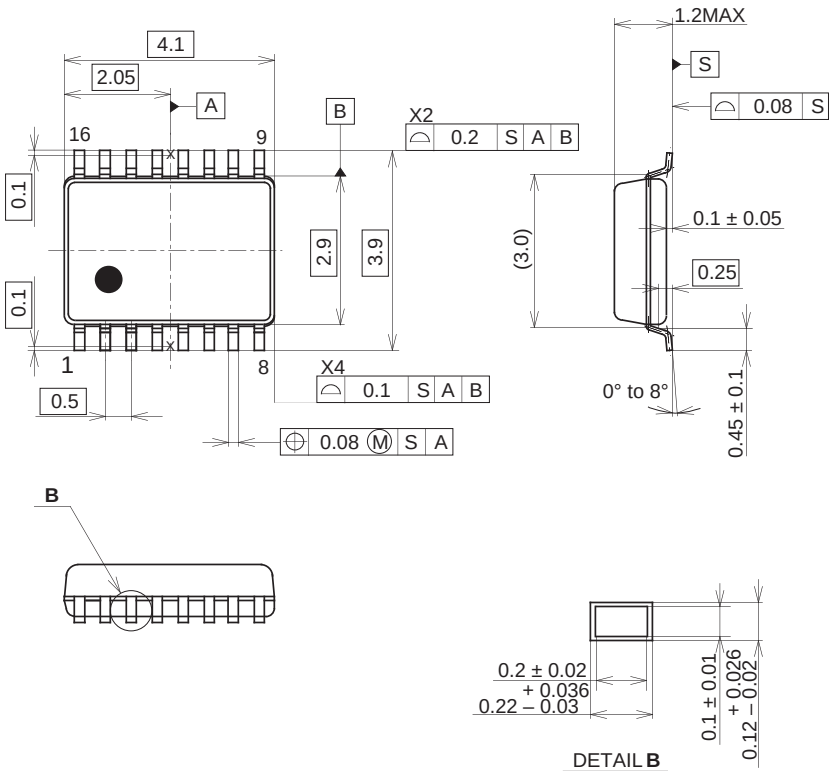
Back



Glass fabric-base 4-layer epoxy board (thickness: 0.3mm × 2)
GND for the 2nd and 3rd layers

Package Outline Unit: mm

16PIN TSSOP(PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g

SONY CODE	TSSOP-16P-L01
EIAJ CODE	————
JEDEC CODE	————