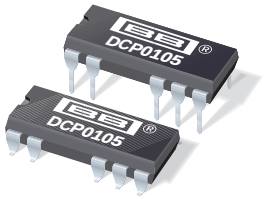
BURR - BROWN®



DCP0105 Series

Miniature 5V Input, 1W Isolated UNREGULATED DC/DC CONVERTERS

FEATURES

- STANDARD JEDEC PLASTIC PACKAGE
- MEETS EN55022 CLASS B
- LOW PROFILE: 0.15" (3.8mm)
- SYNCHRONIZABLE
- OUTPUT SHORT CIRCUIT PROTECTION
- THERMAL SHUTDOWN
- STARTS INTO ANY CAPACITIVE LOAD
- FLOATING OUTPUTS
- EFFICIENCY: Up to 75% (at Full Load)
- 1000Vrms ISOLATION
- 400kHz SWITCHING
- 108 MILLION HOURS MTTF
- 5V, ±5V, 12V, ±12V, 15V, ±15V OUTPUTS
- AVAILABLE IN TAPE AND REEL

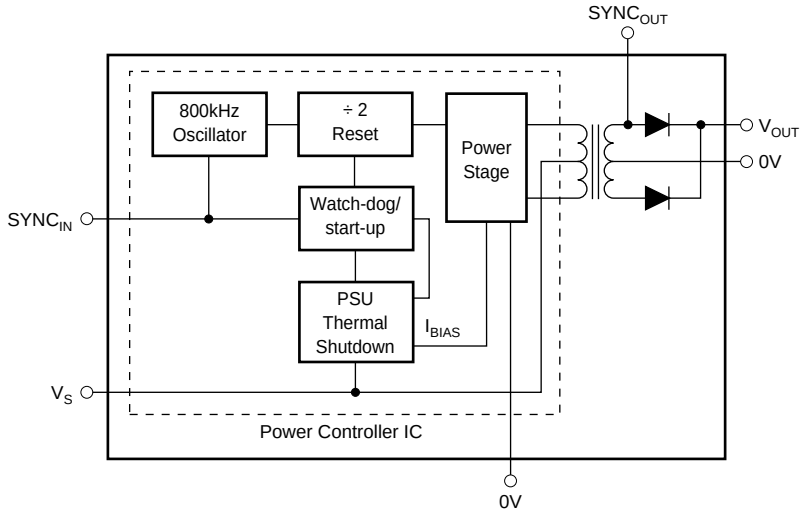
DESCRIPTION

The DCP0105 family is a series of high efficiency, 5V input isolated DC/DC converters. In addition to 1W nominal galvanically isolated output power capability, the range of DC/DCs are also fully synchronizable. The devices feature thermal shutdown, and overload protection is implemented via watchdog circuitry. Advanced power-on reset techniques give superior reset performance and the devices will start into any capacitive load up to full power output.

The DCP0105 family is implemented in standard-molded IC packaging, giving outlines suitable for high volume assembly.

APPLICATIONS

- POINT OF USE POWER CONVERSION
- DIGITAL INTERFACE POWER
- GROUND LOOP ELIMINATION
- DATA ACQUISITION
- INDUSTRIAL CONTROL AND INSTRUMENTATION
- TEST EQUIPMENT



ternational Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

At T_A = +25°C, V_S = +5V, unless otherwise specified.

PARAMETER	CONDITIONS	DCP0105 SERIES MIN	DCP0105 SERIES TYP	DCP0105 SERIES MAX	UNITS
OUTPUT					
Power	V_S + 4%		1		W
	100% Full Load		0.92		W
Voltage (V_{NOM})					
DCP010505	75% Full Load[1]	4.6	5	5.1	V
DCP010505D	75% Full Load	±4.6	±5	±5.1	V
DCP010512	75% Full Load	11.2	12	12.4	V
DCP010512D	75% Full Load	±11.2	±12	±12.4	V
DCP010515	75% Full Load	14.0	15	15.5	V
DCP010515D	75% Full Load	±14.0	±15	±15.5	V
Voltage vs Temperature			±0.08		%/°C
Short-Circuit Duration	V_S ± 10%	Indefinite			
Ripple	C_L = O/P Capacitor = 10µF		20		mVp-p
INPUT					
Nominal Voltage (V_S)			5		V
Voltage Range		–10		10	%
Supply Current	100% Full Load		250		mA
Reflected Ripple Current	C_{IN} = I/P Capacitor = 1µF		20		mArms
	50% Full Load				
ISOLATION					
Voltage[2]	1s Flash Test	1			kVrms
Continuous Voltage[3]			1		kVrms
Insulation Resistance			>1		GΩ
Input/Output Capacitance			2.5		pF
LOAD REGULATION					
DCP010505	10% to 100% Load		25	31	%
	10% to 75% Load		17		%
	75% to 100% Load		–8		%
DCP010505D	10% to 100% Load		25	32	%
	10% to 75% Load		19		%
	75% to 100% Load		–8		%
DCP010512	10% to 100% Load		17	38	%
	10% to 25% Load		7		%
	25% to 75% Load		12		%
	75% to 100% Load		–7		%
DCP010512D	10% to 100% Load		20	37	%
	10% to 25% Load		7		%
	25% to 75% Load		12		%
	75% to 100% Load		–7		%
DCP010515	10% to 100% Load		20	42	%
	10% to 25% Load		11		%
	25% to 75% Load		12		%
	75% to 100% Load		–7		%
DCP010515D	10% to 100% Load		16	41	%
	10% to 25% Load		11		%
	25% to 75% Load		12		%
	75% to 100% Load		–7		%
SWITCHING/SYNCHRONIZATION					
Oscillator Frequency (F_{OSC})	Switching Frequency = F_{OSC}/2		800		kHz
Sync Input Low		0		0.8	V
Sync Input Current	V_{SYNC} = +2V		48		µA
Reset Time			3.8		µs
$SYNC_{OUT}$ Frequency			400		kHz
GENERAL					
No Load Current					
DCP010505P	0% Full Load		38		mA
DCP010505DP	0% Full Load		40		mA
DCP010512P	0% Full Load		30		mA
DCP010512DP	0% Full Load		33		mA
DCP010515P	0% Full Load		34		mA
DCP010515DP	0% Full Load		34		mA

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = +5V, unless otherwise specified.

PARAMETER	CONDITIONS	DCP0105 SERIES MIN	DCP0105 SERIES TYP	DCP0105 SERIES MAX	UNITS
GENERAL (Cont)					
Efficiency					
DCP010505	100% Full Load		71		%
	10% Full Load		40		%
DCP010505D	100% Full Load		66		%
	10% Full Load		47		%
DCP010512	100% Full Load		72		%
	10% Full Load		38		%
DCP010512D	100% Full Load		72		%
	10% Full Load		36		%
DCP010515	100% Full Load		73		%
	10% Full Load		40		%
DCP010515D	100% Full Load		75		%
	10% Full Load		38		%
MTTF(3)	T_A = +85°C	158,000			hrs
	T_A = +55°C	3,050,000			hrs
	T_A = +25°C	108,000,000			hrs
Weight	14-Pin PDIP		1.08		g
THERMAL SHUTDOWN					
Internal Controller IC Temperature		115		140	°C
Shutdown Current			3		mA
TEMPERATURE RANGE					
Operating		–40		+100	°C

NOTES: (1) 100% load current = 1W/V_{NOM} typical. (2) Rated working voltage = 130Vrms (IEC950 Convention). (3) Life test data.

EMC SPECIFICATIONS

Specifications and Related Documents

The DCP010505 was tested to and complied with the limits of the following EMC specifications:

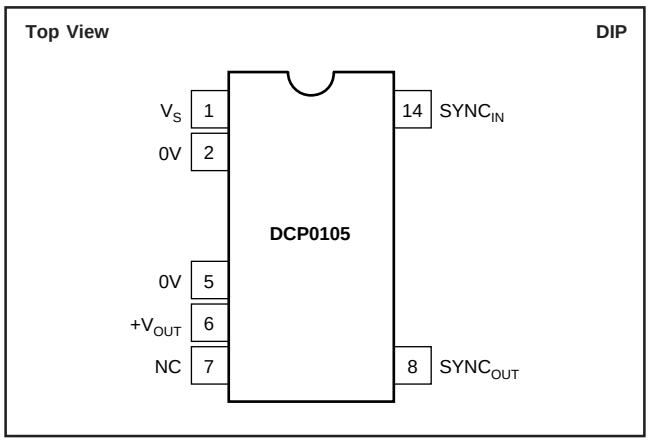
prEN55022 (1992)	Conducted RF emission, telecomm lines.
EN55022 (1995)	Limits and methods of measurement of radio interference characteristics of information technology equipment.
ENV50140 (1993)	Electromagnetic compatibility. Basic immunity standard. Radiated RF immunity.
ENV50141 (1993)	Electromagnetic compatibility. Basic immunity standard. Conducted RF immunity.
EN61000-4-2 (1995)	Electromagnetic compatibility, Part 4. Testing and measurement techniques, Section 2. Electrostatic discharge.
EN61000-4-4 (1995)	Electromagnetic compatibility, Part 4. Testing and measurement techniques, Section 4. Electrical fast transient bursts.
EN61000-4-8 (1994)	Electromagnetic compatibility, Part 4. Testing and measurement techniques, Section 8. Power frequency magnetic field immunity.

List of Tests

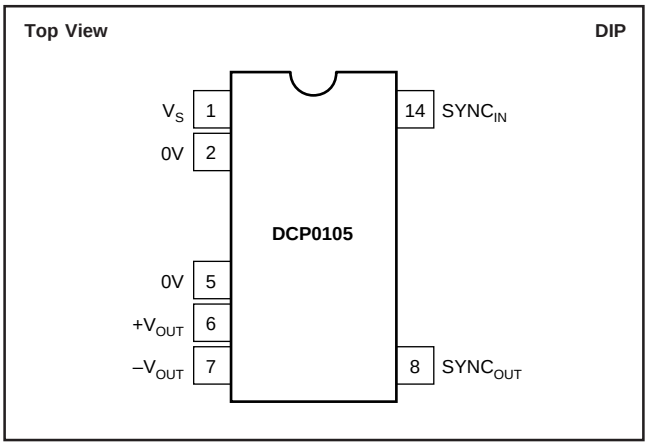
The following is a list of tests which were required for compliance with the above specifications:

Conducted Emission Test	150kHz to 30MHz, power and output lines, Class B limits applying. DC/DC loads of 0%, 8%, and 120% applying.
Radiated Emission Test	30MHz to 1000MHz, Class B limits applying. DC/DC loads of 0%, 8%, and 120% applying.
Radiated Immunity Test, Electric Field	80MHz to 1000MHz, 10V/m, 1kHz 80% AM.
Radiated Immunity Test, Electric Field	900MHz, 10V/m, 200Hz 100% PM.
Electrostatic Discharge Test	4kV, HCP/VCP indirect discharge only.
Electrical Fast Transient Tests	2kV power lines, 2kV signal lines.
Conducted RF Immunity Tests	150kHz to 80MHz, power and output lines, 10Vrms, 1kHz 80% AM.
Radiated Immunity Test, Magnetic Field	50Hz, 30A/m

PIN CONFIGURATION (Single)



PIN CONFIGURATION (Dual)



PIN DEFINITIONS (Single)

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input.
2	0V	Input Side Common.
5	0V	Output Side Common.
6	$+V_{OUT}$	+Voltage Out.
7	NC	Not Connected.
8	$SYNC_{OUT}$	Unregulated 400kHz Output from Transformer.
14	$SYNC_{IN}$	Synchronization Pin.

PIN DEFINITIONS (Dual)

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input.
2	0V	Input Side Common.
5	0V	Output Side Common.
6	$+V_{OUT}$	+Voltage Out.
7	$–V_{OUT}$	–Voltage Out.
8	$SYNC_{OUT}$	Unregulated 400kHz Output from Transformer.
14	$SYNC_{IN}$	Synchronization Pin.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	7V
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

ORDERING INFORMATION

DCP01 05 05 (D) ( )

- Basic Model Number: 1W Product
- Voltage Input: 5V In
- Voltage Output: 5V Out
- Dual Output:
- Package Code: P = 14-Pin Plastic DIP; P-U = 14-Pin Plastic DIP Gull Wing



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

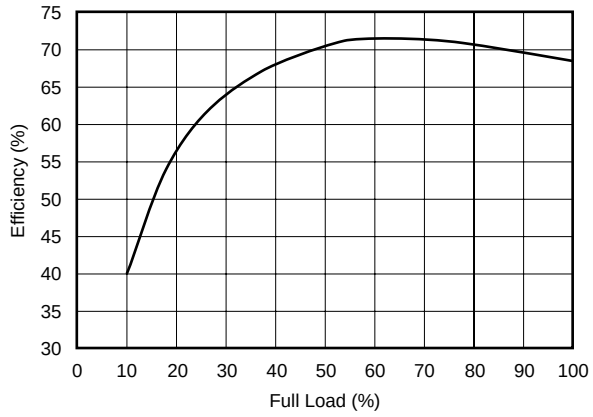
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA
Single						
DCP010505	14-Pin PDIP	010-1	–40°C to +100°C	DCP010505P	DCP010505P	Rails
DCP010505	14-Pin PDIP Gull Wing	010-2	–40°C to +100°C	DCP010505P-U	DCP010505P-U	Rails
"	"	"	"	"	DCP010505P-U/700	Tape and Reel
DCP010512	14-Pin PDIP	010-1	–40°C to +100°C	DCP010512P	DCP010505P	Rails
DCP010512	14-Pin PDIP Gull Wing	010-2	–40°C to +100°C	DCP010512P-U	DCP010505P-U	Rails
"	"	"	"	"	DCP010505P-U/700	Tape and Reel
DCP010515	14-Pin PDIP	010-1	–40°C to +100°C	DCP010515P	DCP010505P	Rails
DCP010515	14-Pin PDIP Gull Wing	010-2	–40°C to +100°C	DCP010515P-U	DCP010505P-U	Rails
"	"	"	"	"	DCP010505P-U/700	Tape and Reel
Dual						
DCP010505D	14-Pin PDIP	010-1	–40°C to +100°C	DCP010505DP	DCP010505DP	Rails
DCP010505D	14-Pin PDIP Gull Wing	010-2	–40°C to +100°C	DCP010505DP-U	DCP010505DP-U	Rails
"	"	"	"	"	DCP010505DP-U/700	Tape and Reel
DCP010512D	14-Pin PDIP	010-1	–40°C to +100°C	DCP010512DP	DCP010512DP	Rails
DCP010512D	14-Pin PDIP Gull Wing	010-2	–40°C to +100°C	DCP010512DP-U	DCP010512DP-U	Rails
"	"	"	"	"	DCP010512DP-U/700	Tape and Reel
DCP010515D	14-Pin PDIP	010-1	–40°C to +100°C	DCP010515DP	DCP010515DP	Rails
DCP010515D	14-Pin PDIP Gull Wing	010-2	–40°C to +100°C	DCP010515DP-U	DCP010515DP-U	Rails
"	"	"	"	"	DCP010515DP-U/700	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /700 indicates 700 devices per reel). Ordering 700 pieces of DCP010505P-U/700 will get a single 700-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

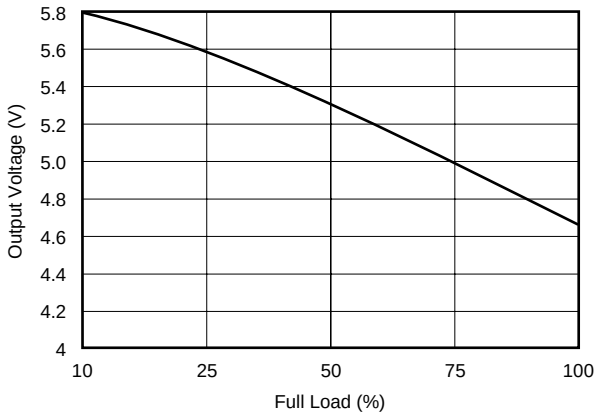
TYPICAL PERFORMANCE CURVES (Common and DCP010505 Specific)

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = +5V and V_S = +5V, unless otherwise noted.

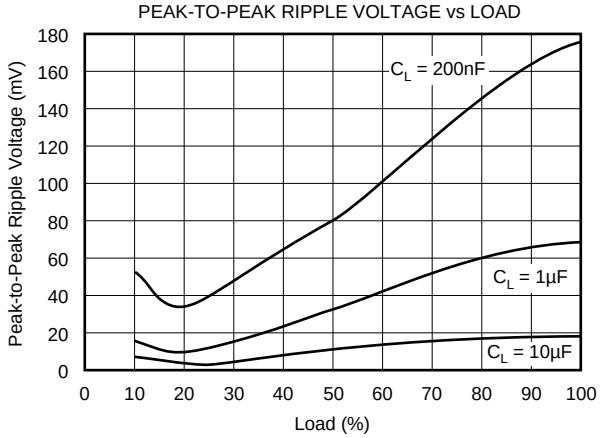
DCP010505 EFFICIENCY vs LOAD



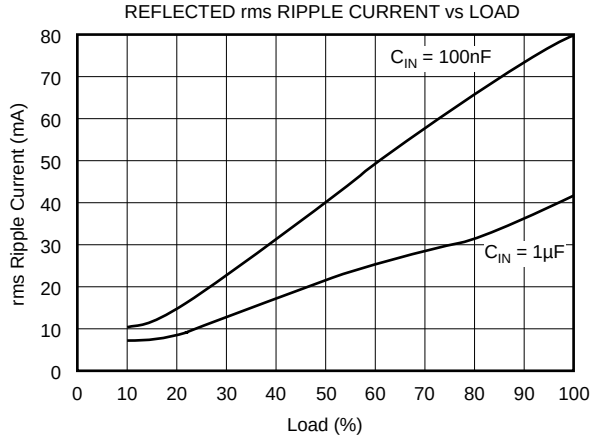
DCP010505 OUTPUT VOLTAGE vs LOAD



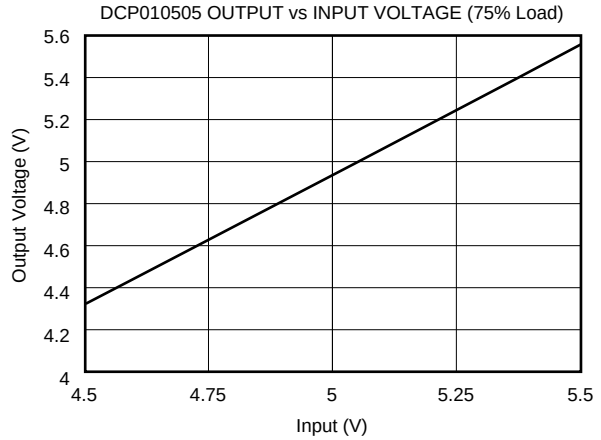
PEAK-TO-PEAK RIPPLE VOLTAGE vs LOAD



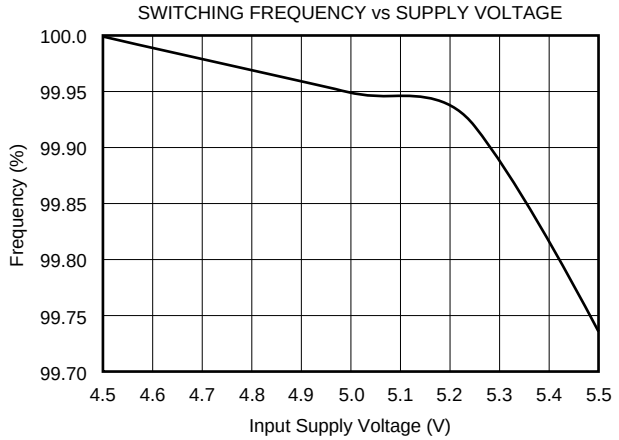
REFLECTED rms RIPPLE CURRENT vs LOAD



DCP010505 OUTPUT vs INPUT VOLTAGE (75% Load)



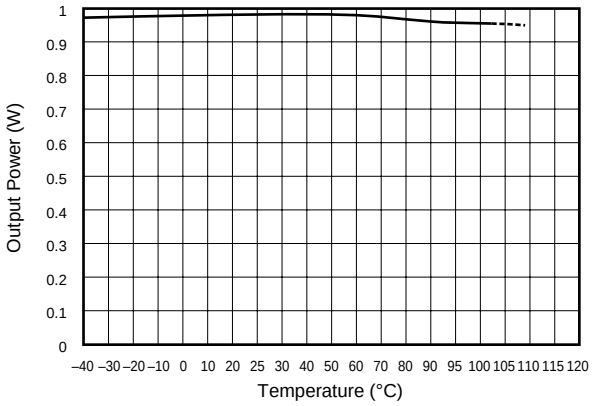
SWITCHING FREQUENCY vs SUPPLY VOLTAGE



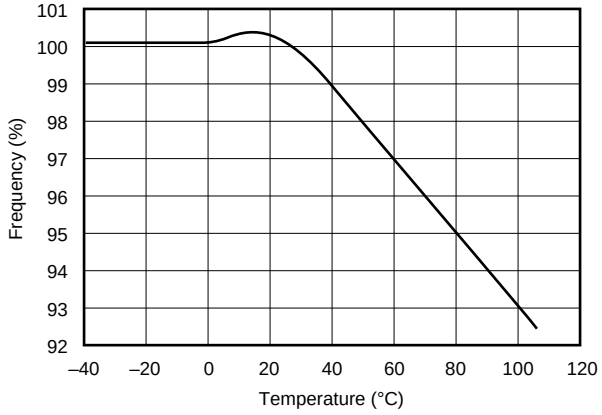
TYPICAL PERFORMANCE CURVES (Common and DCP010505 Specific, cont)

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = +5V and V_S = +5V, unless otherwise noted.

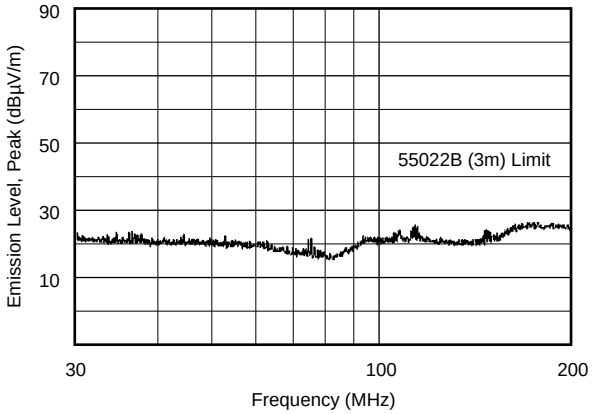
DCP010505 OUTPUT POWER vs TEMPERATURE



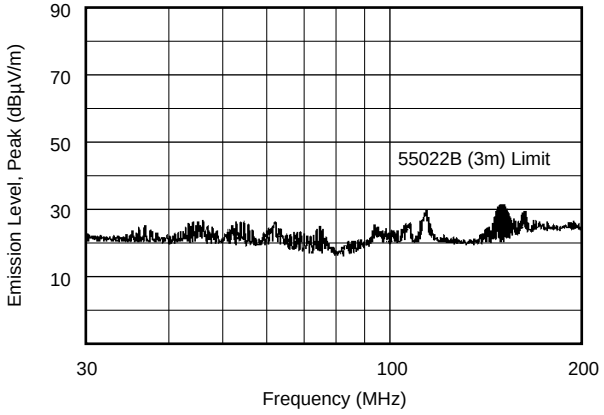
SWITCHING FREQUENCY vs TEMPERATURE



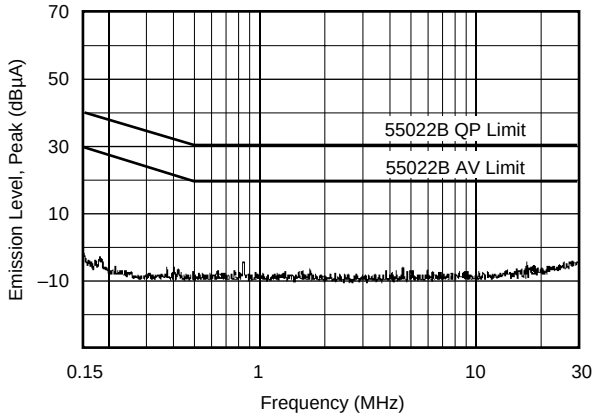
RADIATED EMISSIONS (8% Load)



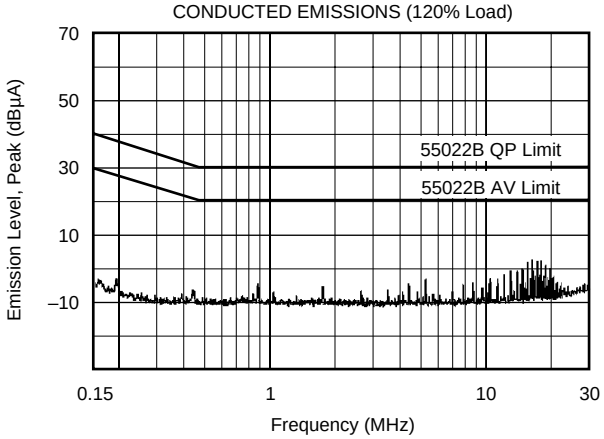
RADIATED EMISSIONS (120% Load)



CONDUCTED EMISSIONS (8% Load)



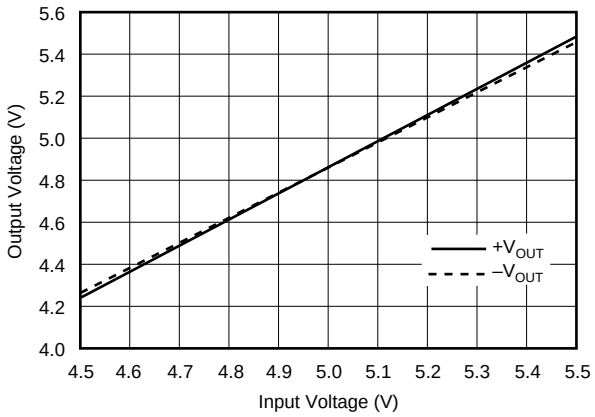
CONDUCTED EMISSIONS (120% Load)



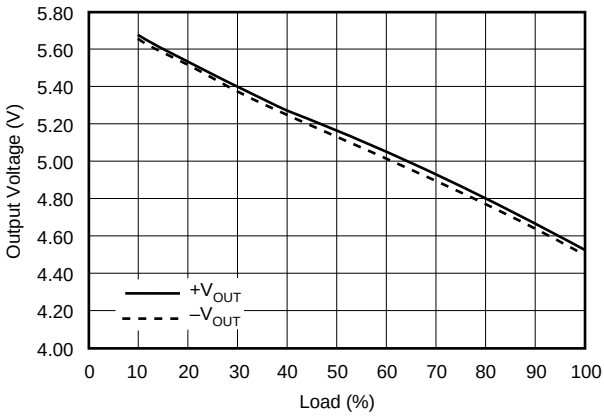
TYPICAL PERFORMANCE CURVES (DCP010505D Specific)

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = ±5V and V_S = +5V, unless otherwise noted.

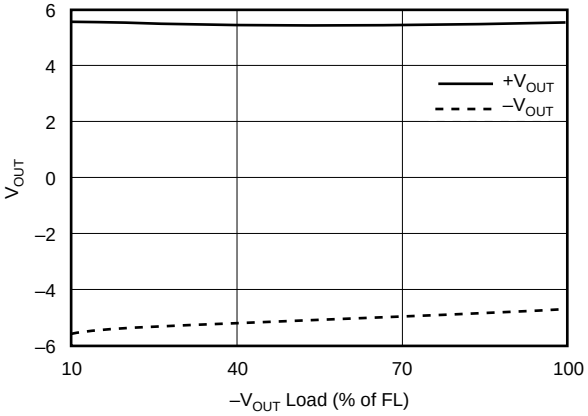
DCP010505D OUTPUT vs INPUT VOLTAGE (75% Load)



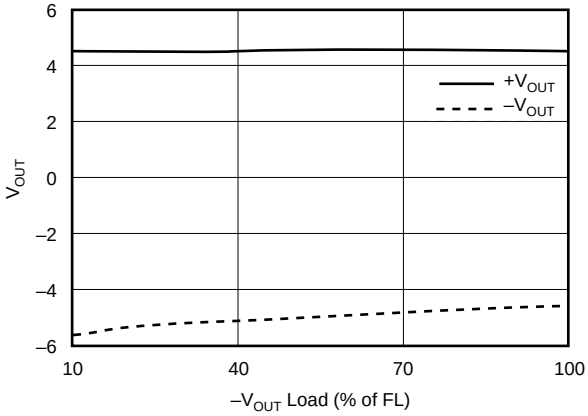
DCP010505D OUTPUT VOLTAGE vs LOAD



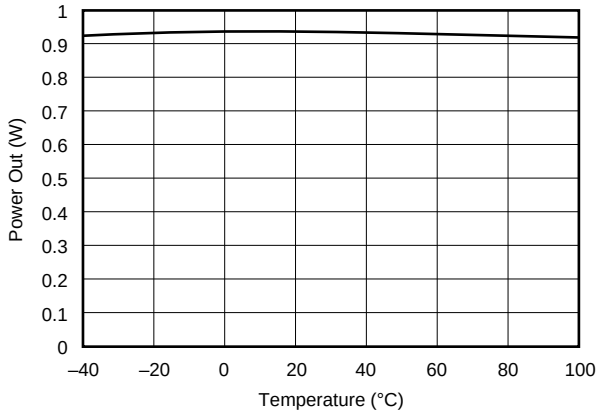
DCP010505D LOAD BALANCE (+V_{OUT} Load = 10%)



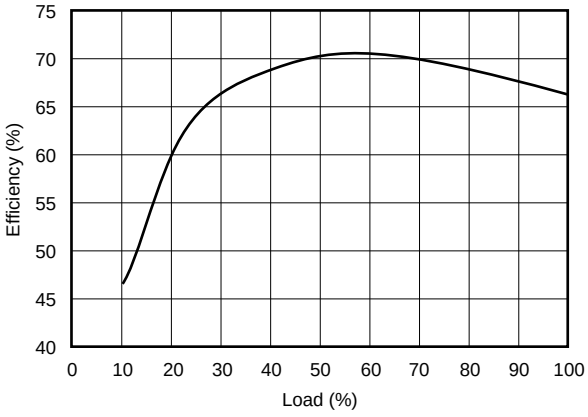
DCP010505D LOAD BALANCE (+V_{OUT} Load = 100%)



DCP010505D POWER vs TEMPERATURE



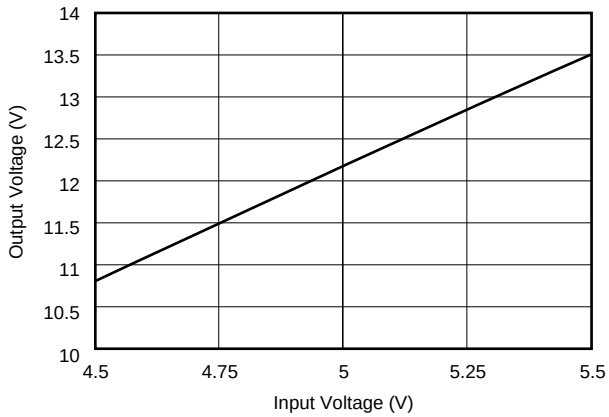
DCP010505D EFFICIENCY vs LOAD



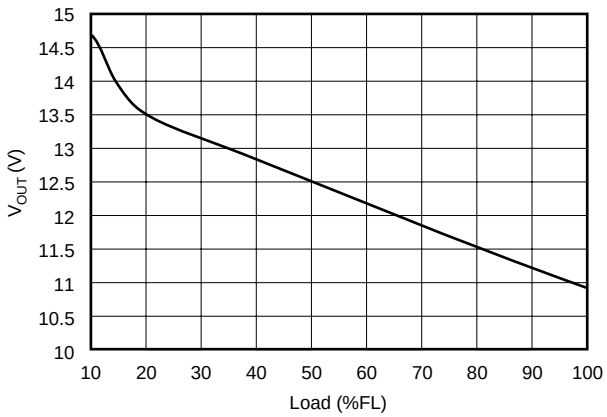
TYPICAL PERFORMANCE CURVES (DCP010512 Specific)

At T_A = +25°C, V_{OUT} nominal (V_{NOM}) = +12V and V_S = +5V, unless otherwise noted.

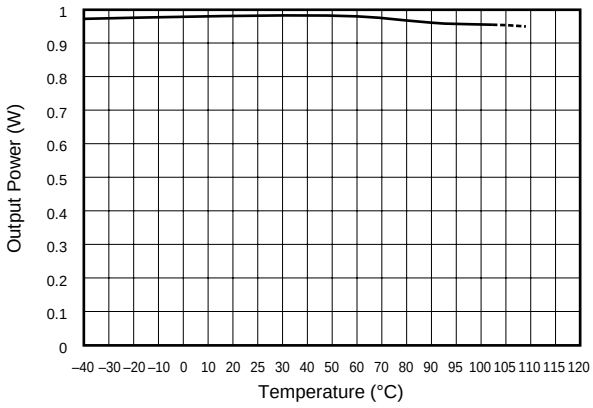
DCP010512 OUTPUT vs INPUT VOLTAGE (75% Load)



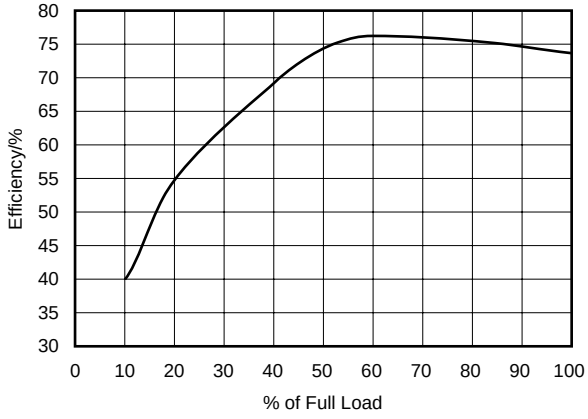
DCP010512 OUTPUT VOLTAGE vs LOAD



DCP010512 OUTPUT POWER vs TEMPERATURE



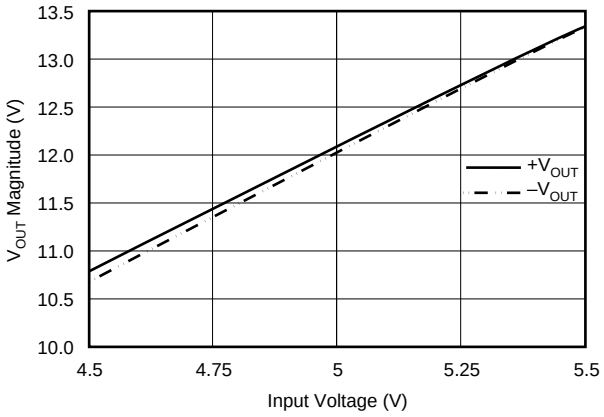
DCP010512 EFFICIENCY vs LOAD



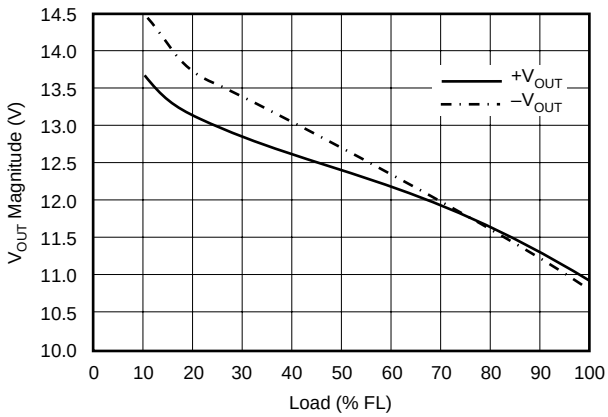
TYPICAL PERFORMANCE CURVES (DCP010512D Specific)

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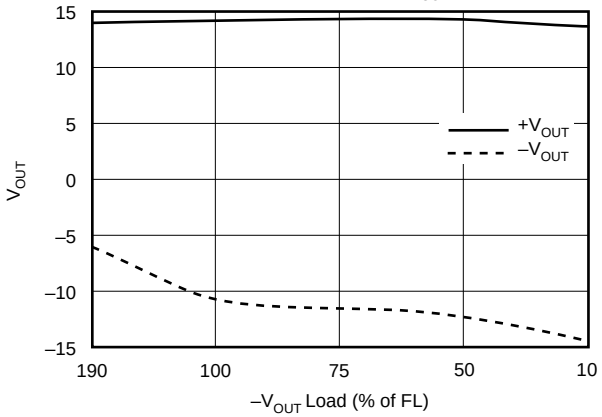
DCP010512D OUTPUT vs INPUT VOLTAGE (75% Load)



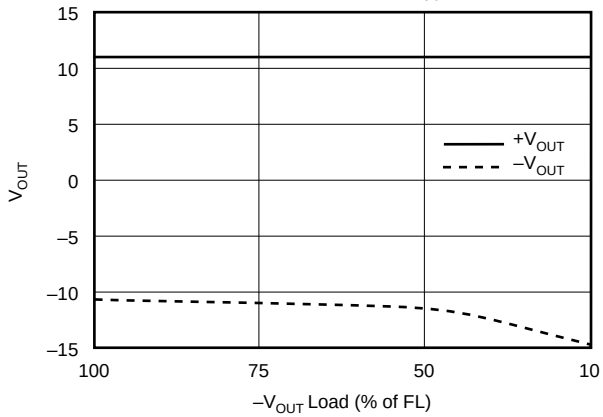
DCP010512D OUTPUT VOLTAGE vs LOAD



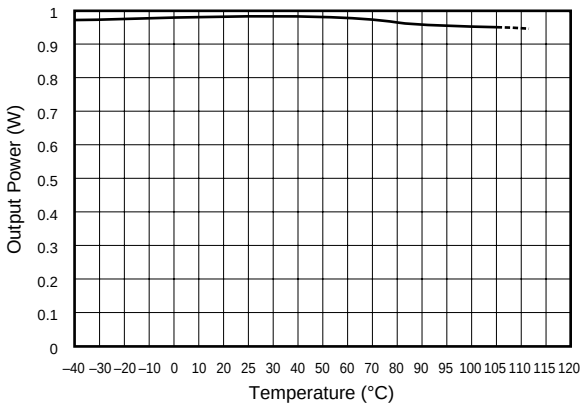
DCP010512D LOAD BALANCE (+V_{OUT} Load = 10%)



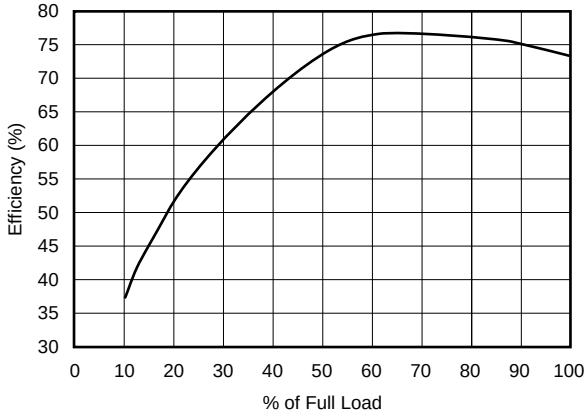
DCP0101512D LOAD BALANCE (+V_{OUT} Load = 100%)



DCP010512D OUTPUT POWER vs TEMPERATURE



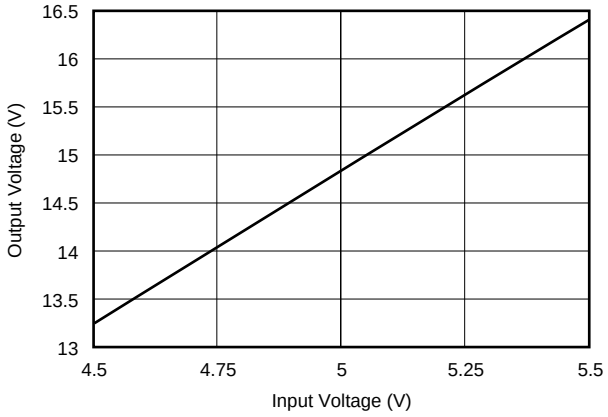
DCP010512D EFFICIENCY vs LOAD



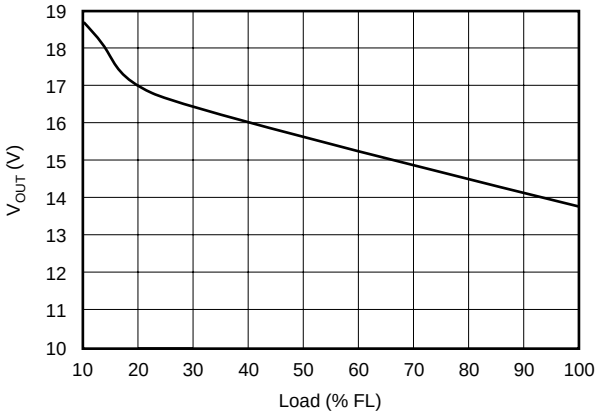
TYPICAL PERFORMANCE CURVES (DCP010515 Specific)

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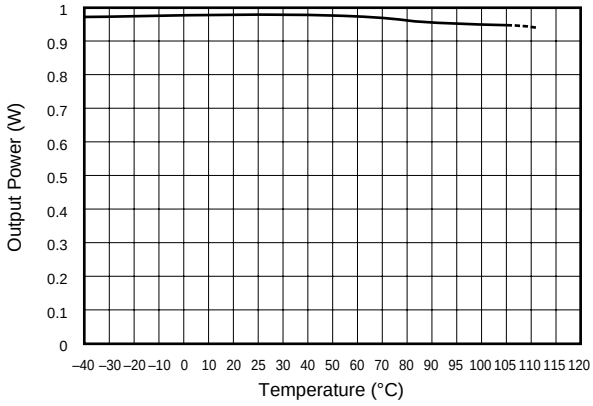
DCP010515 OUTPUT vs INPUT VOLTAGE (75% Load)



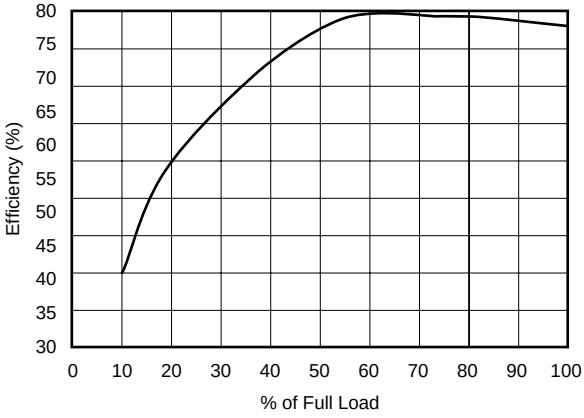
DCP010515 OUTPUT VOLTAGE vs LOAD



DCP010515 OUTPUT POWER vs TEMPERATURE



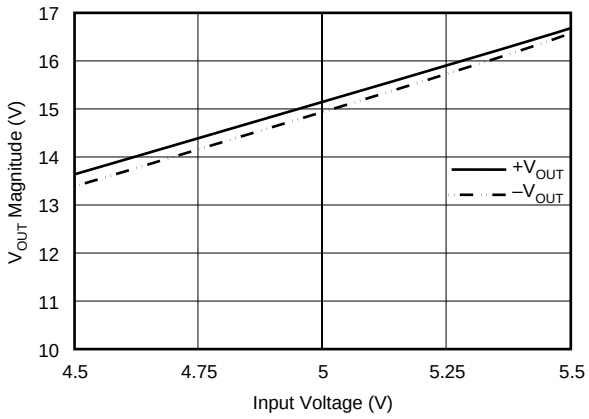
DCP010515 EFFICIENCY vs LOAD



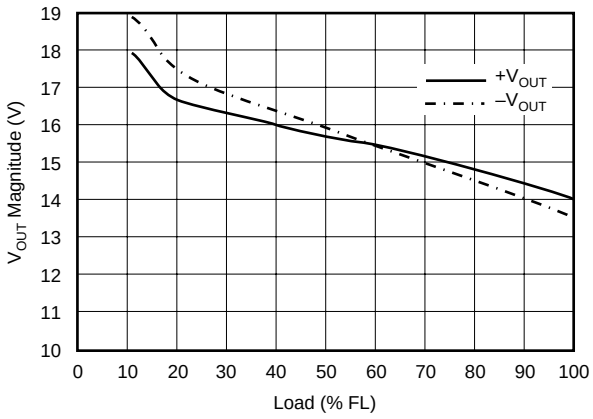
TYPICAL PERFORMANCE CURVES (DCP010515D Specific)

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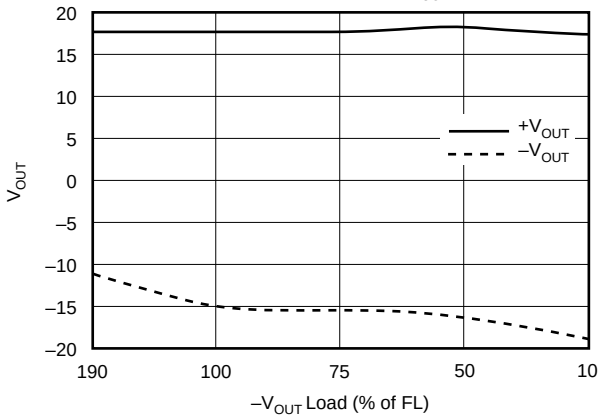
DCP010515D OUTPUT vs INPUT VOLTAGE (75% Load)



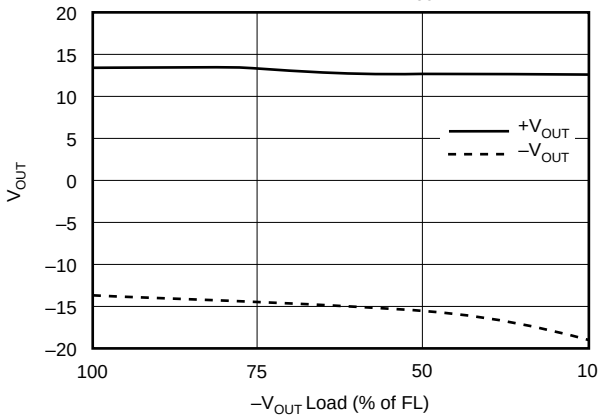
DCP010515D OUTPUT VOLTAGE vs LOAD



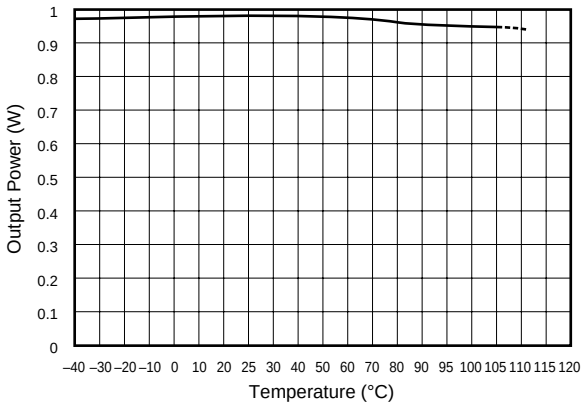
DCP010515D LOAD BALANCE (+V_{OUT} Load = 10%)



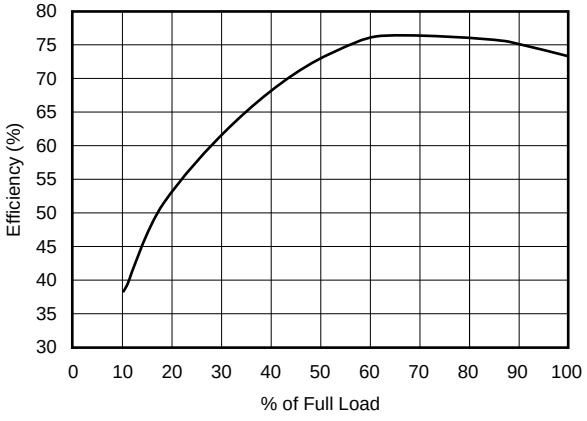
DCP010515D LOAD BALANCE (+V_{OUT} Load = 100%)



DCP010515D OUTPUT POWER vs TEMPERATURE



DCP010515D EFFICIENCY vs LOAD



FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP0105 offers 1W of unregulated output power from a 5V input source with a typical efficiency of up to 75%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC.

POWER STAGE

This uses a push-pull, center-tapped topology switching at 400kHz (divide by 2 from 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The on-board 800kHz oscillator provides the switching frequency via a divide by 2 circuit and allows synchronization via the $SYNC_{IN}$ pins. To synchronize any number of DCP0105 family of devices, simply tie the $SYNC_{IN}$ pins together (see the Synchronization section). The watchdog circuitry protects the DC/DC against a stopped oscillator and checks the oscillator frequency which will shut down the output stage if it drops below a certain threshold—i.e., it will be tri-stated after approximately 10µs.

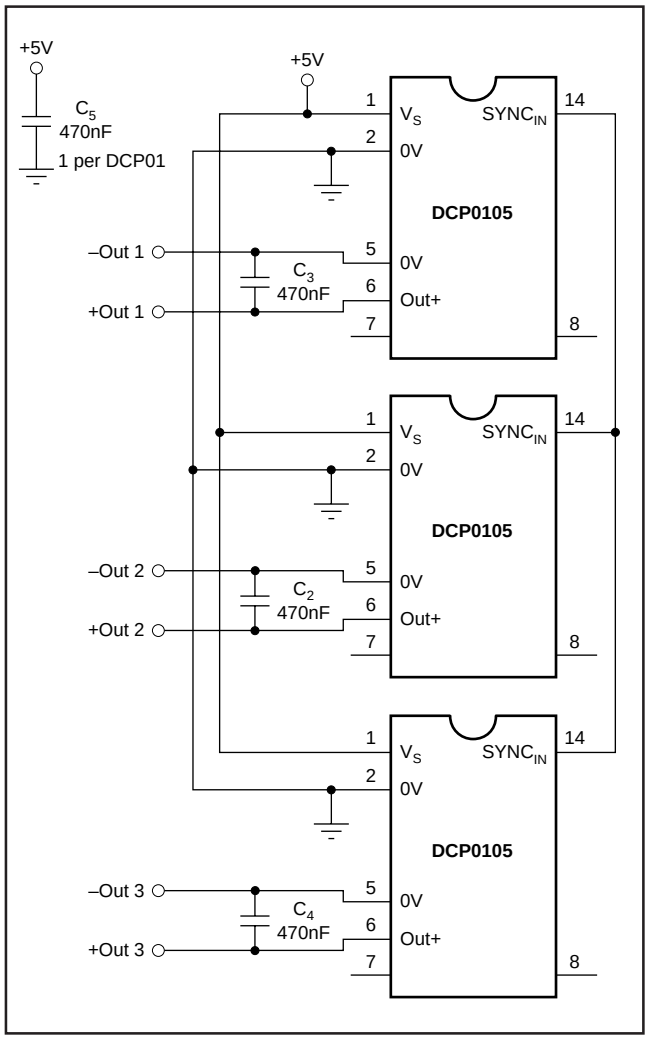


FIGURE 1. Standard Interface.

THERMAL SHUTDOWN

The DCP0105 is also protected by thermal shutdown. If the on-chip temperature reaches a predetermined value, the DC/DC will shutdown. This effectively gives indefinite short circuit protection for the DC/DC.

SYNCHRONIZATION

Any number of DCP0105 devices can be synchronized by connecting the $SYNC_{IN}$ pins on the devices together (see Figure 1). All the DCP0105 devices will then self-synchronize.

This same synchronization method will apply to other V_{IN} versions of the DCP01 family, allowing synchronization of various V_{OUT} and V_{IN} DC/DCs.

Care must taken as synchronized DCP0105s will turn on simultaneously very quickly and draw 300mA each until each output capacitor is fully charged. This may exact a heavy demand on the input power supply.

The $SYNC_{OUT}$ pin gives an unrectified 400kHz signal from the transformer. This can be used to set the timing of external circuitry on the output side. In noise sensitive applications any pick-up from the $SYNC_{OUT}$ pin can be minimized by putting a guard ring round the pin (see Figure 7).

DIVIDE BY 2 RESET

Isolated DC/DC converter performance normally suffers after power reset. This is because a change in the steady state transformer flux creates an offset after power-up. The DCP01 family does not suffer from this problem. This is achieved through a patented[1] technique employed on the divide by 2 reset circuitry resulting in no change in output phase after power interruption.

CONSTRUCTION

The DCP0105's basic construction is the same as standard ICs. There is no substrate within the molded package. The DCP0105 is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. As there is no solder within the package, the DCP0105 does not require any special PCB assembly processing. This results in an isolated DC/DC with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP0105 can be disabled or enabled by driving the $SYNC_{IN}$ pin with an open drain CMOS gate. If the $SYNC_{IN}$ pin is pulled LOW, the DCP0105 will disable. The disable time depends on the output loading but the internal shutdown takes up to 10µs. Making the gate open drain will re-enable the DCP0105. However, there is a trade-off in using this function; the DCP0105 quiescent current may increase and the on-chip oscillator may run slower. This degradation in performance is dependent on the external CMOS gate capacitance. Therefore, the smaller the capacitance, the lower the

performance decrease. Driving the $SYNC_{IN}$ pin with a CPU type tri-state output, which has a low output capacitance, offers the lowest reduction in performance.

DECOUPLING

Ripple Reduction

The high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that 0.47µF capacitors are used on V_S and V_{OUT} (see Figure 2). Both outputs on dual output DCP0105 devices should be decoupled to pin 5. In applications where power is supplied over long lines and output loading is high, it may be necessary to use a 2.2µF capacitor on the input to insure startup.

There is no restriction on the size of the output capacitor used to reduce ripple. The DCP0105 will start into any capacitive load. Low ESR capacitors will give the best reduction.

EXTERNAL SYNCHRONIZATION

The DCP0105 can be synchronized externally if required using a simple external interface. Figure 3 shows a universal interface using a 4066 quad switch. The CTL and $SYNC_{ON}$ pins are used to select external synchronization or self-synchronization.

This interface can also be used to stop (disable) the DCP0105.

CTL	$SYNC_{ON}$	FUNCTION
1	1	External Sync
—	0	Self-Sync
0	1	Device Stop

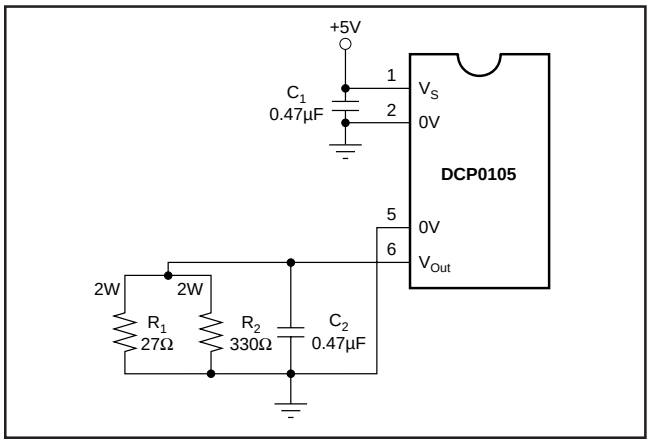


FIGURE 2. DCP010505 Fully Loaded.

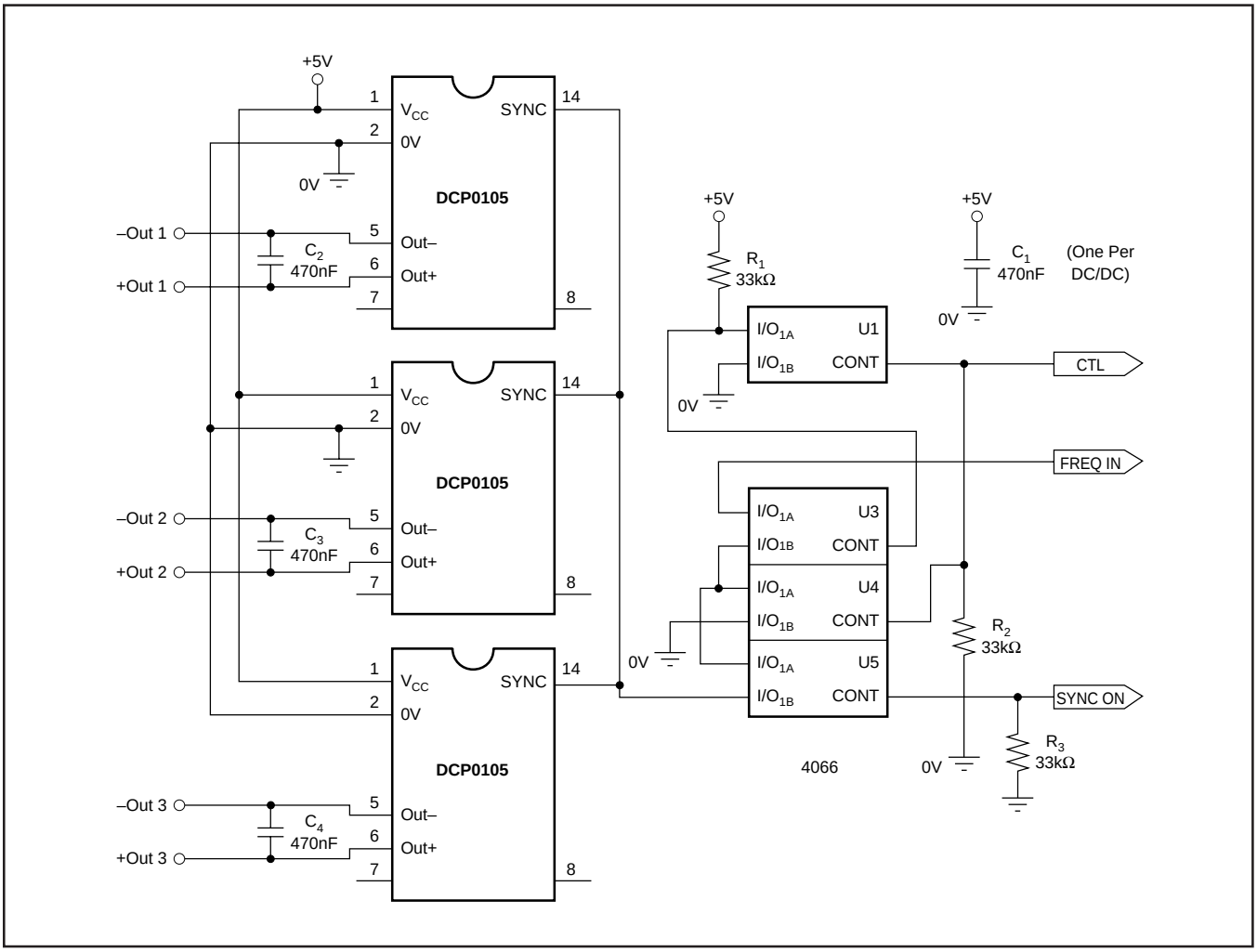


FIGURE 3. Universal Interface.

Connecting the DCP0105 in Series

Multiple DCP0105 isolated 1W DC/DC converters can be connected in series to provide non-standard voltage rails. This is possible by utilizing the floating outputs provided by the DCP0105's galvanic isolation.

Connect the positive V_{OUT} from one DCP0105 to the negative V_{OUT} (0V) of another (see Figure 4). If the $SYNC_{IN}$ pins are tied together, the self-synchronization feature of the DCP0105 will prevent beat frequencies on the voltage rails. The SYNC feature of the DCP0105 allows easy series connection without external filtering which is necessary in competing solutions.

The outputs on dual output DCP0105 versions can also be connected in series to provide 2 times the magnitude of V_{OUT} (see Figure 5). For example, a dual 12V DCP010512D could be connected to provide a 24V rail.

Connecting the DCP0105 in Parallel

If the output power from one DCP0105 is not sufficient, it is possible to parallel the outputs of multiple DCP0105s (see Figure 6). Again, the SYNC feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

THERMAL MANAGEMENT LAYOUT

To maximize the thermal performance of the DCP0105, taking more care in the PCB layout can provide the most efficient thermal dissipation paths from the DC/DC. The input controller IC and the rectifier diodes inside the DCP0105 are bonded directly onto the internal leadframe. The leadframe, being almost 100% copper, provides an excellent path for dissipated heat and does so significantly more efficiently than FR4 PCBs or ceramic substrates found in alternate packaging technology DC/DCs.

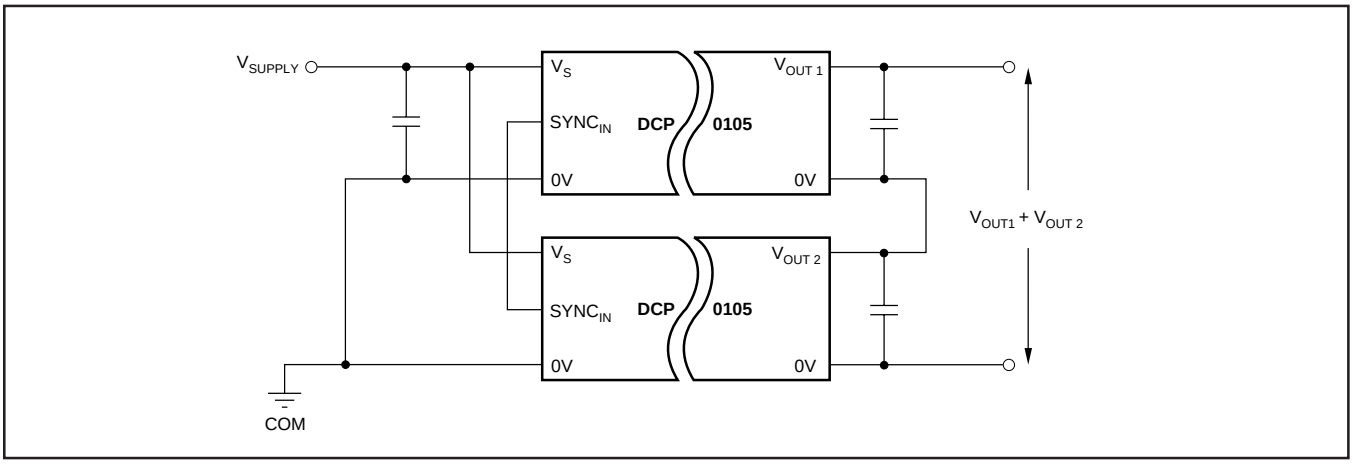


FIGURE 4. Connecting the DCP0105 in Series.

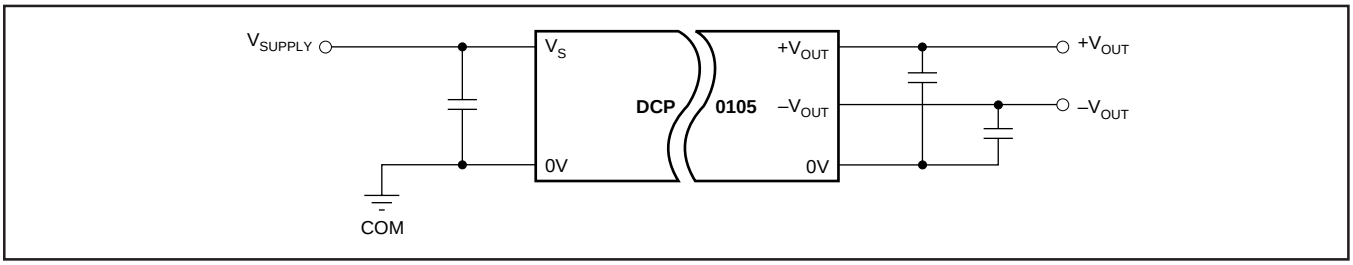


FIGURE 5. Connecting Dual Outputs in Series.

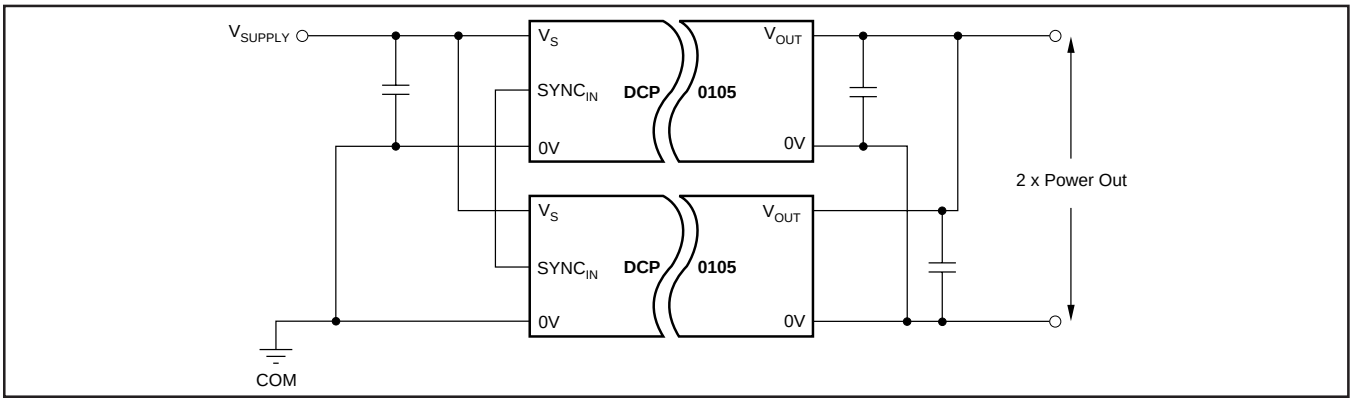


FIGURE 6. Connecting Multiple DCP0105s in Parallel.

Most of the dissipated heat comes from input side common (pin 2). To a lesser extent, the $+V_{OUT}$ pin (pin 6) also dissipates heat from the package. In the layout shown in Figure 7, the large copper areas next to pins 2 and 6 will provide excellent heat dissipation paths.

The tracking in Figure 7, shown in dotted lines, will provide shielding for the $SYNC_{IN}$ (pin 14) and $SYNC_{OUT}$ (pin 7) pins if necessary.

As described earlier in the Disable/Enable section of this data sheet, any additional capacitance to the 25pF internal capacitor at the $SYNC_{IN}$ pin will affect performance. If there is the possibility of significant leakage capacitance at the $SYNC_{IN}$ pin, it can be shielded as shown.

As described earlier in the Synchronization section of this data sheet, the $SYNC_{OUT}$ pin can be shielded as shown to minimize noise pick-up in sensitive applications.

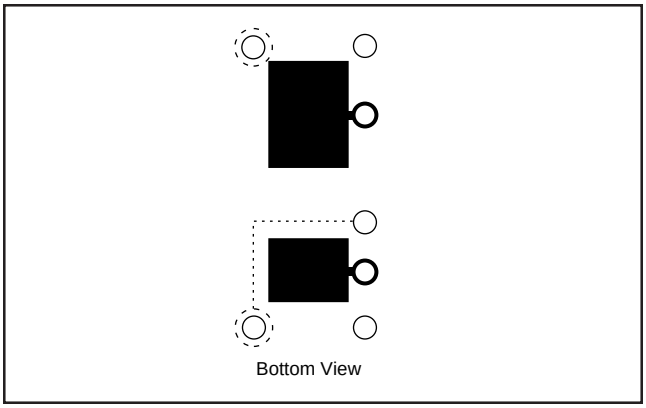


FIGURE 7. Thermal Management Layout.

LAYOUT FOR DCP0105 AND SIP PRODUCTS

Figure 8 shows a layout to allow the use of a DCP0105 and a competitive SIP isolated DC/DC converter.

POST REGULATION OF THE DCP010505P USING THE LP2986 LDO REGULATOR

In digital applications where the load range is wide or evolving, or the input supply voltage is not well regulated and 5V±5% or 5V±V10% cannot be guaranteed, it is often necessary to have a regulated 5V output from the DCP0105.

It is possible to post regulate the $5V_{OUT}$ DCP0105 and still guarantee a minimum V_{OUT} of 4.75V. This still gives the benefits of isolation in reducing the power supply noise to 5V digital circuitry.

By using an ultra-low dropout regulator (e.g., National Semiconductor's LP2986IM-5.0) in series with the output of a $5V_{OUT}$ DCP0105, it is possible to supply up to 100% load current (depending on V_{IN}). Figure 9 shows the typical load current for the post-regulated $5V_{IN}/5V_{OUT}$ DCP010505. It is possible with a V_{IN} of 5V to supply 130mA. Because of the 1:1 line regulation of the DCP0105, a 5% change in the input will result in a 5% change in the output. Therefore, the amount of current that the LDO can deliver is strongly dependent on the V_{IN} of the DCP010505. With a V_{IN} of 5.25V, the LP2986 LDO can deliver up to 165mA.

The LP2986 LDO has a very low dropout voltage of typically less than 180mV, which allows us to deliver 4.75V guaranteed from a $5V_{OUT}$ unregulated DC/DC. It also offers low output flagging and shutdown capability and is supplied in either MSOP-8 or SO-8 packages ensuring additional board area is minimal and low profile is maintained.

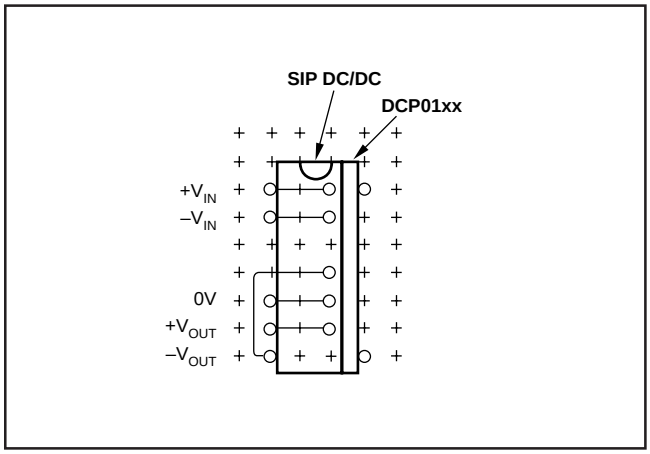


FIGURE 8. PCB Layout for DCP0105 and Competitive SIP DC/DC.

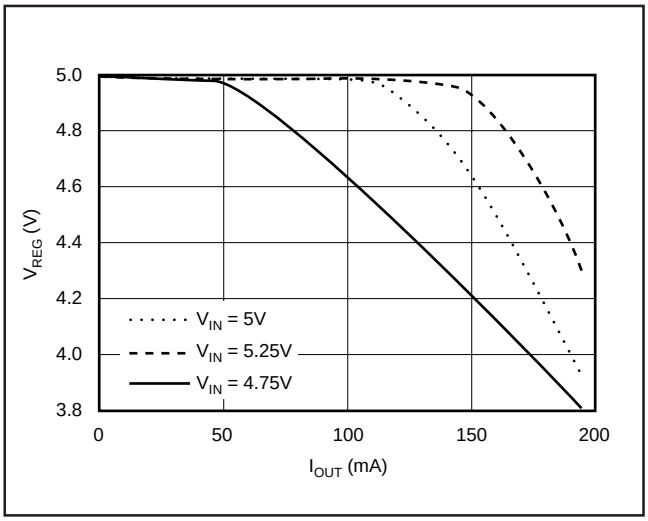


FIGURE 9. DCP010505P AND LP2986 Regulator.

DCP01 AND LP2986 APPLICATION CIRCUIT

Figure 10 shows the LP2986 in series with the DCP010505 output. The 2.2µF capacitor on the input of the LP2986 and the 4.7µF capacitor on the output are the minimum recommended for good ripple reduction. Pin 7 on the LP2986 flags an error by going LOW if the output drops 5% below nominal.

OTHER LDO REGULATORS

The SGS-Thomson L4940V5 LDO can also be used to post regulate the $5V_{OUT}$ DCP010505 and can deliver a regulated minimum 4.75V up to 135mA.

The $5V_{OUT}$ DCP010505 can also be post regulated with the Micrel MIC5207 which offers up to 180mA output drive with a typical dropout voltage of 165mV at 150mA. The MIC5207 is available in a micro-sized SOT23-5 package which gives the minimum additional board area for post regulation.

PREDICTING OUTPUT VOLTAGE VERSUS LOAD

The Load Regulation specifications are calculated as follows:

CONDITION	CALCULATION
10% to 100% Load	(V_{OUT} at 10% load – V_{OUT} at 100% load)/ V_{OUT} at 75% load
10% to 25% Load	(V_{OUT} at 10% load – V_{OUT} at 25% load)/ V_{OUT} at 25% load
10% to 75% Load	(V_{OUT} at 10% load – V_{OUT} at 75% load)/ V_{OUT} at 75% load
75% to 100% Load	(V_{OUT} at 75% load – V_{OUT} at 100% load)/ V_{OUT} at 75% load

1. To predict the output voltage at 100% load take the measured or specified voltage at 75% load and multiply by (1 + Load Reg 75% to 100%). For example a DCP010505P typical V_{OUT} at 100% load will be 5V x (1 – 8%) = 4.6V.
2. To predict the output voltage at 10% load take the measured or specified voltage at 75% load and multiply by (1 + Load Reg 10% to 75%). For example a DCP010505P typical V_{OUT} at 10% load will be 5V x (1 + 17%) = 5.85V.
3. To predict the output voltage at 25% load on higher V_{OUT} versions take the measured or specified voltage at 75% load and multiply by (1 + Load Reg 25% to 75%). For example a DCP010512P typical V_{OUT} at 25% load will be 12V x (1 + 12%) = 13.4V. To then estimate the voltage at 10% load take the previously calculated V_{OUT} at 25% load and multiply by (1 + Load Reg 10% to 25%). In this case the typical V_{OUT} at 10% load will be 13.4V x (1 + 7%) = 14.3V.

To obtain predictions for loads other than those specified assume the V_{OUT} versus load characteristic is linear between the load points and calculate accordingly. The 10% to 100% load specification guarantees the maximum voltage excursion for any load between 10% to 100% with respect to V_{OUT} at 75% load.

The above does not take into consideration line regulation and assumes a nominal input voltage. The 1:1 line regulation of the DCP01 family means that a percentage change in the input will give a corresponding percentage change in the output.

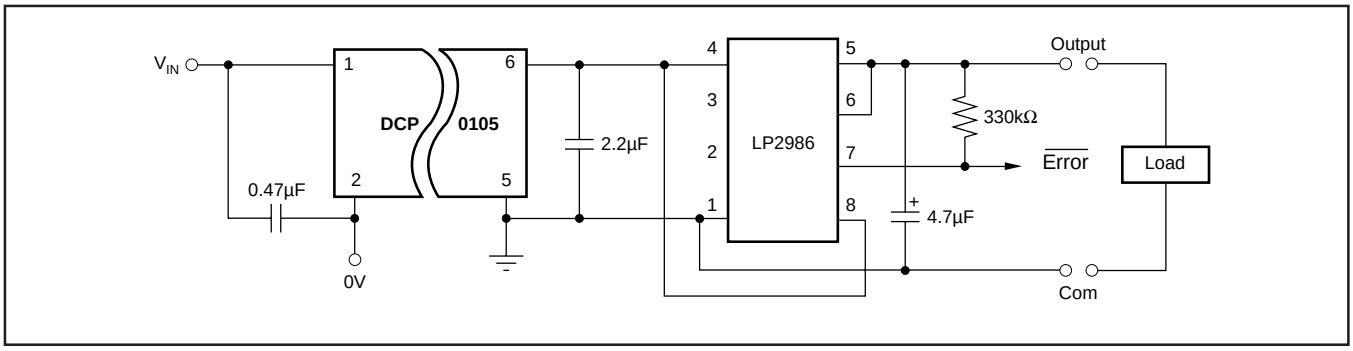


FIGURE 10. Post Regulation of DCP010505P.

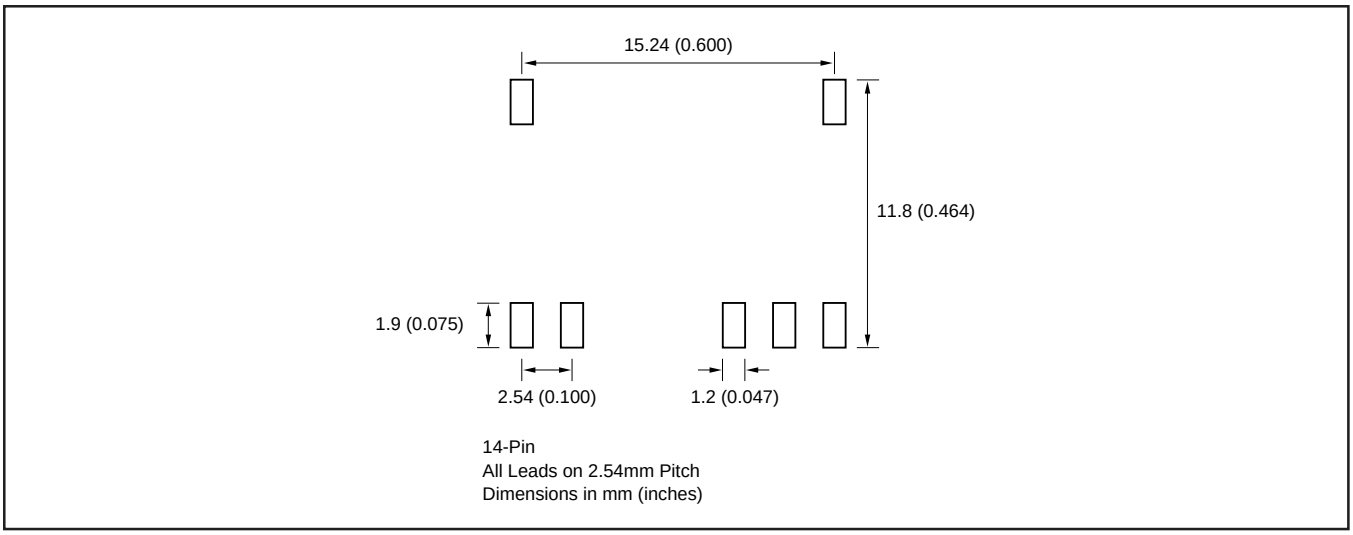


FIGURE 11. PCB Pad Size and Placement for "U" Package.