PL133-27

Low-Power, 1.62V to 3.63V, 1:2 Inverting Fanout Buffer IC

Features

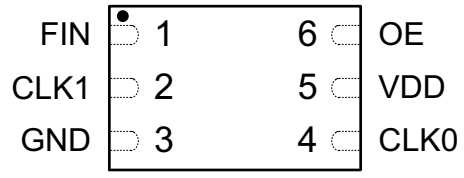
- Two LVCMOS Outputs
- Input/Output Frequency: 1 MHz to 150 MHz
- Supports LVCMOS or Sine-Wave Input Clock
- Extremely Low Additive Jitter
- 8 mA Output Drive Strength
- Low Current Consumption
- Single 1.8V, 2.5V, or 3.3V ±10% Power Supply
- Operating Temperature Range:
  - 0° to +70°C (Commercial)
  - –40° to +85°C (Industrial)
- Available in TDFN-6L Green/RoHS-Compliant Package

General Description

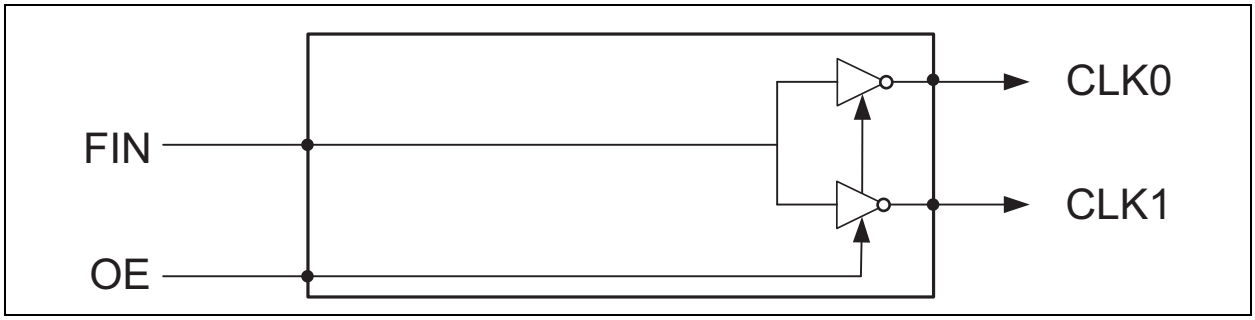
The PL133-27 is an advanced inverting fanout buffer design for high performance, low-power, small form-factor applications. The PL133-27 accepts a reference clock input of 1 MHz to 150 MHz and produces two outputs of the same frequency. Reference clock inputs may be LVCMOS or sine-wave signals (the inputs are internally AC-coupled). PL133-27 is designed to fit in a small 2 mm x 1.3 mm x 0.6 mm TDFN package and offers the best phase noise, jitter performance, and lowest power consumption of any comparable IC.

Package Type

PL133-27
2 mm x 1.3 mm TDFN
(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage Range (V_{DD}) ..... –0.5V to +4.6V
Input Voltage Range (V_{IN}) ..... –0.5V to V_{DD}+0.5V
Output Voltage Range (V_{OUT}) ..... –0.5V to V_{DD}+0.5V

† Notice: Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. Parts are tested to commercial grade only.

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Frequency	f_{IN}	1	—	150	MHz	@ V_{DD} = 2.5V and 3.3V
		1	—	65		@ V_{DD} = 1.8V
Input Signal Amplitude	—	0.8	—	V_{DD}	V_{PP}	Internally AC-coupled
Output Rise Time	t_r	—	2	3	ns	15 pF Load, 10/90%V_{DD}, 3.3V
Output Fall Time	t_f	—	2	3	ns	15 pF Load, 90/10%V_{DD}, 3.3V
Output-to-Output Skew	—	—	—	500	ps	—
Duty Cycle	—	45	50	55	%	Input duty cycle is 50%

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Supply Current, Dynamic	I_{DD}	—	1.8	—	mA	V_{DD} = 3.3V, 25 MHz, No Load
		—	1.3	—		V_{DD} = 2.5V, 25 MHz, No Load
		—	0.8	—		V_{DD} = 1.8V, 25 MHz, No Load
Operating Voltage	V_{DD}	1.62	—	3.63	V	—
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = +4 mA, V_{DD} = 3.3V
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OL} = –4 mA, V_{DD} = 3.3V
Output Current	I_{OSD}	8	—	—	mA	V_{OL} = 0.4V, V_{OH} = 2.4V, V_{DD} = 3.3V

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Operating Temperature	T_A	–40	—	+85	°C	—
Storage Temperature	T_S	–65	—	+150	°C	—

2.0 NOISE CHARACTERISTICS

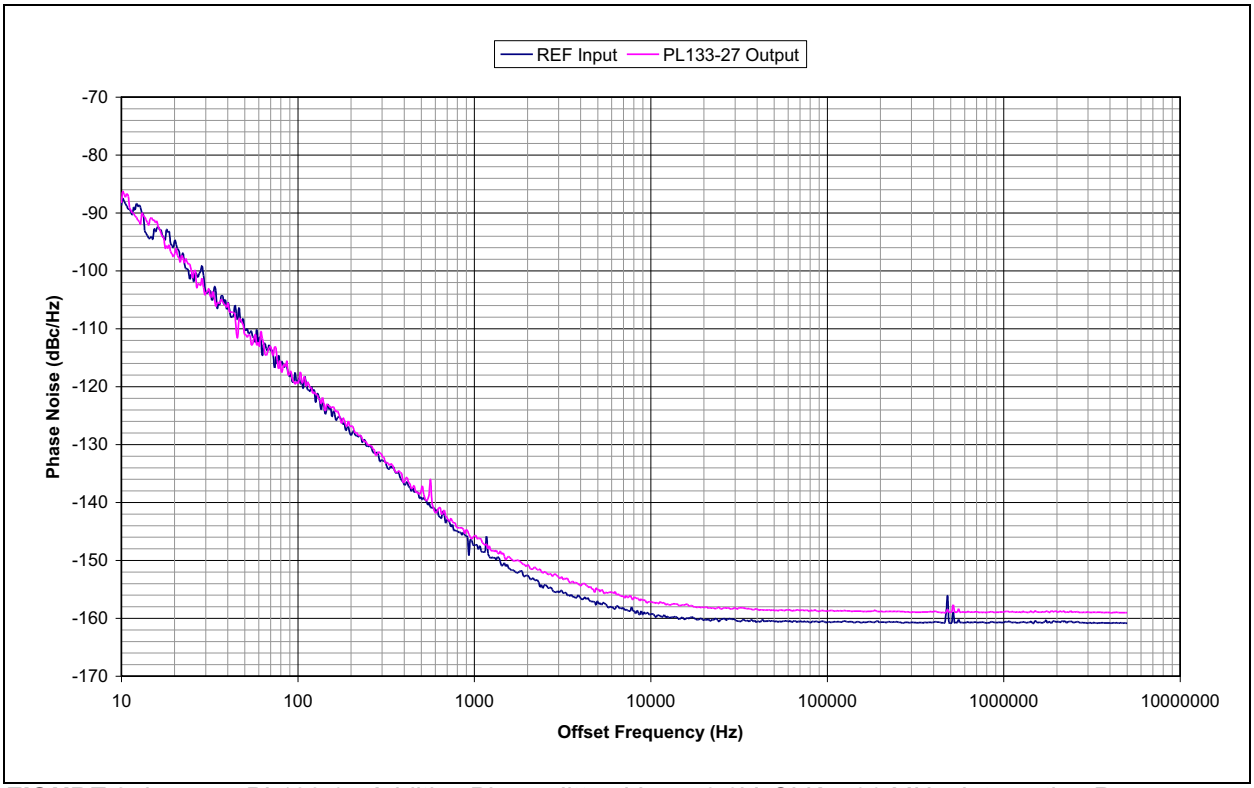


FIGURE 2-1: *PL133-27 Additive Phase Jitter. V_{DD} = 3.3V, CLK = 26 MHz, Integration Range: 12 kHz to 5 MHz, 0.127 ps Typical.*

TABLE 2-1: NOISE CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Additive Phase Jitter		—	130	—	fs	V_{DD} = 3.3V, Frequency = 26 MHz Offset = 12 kHz ~ 5 MHz
		—	150	—		V_{DD} = 3.3V, Frequency = 100 MHz Offset = 12 kHz ~ 20 MHz

When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called Additive Phase Jitter. The formula for the Additive Phase Jitter is as follows:

EQUATION 2-1:

$$\text{Additive Phase Jitter} = \sqrt{\text{Output Phase Jitter}^2 - \text{Input Phase Jitter}^2}$$

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	FIN	I	Reference clock input.
2	CLK1	O	Clock output (inverted).
3	GND	P	Ground connection.
4	CLK0	O	Clock output (inverted).
5	VDD	P	V_{DD} connection.
6	OE	I	Output enable input.

3.1 Layout Recommendations

The following guidelines are to assist you with a performance-optimized PCB design.

3.1.1 SIGNAL INTEGRITY AND TERMINATION CONSIDERATIONS

- Keep traces short.
- Trace = Inductor. With a capacitive load this equals ringing.
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

3.1.2 DECOUPLING AND POWER SUPPLY CONSIDERATIONS

- Place decoupling capacitors as close as possible to the VDD pin to limit noise from the power supply.
- Multiple VDD pins should be decoupled separately for best performance.
- The addition of a ferrite bead in series with VDD can help prevent noise from other board sources.
- The value of decoupling capacitor is frequency dependent. Typical values to use are 0.1 µF for designs using crystals <50 MHz and 0.01 µF for designs using crystals >50 MHz.

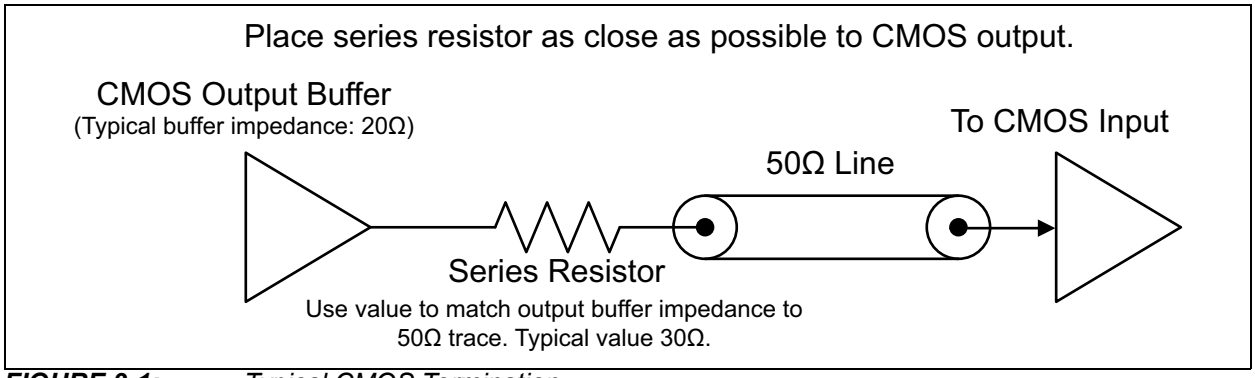


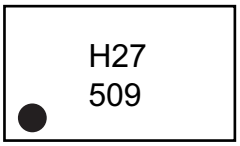
FIGURE 3-1: *Typical CMOS Termination.*

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

6-Lead TDFN*

Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

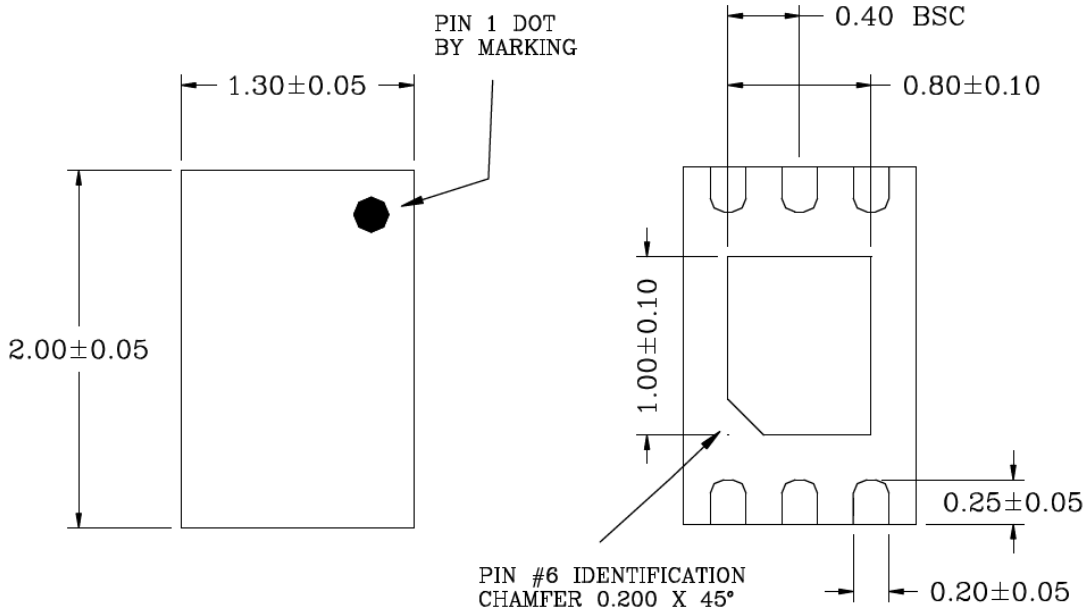
Underbar (_) and/or Overbar (¯) symbol may not be to scale.

6-Lead TDFN 2.0 mm x 1.3 mm Package Outline Drawing and Recommended Land Pattern

TITLE

6 LEAD TDFN 2.0x1.3 mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TDFN2013-6LD-PL-1	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu

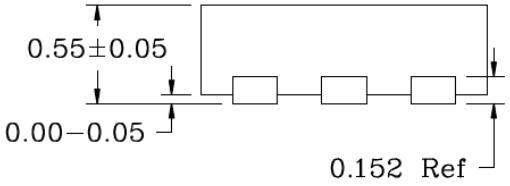


TOP VIEW

NOTE: 1, 2

BOTTOM VIEW

NOTE: 1, 2



SIDE VIEW

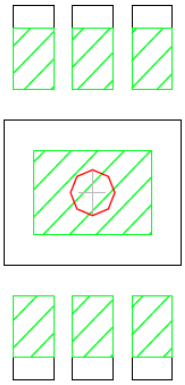
NOTE: 1, 2

NOTES
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mmm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. UNIT IN mm.
5. SHADED AREA IS SOLDER STENCIL OPENING.
6. RECOMMENDED VIA SIZE IS 0.30-0.35mm.

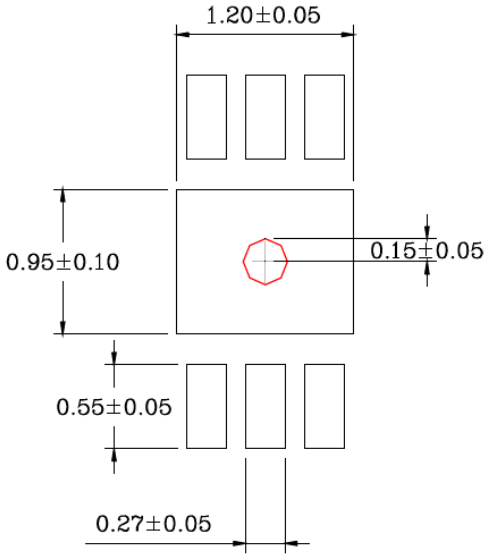
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern TDFN2013-6LD-PL-1

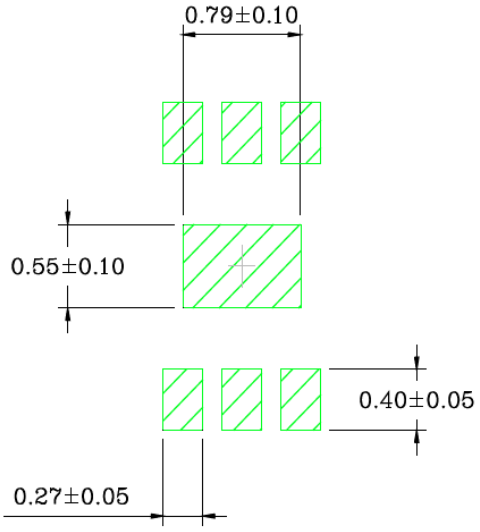
RECOMMENDED LAND PATTERN



STACKED-UP
NOTE: 4, 5, 6



EXPOSED METAL TRACE
NOTE: 4, 6



SOLDER STENCIL OPENING
NOTE: 4, 5

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2020)

- Converted Micrel document PL133-27 to Microchip data sheet DS20006429A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	-X
Device	Package	Temp. Range	Packing

Device:	PL133-27:	Low-Power, 1.62V to 3.63V, 1:2 Fanout Buffer IC	
Package:	G	=	6-Lead 2 mm x 1.3 mm TDFN
Temperature Range:	C	=	0°C to +70°C (NiPdAu Lead-Free)
	I	=	–40° to +85°C (NiPdAu Lead-Free)
Tape and Reel:	<blank>	=	20/Bag
	R	=	3,000/Reel

Examples:

a) PL133-27GC:
6-Lead TDFN, 0°C to +70°C Temperature Range, 20/Bag

b) PL133-27GI:
6-Lead TDFN, –40° to +85°C Temperature Range, 20/Bag

c) PL133-27GC-R:
6-Lead TDFN, 0°C to +70°C Temperature Range, 3,000/Reel

d) PL133-27GI-R:
6-Lead TDFN, –40° to +85°C Temperature Range, 3,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
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ISBN: 978-1-5224-6891-2