

**Document Title****256K x 16 bit Super Low Power and Low Voltage Full CMOS RAM****Revision History**

Revision No.	History	Draft date	Remark
0.0	Initial Draft	May. 2 <sup>nd</sup> , 2004	Final
0.1	Added <u>G(Pb-Free)</u> and <u>H(Pb-Free &amp; Halogen Free)</u> descriptions	Oct. 26 <sup>th</sup> , 2005	Final
0.2	Removed 60ns descriptions	Aug. 22 <sup>nd</sup> , 2006	Final
0.3	Added Power Up Sequence	Sep. 6 <sup>th</sup> , 2006	Final

## 256K x 16 bit Super Low Power and Low Voltage Full CMOS RAM

### FEATURES

- Process Technology : Full CMOS
- Organization : 256K x 16
- Power Supply Voltage : 2.7~3.3V
- Three state output and TTL Compatible
- Package Type : 48-FBGA-6.00x8.00 mm<sup>2</sup>
- Separated I/O power(VCCQ) & Core Power(VCC)
- Easy memory expansion with /CS1, CS2, and /OE features
- Automatic power-down when deselected

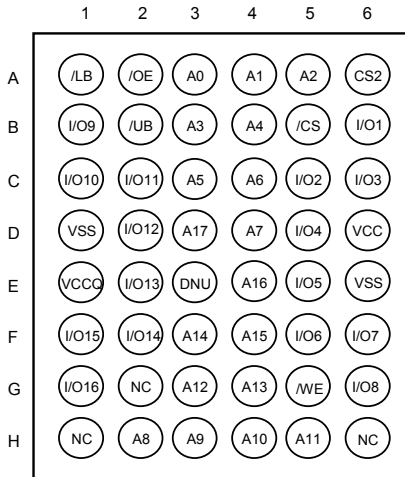
### PRODUCT FAMILY

Product Family	Operating Temperature	Operating Voltage (V)			Speed	Power Dissipation					
		Min.	Typ.	Max.		ICC1		ICC2		ISB1 (CMOS Standby Current)	
						f = 1MHz		f = fmax			
						Typ.	Max.	Typ.	Max.	Typ.	Max.
CMP0417AA0-F70I	Industrial (-40~85°C)	2.7	3.0	3.3	70ns	1.5mA	3mA	12mA	20mA	30uA	70uA

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at Vcc = Vcc (typ) and T<sub>A</sub> = 25C.

2. F=FBGA, G=FBGA(Pb-Free), H=FBGA(Pb-Free & Halogen Free), W=WAFER

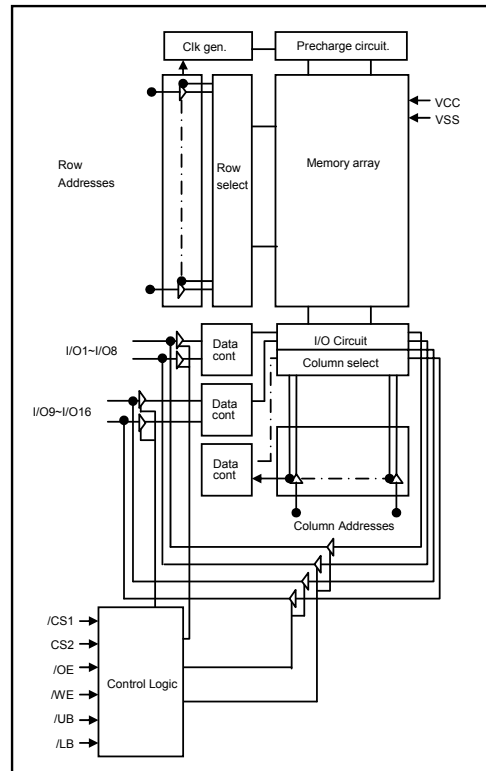
### PIN DESCRIPTION



48-FBGA : Top View(Ball Down)

Name	Function	Name	Function
CS2	Chip Select Input	VCC	Core Power
/CS1	Chip Select Input	VCCQ	I/O Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte(I/O9~16)
A0~A17	Address Inputs	/LB	Lower Byte(I/O 1~8)
I/O1~I/O16	Data Inputs/Outputs	DNU	Do Not Use
NC	No Connection		

### FUNCTIONAL BLOCK DIAGRAM



## PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
CMP0417AA0-F70I	48-FBGA, 70ns, VCC=3.0V, VCCQ=3.0V(2.5V,1.8V)

1. F=FBGA, G=FBGA(Pb-Free), H=FBGA(Pb-Free & Halogen Free), W=WAFER

## FUNCTIONAL DESCRIPTION

/CS1	CS2	/OE	/WE	/LB	/UB	I/O1-8	I/O9-16	Mode	Power
H	H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselect/Power-down	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselect/Power-down	Standby
X <sup>1)</sup>	H	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	Deselect/Power-down	Standby
L	H	H	H	L	X <sup>1)</sup>	High-Z	High-Z	Output Disabled	Active
	H	H	H	X <sup>1)</sup>	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
				H	L	High-Z	Dout	Upper Byte Read	Active
				L	L	Dout	Dout	Word Read	Active
		X <sup>1)</sup>	L	L	H	Din	High-Z	Lower Byte Write	Active
				H	L	High-Z	Din	Upper Byte Write	Active
				L	L	Din	Din	Word Write	Active

1. X means don't care.(Must be low or high state)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.2 to Vcc+0.3V	V
Voltage on Vcc supply relative to Vss	Vcc	-0.2 to 3.6	V
Power Dissipation	PD	1.0	W
Storage temperature	TSTG	-65 to 150	°C
Operating Temperature	TA	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for Industrial periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	CMP0417AA0						Unit
		Min	Max	Min	Max	Min	Max	
Supply voltage	VCC	2.7	3.3	2.7	3.3	2.7	3.3	V
I/O operating voltage (VCCQ ≤ VCC)	VCCQ	2.7	3.3	2.25	2.75	1.65	1.95	V
Ground	VSS	0	0	0	0	0	0	V
Input high voltage	VIH	0.8VCCQ	VCC+0.2 <sup>2)</sup>	0.8VCCQ	VCC+0.2 <sup>2)</sup>	0.8VCCQ	VCC+0.2 <sup>2)</sup>	V
Input low voltage	VIL	-0.2 <sup>3)</sup>	0.2VCCQ	-0.2 <sup>3)</sup>	0.2VCCQ	-0.2 <sup>3)</sup>	0.2VCCQ	V

Note :

1.TA=-40 to 85°C, otherwise specified.

2. Overshoot : Vcc+1.0V in case of pulse width≤20ns.

3. Undershoot : -1.0V in case of pulse width≤20ns.

4. Overshoot and undershoot are sampled, not 100% tested.

**CAPACITANCE**<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

1. Capacitance is sampled, not 100% tested.

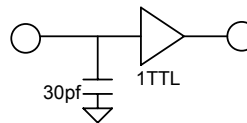
**DC AND OPERATING CHARACTERISTICS**

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	uA
Output leakage current	I <sub>LO</sub>	/CS=V <sub>IH</sub> , CS2=V <sub>IH</sub> , /OE=V <sub>IH</sub> or /WE=V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	uA
Average operating current	I <sub>CC1</sub>	Cycle time=1us, 100%duty, I <sub>IO</sub> =0mA, /CS≤0.2V, CS2=V <sub>IH</sub> , V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	1.5	3	mA
	I <sub>CC2</sub>	Cycle time=Min, I <sub>IO</sub> =0mA, 100% duty, /CS=V <sub>IL</sub> , CS2=V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	15	25	mA
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =0.5mA			0.2V <sub>CCQ</sub>	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-0.5mA	0.8V <sub>CCQ</sub>			V
Standby Current(TTL)	I <sub>SB</sub>	/CS=V <sub>IH</sub> , CS2=V <sub>IH</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.3	mA
Standby Current(CMOS)	I <sub>SB1</sub>	/CS≥V <sub>CC</sub> -0.2V, CS2≤0.2V, Other inputs=0~V <sub>CC</sub>	-	-	70	uA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.2 to VCC-0.2V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 0.5\*VCCQ  
 Output load (see right) : CL=30pF+1TTL



## AC CHARACTERISTICS (VCC=2.7V~3.3V, Industrial product : T<sub>A</sub>=-40 to 85°C)

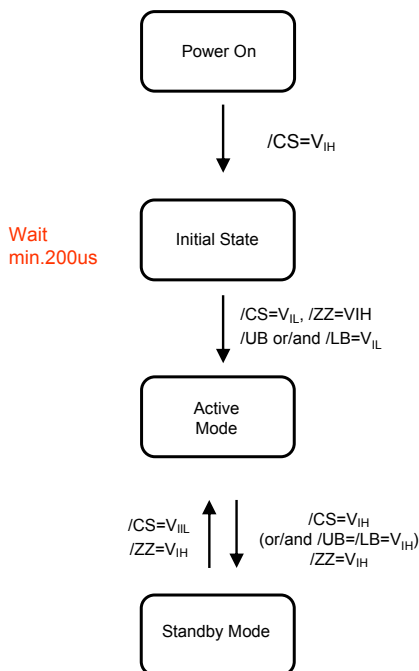
Parameter List		Symbol	70ns		Units
			Min	Max	
Read	Read Cycle Time	tRC	70	-	ns
	Address Access Time	tAA	-	70	ns
	Chip Select to Output	tCO	-	70	ns
	Output Enable to Valid Output	tOE	-	25	ns
	/UB, /LB Access Time	tBA	-	70	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	/UB, /LB Enable to Low-Z Output	tBLZ	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	ns
	Chip Disable to High- Z Output	tHZ	0	5	ns
	/UB, /LB Disable to High- Z Output	tBHZ	0	5	ns
	Output Disable to High- Z Output	tOHZ	0	5	ns
	Output Hold from Address Change	tOH	5	-	ns
Write	Write Cycle Time	tWC	70	-	ns
	Chip Select to End of Write	tCW	60	-	ns
	Address Set-up Time	tAS	0	-	ns
	Address Valid to End of Write	tAW	60	-	ns
	/UB, /LB Valid to End of Write	tBW	60	-	ns
	Write Pulse Width	tWP	50	-	ns
	Write Recovery Time	tWR	0	-	ns
	Write to Output High-Z	tWHZ	0	5	ns
	Data to Write Time Overlap	tDW	20	-	ns
	Data Hold from Write Time	tDH	0	-	ns
	End Write to Output Low-Z	tOW	5	-	ns
/CS High Pulse Width <sup>1)</sup>		tCP	10	-	ns

1. /CS High Pulse Width is defined by /CS or (/UB and /LB) because /UB & /LB can make standby mode when /UB=High and /LB=High.

**Power Up Sequence**

1. Apply Power
2. Maintain stable power for a minimum of 200us with /CS=VIH

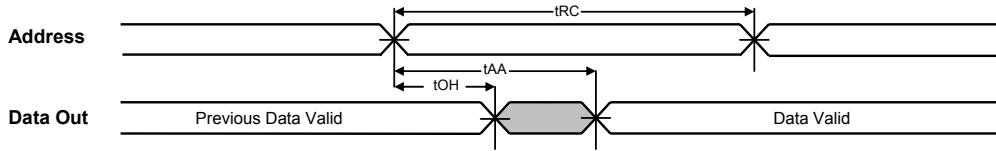
**Standby Mode State machines**



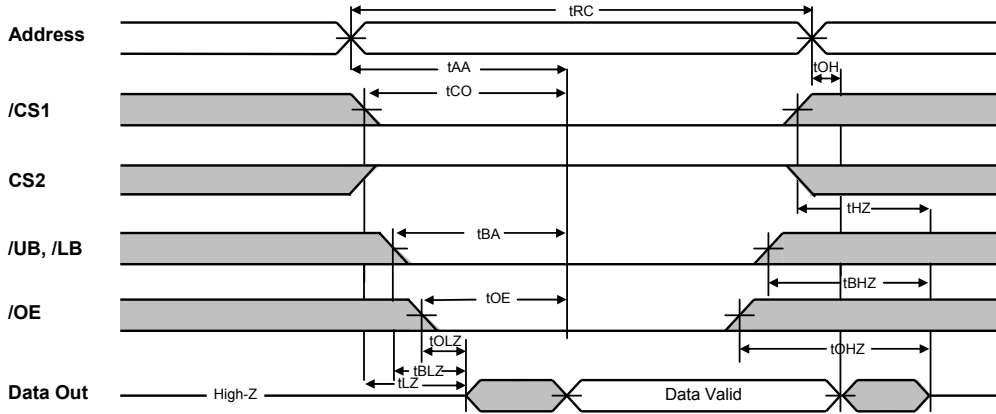
**Standby Mode Characteristics**

Mode	Memory Cell Data	Standby Current(uA)	Wait Time(us)
Standby	Valid	70 (ISB1)	0

**READ CYCLE (1)** (Address controlled, /CS1=/OE=VIL, CS2=WE=VIH, /UB or/and /LB=VIL)

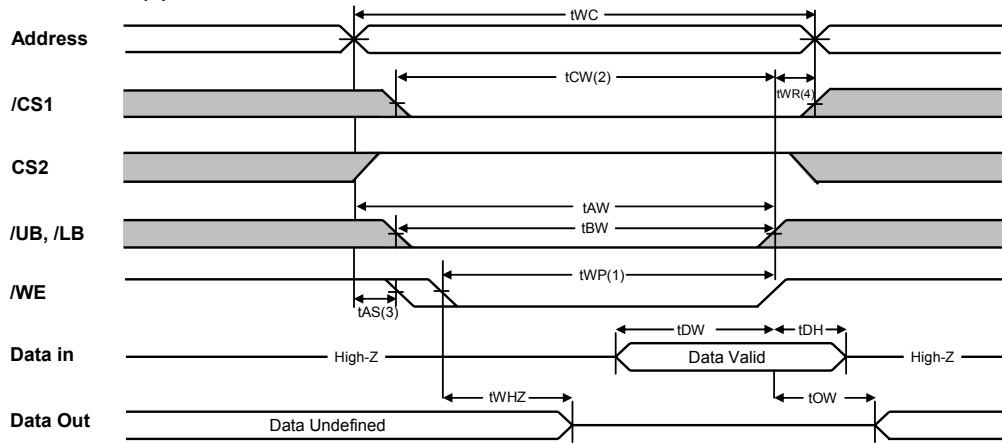


**READ CYCLE (2)** (CS2=WE=VIH)

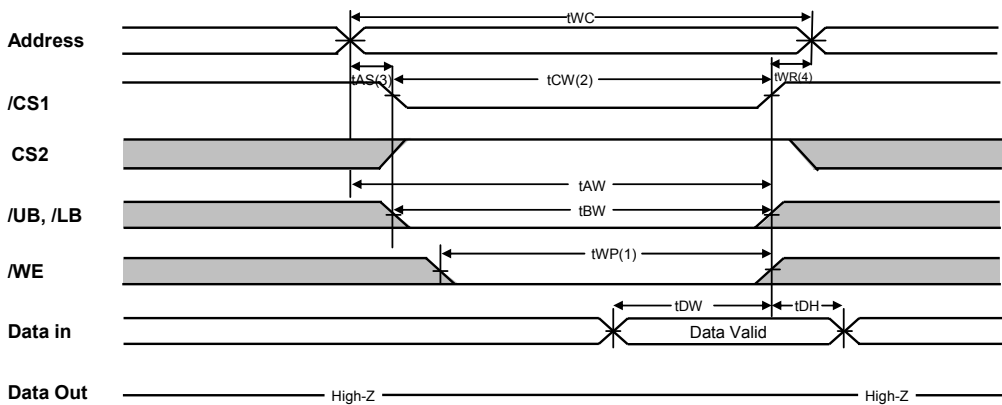


1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

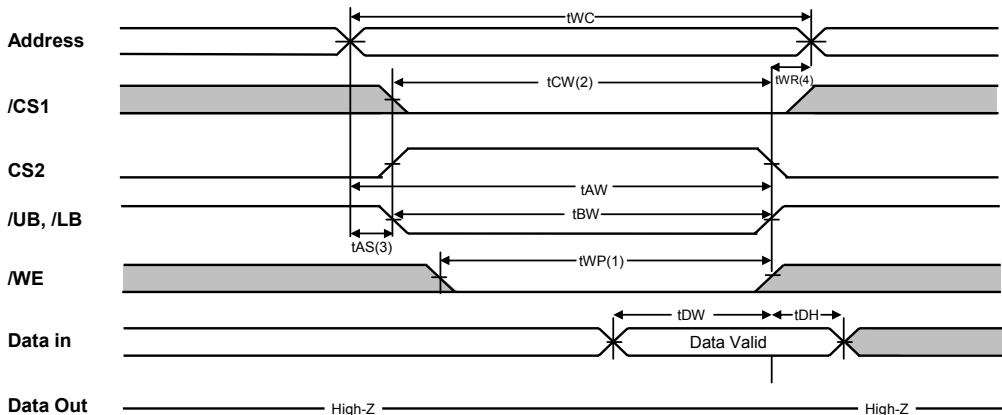
**WRITE CYCLE (1)** (/WE controlled)



**WRITE CYCLE (2)** (/CS1 controlled)

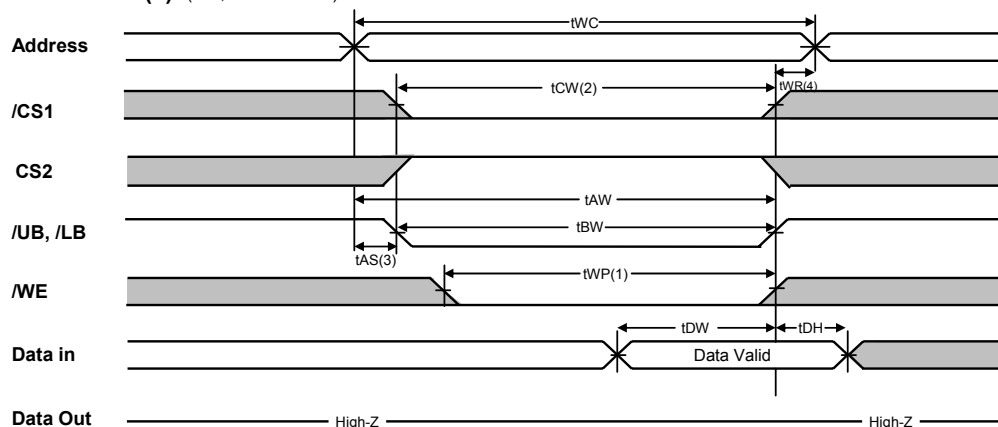


**WRITE CYCLE (3)** (CS2 controlled)





**WRITE CYCLE (4)** (/UB, /LB controlled)



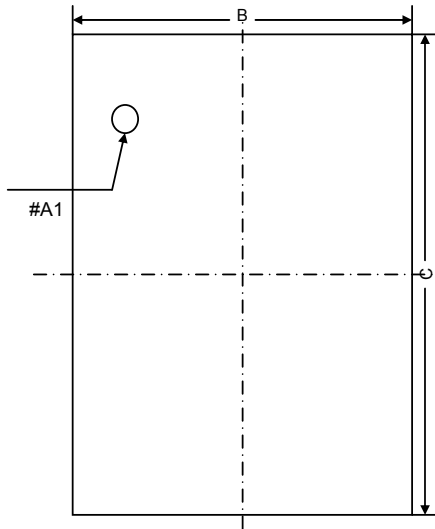
1. A write occurs during the overlap ( $t_{WP}$ ) of low /CS and /WE. A write begins when /CS goes low and /WE goes low with asserting /UB or /LB for single byte operation or simultaneously asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CS goes high and /WE goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the /CS going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as /CS or /WE going high.

PACKAGE DIMENSION

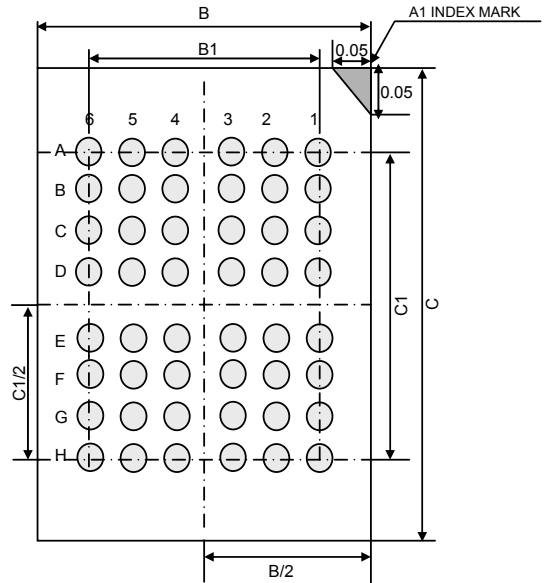
Unit : millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)

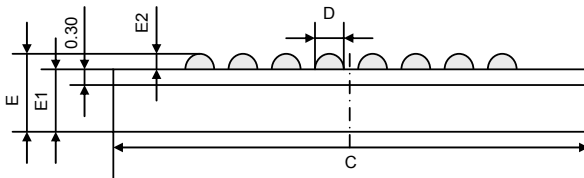
Top View



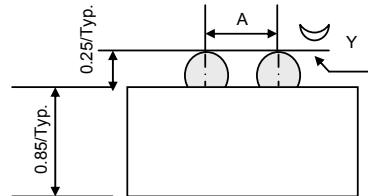
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.00	-
E1	-	0.75	-
E2	0.20	0.25	0.30
Y	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)