Non-Volatile SRAM MODULE 4Mbit (512K x 8-Bit),32Pin-DIP, 3.3V

Part No. HMN5128DV

GENERAL DESCRIPTION

The HMN5128DV Nonvolatile SRAM is a 4,194,304-bit static RAM organized as 524,288 bytes by 8 bits.

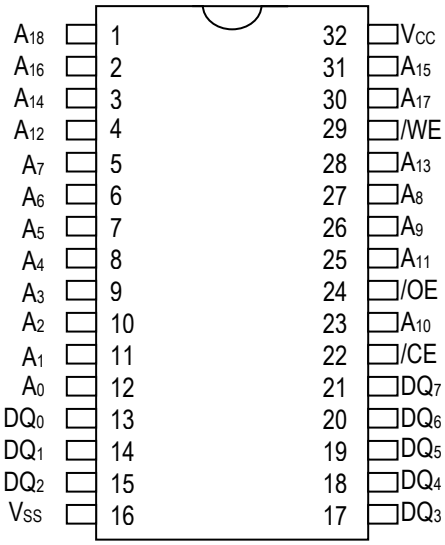
The HMN5128DV has a self-contained lithium energy source provide reliable non-volatility coupled with the unlimited write cycles of standard SRAM and integral control circuitry which constantly monitors the single 3.3V supply for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on to sustain the memory until after Vcc returns valid and write protection is unconditionally enabled to prevent garbled data. In addition the SRAM is unconditionally write-protected to prevent an inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after V_{CC} returns valid.

The HMN5128DV uses extremely low standby current CMOS SRAM's, coupled with small lithium coin cells to provide non-volatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

FEATURES

- Access time : 70, 85ns
- High-density design : 4Mbit Design
- Battery internally isolated until power is applied
- Industry-standard 32-pin 512K x 8 pinout
- Unlimited write cycles
- Data retention in the absence of V_{CC}
- 5-years typical data retention in absence of power
- Automatic write-protection during power-up/power-down cycles
- Data is automatically protected during power loss
- Conventional SRAM operation; unlimited write cycles

PIN ASSIGNMENT



32-pin Encapsulated Package

OPTIONS MARKING

- Timing

70 ns	-70
85 ns	-85

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FUNCTIONAL DESCRIPTION

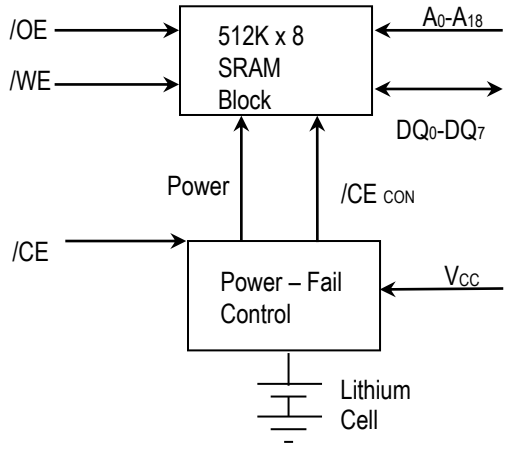
The HMN5128DV executes a read cycle whenever /WE is inactive(high) and /CE /OE are active(low). The address specified by the address inputs(A_0-A_{18}) defines which of the 524,288 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (access time) after the last address input signal is stable.

When power is valid, the HMN5128DV operates as a standard CMOS SRAM. During power-down and power-up cycles, the HMN5128DV acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

The HMN5128DV is in the write mode whenever the /WE and /CE signals are in the active (low) state after address inputs are stable. The later occurring falling edge of /CE or /WE will determine the start of the write cycle. **The write cycle is terminated by the rising edge of /CE or /WE**. All address inputs must be kept valid throughout the write cycle. /WE must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The /OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus been enabled (/CE and /OE active) then /WE will disable the outputs in t_{ODW} from its falling edge.

The HMN5128DV provides full functional capability for Vcc greater than 3.0 V and write protects by 2.8 V nominal. Power-down/power-up control circuitry constantly monitors the Vcc supply for a power-fail-detect threshold V_{PFD}. When V_{CC} falls below the V_{PFD} threshold, the SRAM automatically write-protects the data. All inputs to the RAM become “don’t care” and all outputs are high impedance. As Vcc falls below approximately 2.5 V, the power switching circuit connects the lithium energy soure to RAM to retain data. During power-up, when Vcc rises above approximately 2.5 volts, the power switching circuit connects external Vcc to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after Vcc exceeds 3.0 volts.

BLOCK DIAGRAM



PIN DESCRIPTION

A_0-A_{18} : Address Input
/CE : Chip Enable
V_{ss} : Ground
DQ_0-DQ_7 : Data In / Data Out
/WE : Write Enable
/OE : Output Enable
V_{CC} : Power (+3.3V)

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TRUTH TABLE

MODE	/OE	/CE	/WE	I/O OPERATION	POWER
Not selected	X	H	X	High Z	Standby
Output disable	H	L	H	High Z	Active
Read	L	L	H	D_{OUT}	Active
Write	X	L	L	D_{IN}	Active

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	CONDITIONS
DC voltage applied on V_{CC} relative to V_{SS}	V_{CC}	-0.5V to Vcc+0.5	
DC Voltage applied on any pin excluding V_{CC} relative to V_{SS}	V_T	-0.3V to 4.6V	$V_T \leq V_{CC}$+0.3
Operating temperature	T_{OPR}	0 to 70°C	
Storage temperature	T_{STG}	-30°C to 80°C	

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

Functional operation should be restricted to the Recommended DC Operating Conditions detailed in this data sheet.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.
Not recommend direct soldering by soldering machine, recommend by manual soldering or using socket.

RECOMMENDED DC OPERATING CONDITIONS ($T_A = T_{OPR}$)

PARAMETER	SYMBOL	MIN	TYPICAL	MAX
Supply Voltage	V_{CC}	3.0V	3.3V	3.6V
Ground	V_{SS}	0	0	0
Input high voltage	V_{IH}	2.2	-	Vcc+0.3V
Input low voltage	V_{IL}	-0.3	-	0.6V

NOTE: Typical values indicate operation at T_A = 25℃

DC ELECTRICAL CHARACTERISTICS ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Input Leakage Current	$V_{IN}=V_{SS}$ to V_{CC}	I_{LI}	-	-	±2.0	μA
Output Leakage Current	/CE=V_{IH} or /OE=V_{IH} or /WE=V_{IL}	I_{LO}	-	-	±2.0	μA
Output high voltage	I_{OH}=-1.0mA	V_{OH}	2.4	-	-	V
Output low voltage	I_{OL}= 2.0mA	V_{OL}	-	-	0.4	V
Power-fail Deselect Voltage	Threshold Select Voltage (THS = V_{SS})	V_{PFD}	2.8	2.9	3.0	V
Standby supply current	/CE=V_{IH}	I_{SB}	-	-	0.3	㎃
Standby supply current	/CE≥V_{CC}-0.2V, 0V≤V_{IN}≤0.2V, or V_{IN}≥V_{CC}-0.2V	I_{SB1}	-	-	15	μA
Operating supply current	Min.cycle,duty=100%, /CE=V_{IL}, $I_{I/O}$=0㎃, A_{17}< V_{IL} or A_{17}> V_{IH}, A_{18}< V_{IL} or A_{18}> V_{IH}	I_{CC}	-	-	8	㎃
Supply switch-over voltage		V_{SO}	-	2.5	-	V

NOTE: Typical values indicate operation at T_A = 25℃.

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READ CYCLE (T_A= T_{OPR}, V_{CCmin} ≤ V_{CC}≤ V_{CCmax})

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Read Cycle Time	t_{RC}		70		ns
Address access Time	t_{ACC}			70	ns
Chip enable access time	t_{ACE}			70	ns
Output enable to output valid	t_{OE}			40	ns
Chip enable to output in high Z	t_{CHZ}			35	ns
Output enable to output high Z	t_{OHZ}			10	ns
Output hold from address change	t_{OH}		10		ns
Output enable end to chip select end	t_{OETCE}		0		ns

WRITE CYCLE (T_A= T_{OPR}, V_{ccmin} ≤ V_{cc} ≤ V_{ccmax})

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Write Cycle Time	t_{WC}		70		ns
Chip enable to end of write	t_{CW}		70		ns
Address setup time	t_{AS}		0		ns
Address valid to end of write	t_{AW}		60		ns
Write pulse width	t_{WP}		55		ns
Write recovery time	t_{WR}		0		ns
Data valid to end of write	t_{DW}		30		ns
Data hold from write time	t_{DH}		0		ns
Output active from end of write	t_{OW}		5		ns
Write end to chip enable end	t_{WETCE}		0		ns

NOTE: 1. A write ends at the transition of /WE low to high.

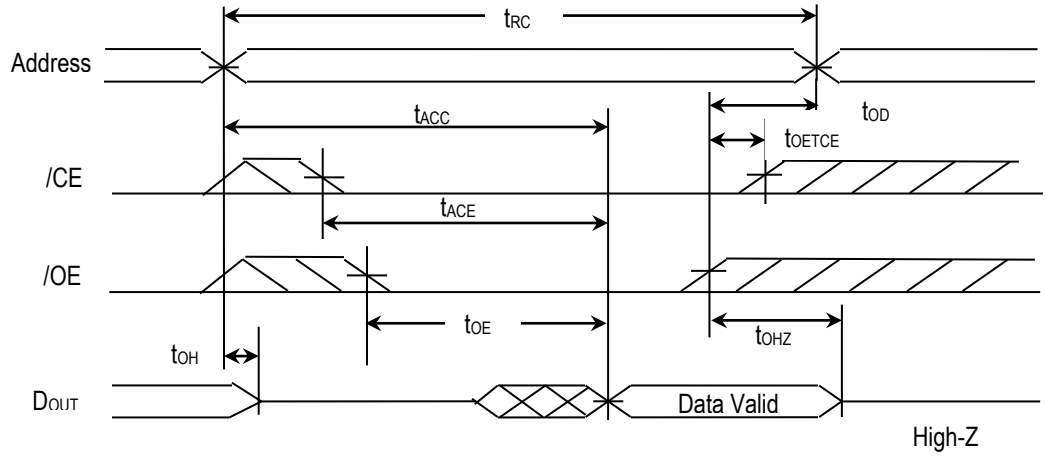
POWER-DOWN/POWER-UP CYCLE

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{PFD}(max) to V_{PFD}(min) V_{CC} Fail Time	t_F		300	-	-	μs
V_{PFD}(max) to V_{SS} V_{CC} Fail Time	t_{FB}		150	-	-	μs
V_{PFD}(max) to V_{PFD}(min) V_{CC} Rise Time	t_R		10	-	-	μs
Write Protect Time	t_{WPT}	Delay after Vcc slews down past V_{PFD} before SRAM is Write-protected.	40		250	μs
Chip Enable Recovery	t_{CER}		40	-	120	ms
V_{SS} to V_{PFD} (min) V_{CC} Rise Time	t_{RB}		1	-	-	μs

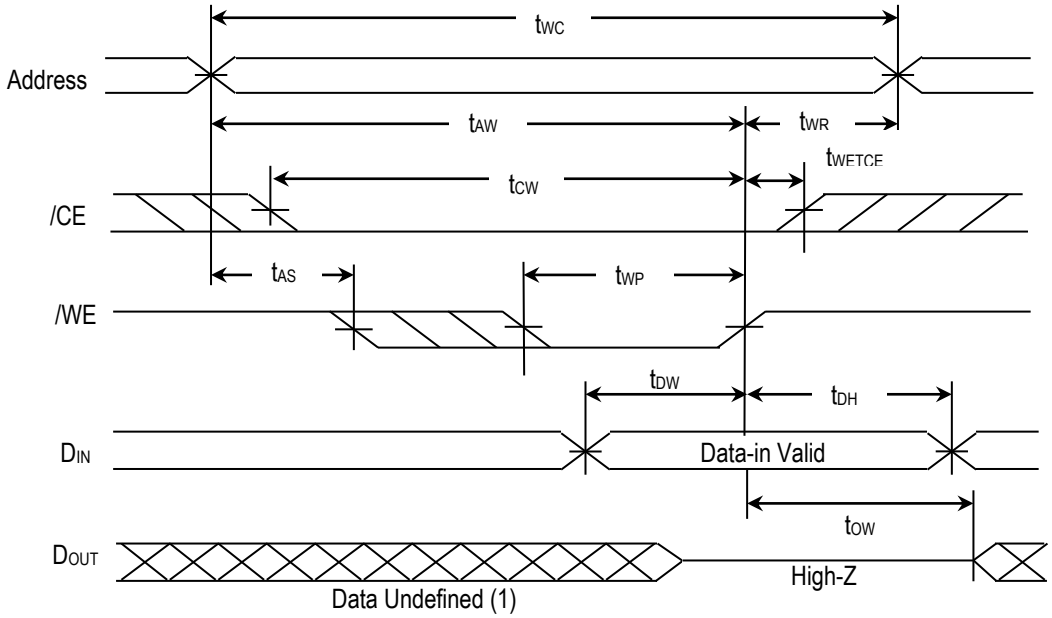
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TIMING WAVEFORM

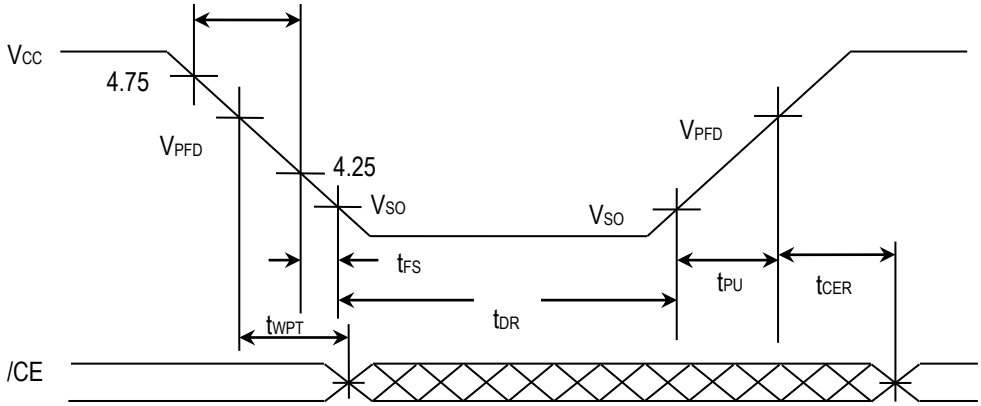
- Read Cycle



- Write Cycle



POWER-DOWN/POWER-UP TIMING

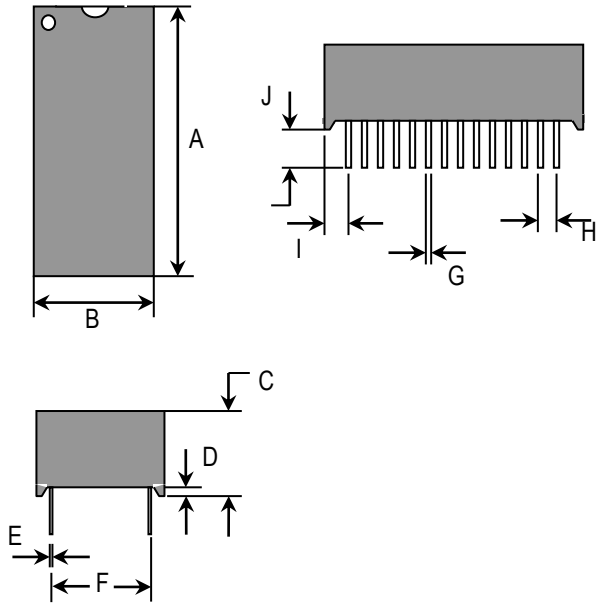


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PACKAGE DIMENSION

Dimension	Min	Max
A	1.650	1.710
B	0.700	0.760
C	0.365	0.380
D	0.012	-
E	0.008	0.013
F	0.590	0.630
G	0.017	0.023
H	0.090	0.110
I	0.075	0.110
J	0.150	0.190

All dimensions are in inches.



ORDERING INFORMATION

H M N 5128 D V LF – 70

- **Speed options :** 70 = 70 ns, 85 = 85 ns
- **LF :** Lead Free
- **3.3V Operating, Dip type package**
- **Device :** 512K x 8 bit
- **Nonvolatile SRAM**
- **HANBit Memory Module**

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